Large Size GEM R&D for SoLID

Kondo GNANVO University of Virginia

GEM detector team @ UVA:

Prof. Nilanga Liyanage, Dr Vladimir Nelyubin, Dr Kondo Gnanvo, Kiadtisak Saenboonruang, Seth Saher



SoLID GEM Design and Production

APV25 Electronics at UVa

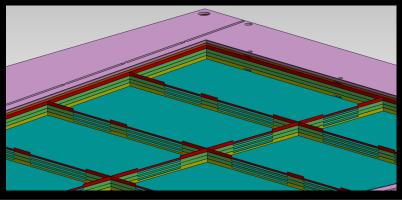
Test Beam @ FermiLab

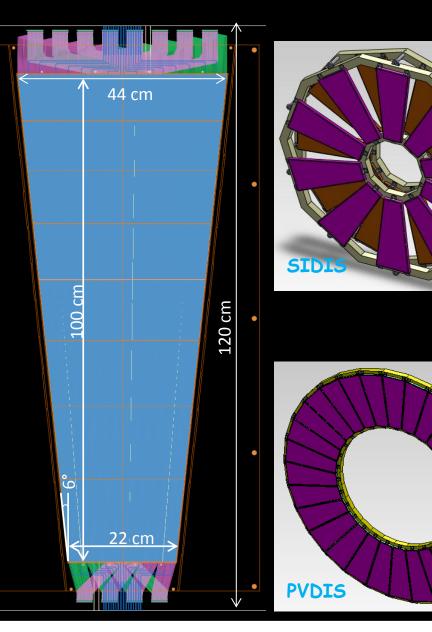


Large Area GEM R&D

Common R&D for various projects

- We have completed the design of Large trapezoidal triple GEM prototype for EIC and SoLID GEM trackers R&D.
- Chamber similar in size to CMS high Eta Muon Upgrade
- Design in collaboration with the GEM team at CERN (January 2013)
- Production of the GEM and R/O board on going at CERN

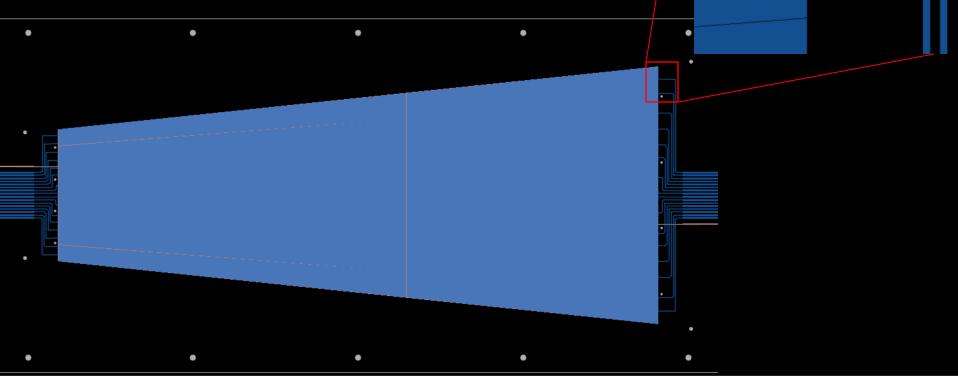






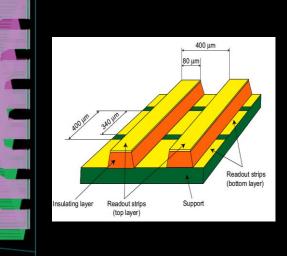
SoLID GEM Foil design

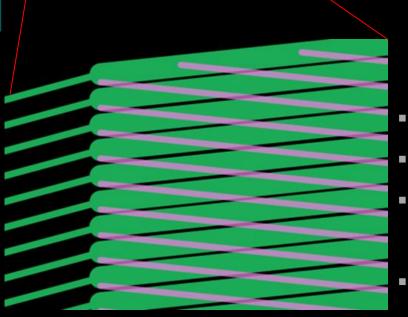
- The foil is divided into 32 HV sectors of roughly 100 cm2 with
- The V applied on the 16 sectors from the top and 16 from the bottom
- The chamber from the point of view of HV is divided in two parts





2D stereo-angle (U/V) flexible readout board



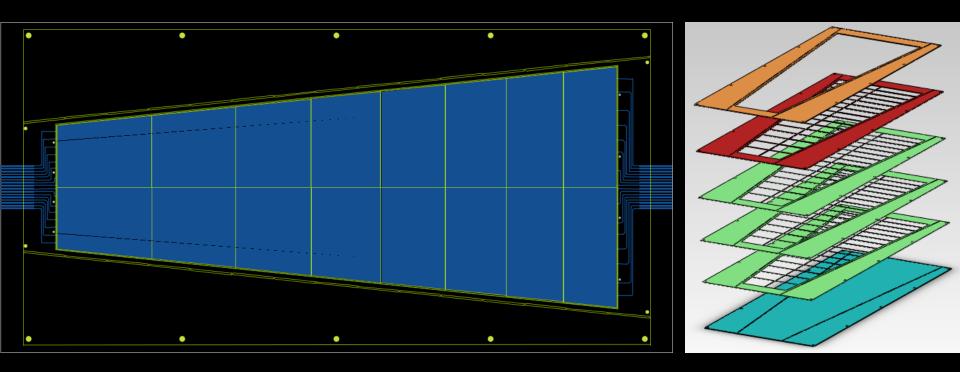


- COMPASS-like 2D stereo angle (12°) U/V readout board
- Pitch = 550 mm, top strips = 140 mm, bottom = 490 mm
- The support for the r/o based on Rohacell foam instead of honeycomb sandwiched between 100 mm fiberglass
 connectors on the top and bottom part of the r/o board



The Frames supporting the GEM foils

- Frames with the standard 300 μm spacers
- 8 mm width on the side and 60 mm width on top and bottom
- Extra frame material with alignment holes for the assembly
- Frame production by RESARM (Belgium)





Cross section of SoLID GEM prototype

- The gas flow system is pretty simple, only the entrance window frame and last GEM frame had inlet and outlet for the gas,
- Gas will exit the chamber from holes on one side of all frames
- Drift cathode is a GEM foil with copper only on inner side





SoLID GEM Design and Production

APV25 Electronics at UVa

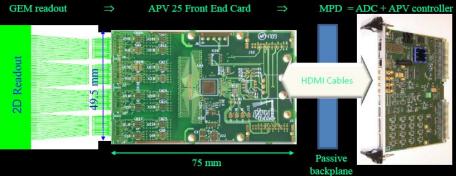
Test Beam @ FermiLab



APV25 Electronics @ UVa

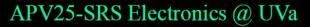
- Two apv25-based electronics available
 - CERN RD51 development of APV25-SRS electronics
 - APV25-MPD developped for the SBS experiment by P. Musico (Genoa Italy)

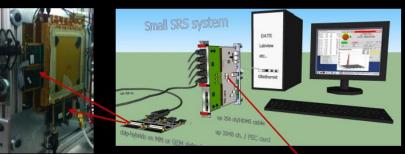
APV25-MPD Electronics



Main features:

- 2 "active" components: Front-End Card and VME64x custom module (MPD=Multi Purpose Digitizer)
- HDMI Copper cables between front-end and VME
- Optional backplane acting as signal bus, electrical shielding, GND distributor and mechanical support
- Developed by INFN, manufactured by a commercial company





Scalable Readout System (SRS)

- Portable readout system developed by RD51 Collaboration (CERN)
- Successfully tested with APV25 chip (many users and experiments)
 PV25 cards, 1 ADC board, 1 Data Concentrator board
 vata transferred through Gb Ethernet via UDP (ALICE DAQ)

 common platform for different chips (Bettle, VFAT, VMM1)



- Extensive study of the electronic gain and the noise of the two systems
- Performances of the apv25-SRS better than apv25-MPD Electronics



Study of the Noise of APV25 Electronics

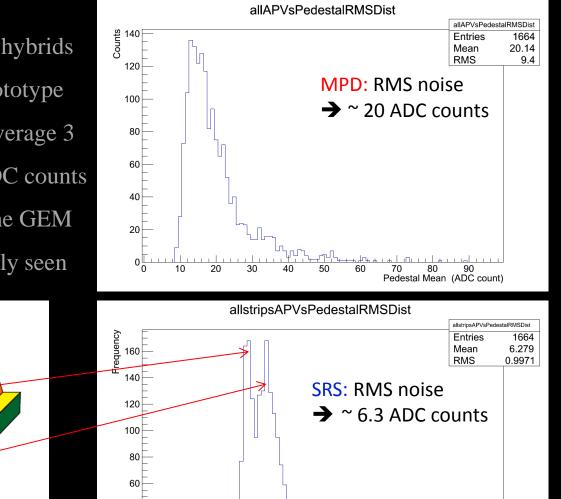
- Distribution of the noise of 13 apv25 hybrids cards connected to our SBS GEM prototype
- Average noise APV-MPD level on average 3 time higher than for APV-SRS on ADC counts
- With the APV25-SRS, the effect of the GEM readout strip capacitance can be clearly seen

400 µm

Readout strips (bottom layer)

80 µm

Support





Insulating layer

400 µm

340 µm

Readout strips

(top layer)

SoLID Coll. Meeting @ Hall A, JLab 03/23/2013

40

20

16

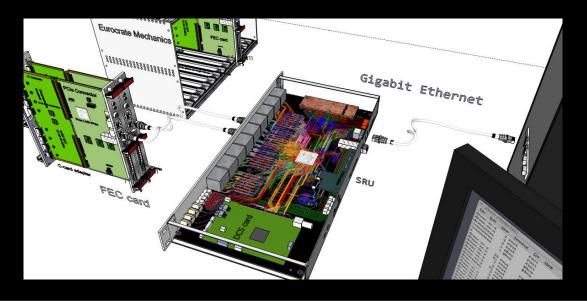
Pedestal RMS (ADC count)

14

18

Upgrading APV25-SRS electronics @ UVa

- 5 ADC boards and 5 FEC boards (V6) \rightarrow readout up to 80 APV25 Front end cards \rightarrow 10K channels
- FEC V6 → More FPGA resources, additional DDR memory, dual SFP etherrnet connector
- SRU (scalable Readout Unit) → a 1U x 19" box that serves DTC links of up to 40 EFC cards and multiplexes event data via a single Gigabit Ethernet link to the readout computer. It also provides I/O options for user-defined trigger and clock systems





- SoLID GEM Design and Production
- APV25 Electronics at UVa
- Test Beam @ FermiLab



FLYSUB-Consortium Test beam at FTBF

- FLYSUB is a consortium consisting of BNL, Florida Tech, Stony Brook University (SBU), University of Virginia (UVa), and Yale University. The groups have been working together for about two years
- Planning to assemble a set of detectors at FermiLab Test Beam Facility (FTBF) which is targeted toward tracking and PID components of an EIC detector.
- UVA will be bringing a the test beam:
 - SoLID/EIC large GEM prototype
 - one $50 \times 50 \text{ cm}^2 \text{ SBS GEM}$
 - small three 10×10 cm2 GEM for the tracking
- The main goal is to measure position resolution of the U/V readout of the SBS and SoLID GEMs and performances at high rate of both detectors.
- We are also going to test the new development of the SRS electronics that we are acquiring



Beam available at FTBF

- Electrons
 - Energy of beam: 10 GeV, Intensity: Single particles (if possible), Beam spot size: as small as possible
- Pions
 - Energy of beam: > 4 GeV, > 20 GeV, intensity: single particles (if possible); variations 1k
 100k particles/ 4 sec spill, Beam spot size: as small as possible; about 1 cm2
- Kaons
 - Energy of beam: > 13 GeV, Intensity: single particles (if possible)
- Protons
 - Energy of beam: > 27 GeV, Intensity: single particles (if possible), Beam spot size: as small as possible



FLYSUB-Consortium Test beam at FTBF

FTBF Fermilab Test Beam Facility

PPD | 🛟 Fermilab

Fermilab: 🔥 Home 🛛 🚱	🕢 Help 🛛 🔁 Phone Book 🛛 🕕 Fermilab at Work				Searc	h GO
10	122	- A -	1. 16		122	
FTBF	Schedu	ıle				
Become a User	This is the official	a cha dula far ETDE	activities. Tunical run parias	la actabliab baam an l	Madaga dava and rup	through Tugo dou
Working at FTBF	This is the official schedule for FTBF activities. Typical run periods establish beam on Wednesdays, and run through Tuesday. Scheduling meetings are held most Tuesdays at 2pm. To schedule beam time please see our <u>Guidelines for Requesting Beam</u> and contact the Test Beam Coordinator.					
Beam Details						
Facility Details	Accelerator I	VOvA Upgra	de Shutdown disab	les Test Beam f	rom April 30, 2	012 ~ July 1, 2013
Instrumentation	MTest FY13	MTest FY1	MCenter FY13	Previous Years	Calendar	
High Rate Tracking				2013		
Location	Dates	Experiment	Descr	iption	User	Area Contact
	- 1. Oct 2 - Oct 8	<u>T1037</u>	FLYSUB-Consortium		Primary	MT6-ALI <u>Dehmelt</u>
Test Experiments	_					
Schedule	2. Oct 9 - Oct 15	<u>T1037</u>	FLYSUB-Consortium		Primary	MT6-ALIDehmelt
Contact & Personnel						
Performance & Feedback	3. Oct 16 - Oct 22	<u>T1037</u>	FLYSUB-Consortium		Primary	MT6-ALI <u>Dehmelt</u>
Pictures						



SoLID Coll. Meeting @ Hall A, JLab 03/23/2013

To summarize

- Complete the design for the SoLID/EIC large trapezoidal GEM prototype
- Production of the GEM foils and 2D U/V readout board on going at CERN → expect to have them delivered by July 2013 and built the chamber by September 2013
- Upgrading our apv25-SRS electronics capacity from 2K channels to 12K channels
- We are scheduled for a test beam at Fermilab)ctober 2013 to test the performances of the SoLID/EIC and SBS detectors prototypes as well as testing the new features of the large size SRS electronics that we are purchasing.

