SoLID DAQ / electronics test plan

Short term plan

- Must
  - Trigger FADC test :
    - Test waveform readout (Bob , Alex)
    - Calorimeter trigger preliminary design (Alex , Electronics group , ?)
  - APV25 max rate
    - INFN (Alex , ?)
    - SRS (Alex, Kondo, Mitra, Jones)
  - SIDIS rates : EC LC GEM (Zhiwen, Michael, Ole)
  - MaPMT EC test (Rakitah, Yuxiao , Zhiwen)

Long term plan

- Test trigger logic and FADC performance
- Simulation digitization
- SIDIS GEM occupancy from G4 full MC
- SIDIS rates from G4 simulation full MC
- MRPC development custom electronics
- L3 reduction factor and ressource need test algorithm

MaPMT test

- Test optical cross talk between pixel
- Linearity with DC current
- Test linearity with FADC

MaPMT drawback

- Optical cross talk (highly dependent on mechanical design of coupling)
- Electronic crosstalk
- Gain non uniformity (could compensate with FADC but signal has to be out)
- Pixel with higher rate might drive gain
- Mechanical coupling difficult

Longer term

- FADC system UVA / Temple / WM /Duke

(about 30 K$ worth electronics each should be able to borrow FADC,TI,SD need VXS crate 15K$ and CPU 3.5 K$)

- Temple :
  - Define and test FE maybe adapt base for optimization with FADC (signal shape)
- UVA : realistic response of trigger with detector

- Beam test