GEM Electronic System Status

- New releases of electronic boards:
  - MPD v 4.0
  - Backplane 5 slot short (for UVa design)
  - APV Front-End with Panasonic connector
- Firmware Update on MPD v 4.0
  - Some preliminary tests on VME intrerface

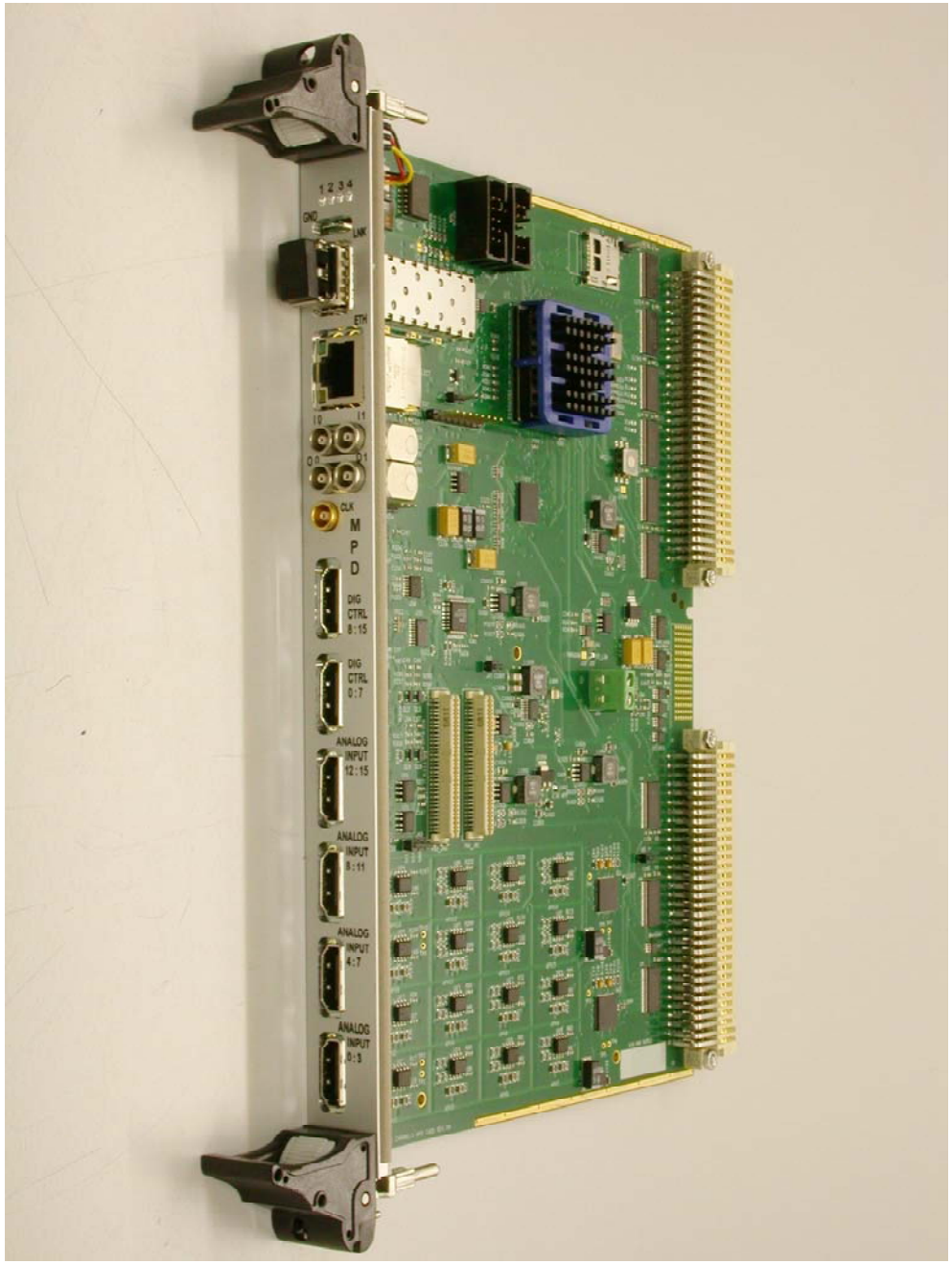
Paolo Musico and Evaristo Cisbani

MPD v 4.0

2 prototypes ready (1 @UVa)

Hardware modifications:

- Used HDMI-A connectors for analog and digital signals
- Adopted larger FPGA (+20%)
- Replaced DDR with DDR2 (128 MB)
- 110 MHz system clock
- Removed USB support
- Moved from Flash to SD-Card
- Added front panel coax clock
- All spare signals go to PMC compliant connectors
- Improved ADC power distribution
- Added optional termination on ADC inputs

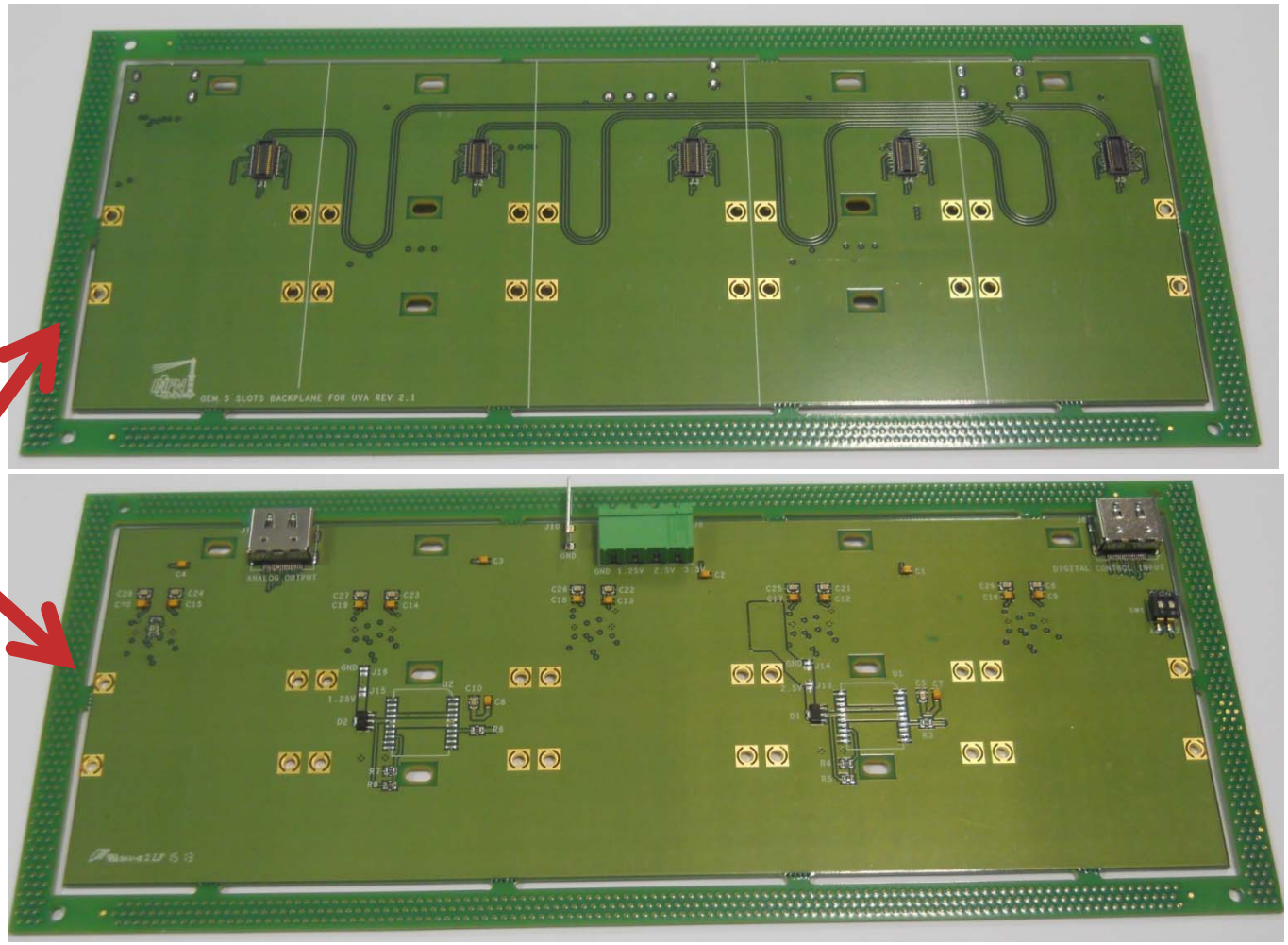


Backplane 5 slots "short"

TOP SIDE

External frame used only for assembly: will be removed

BOTTOM SIDE



Dimensions: 254.3 x 88.5 mm
Front-end boards pitch: 51.2 mm

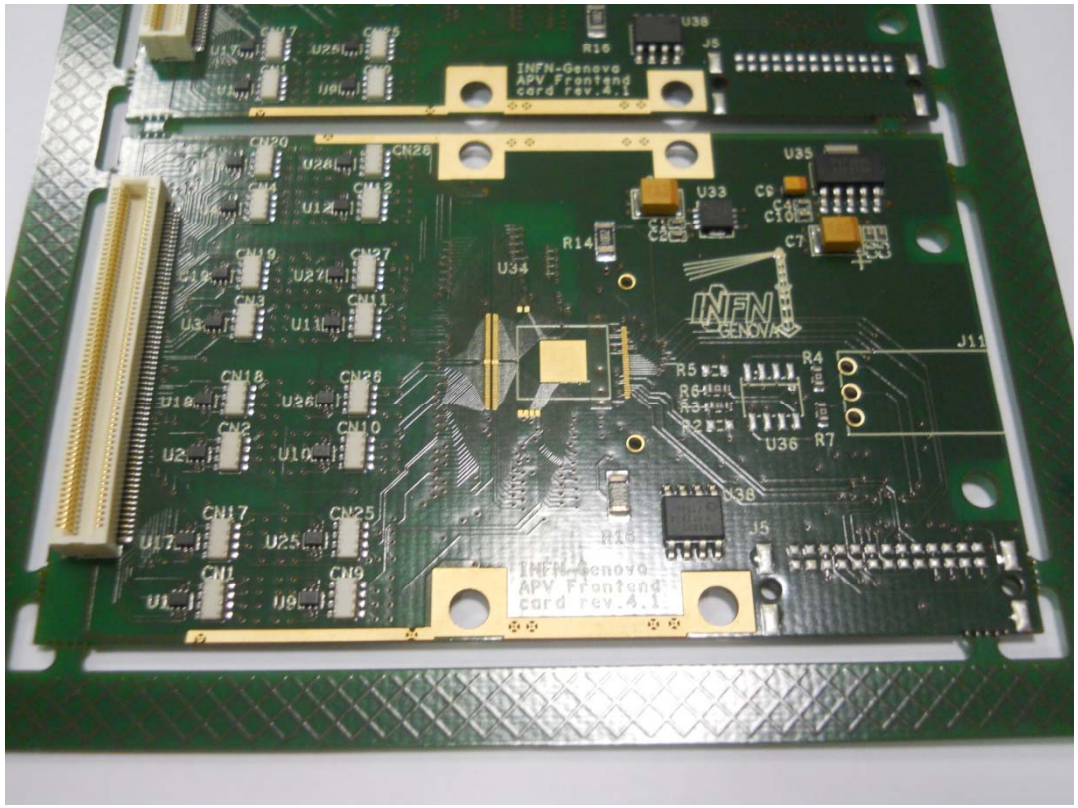
8 boards assembled, to be tested

APV Front-End w Panasonic conn.

Picture taken after SMD assembly

APV25 not yet present

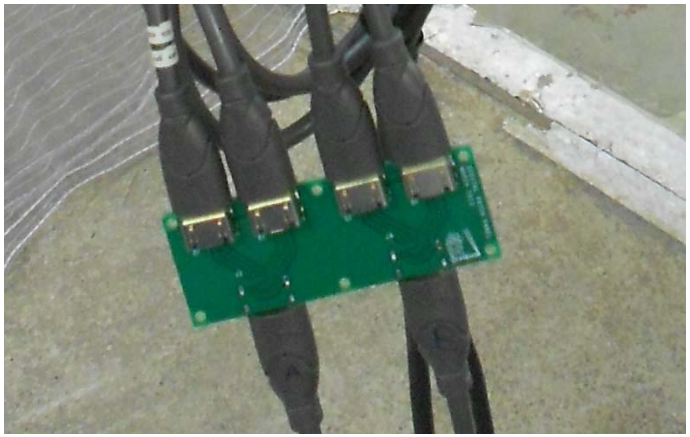
External frame will be removed



Dimensions: 80.5 x 49.5 mm → 3.5 mm longer to house different connector
25 boards assembled: bonding in progress, ready by next week. Test will follow
Used an external company for bonding: Siae Microelettronica in Milan

HDMI Patch Panel boards

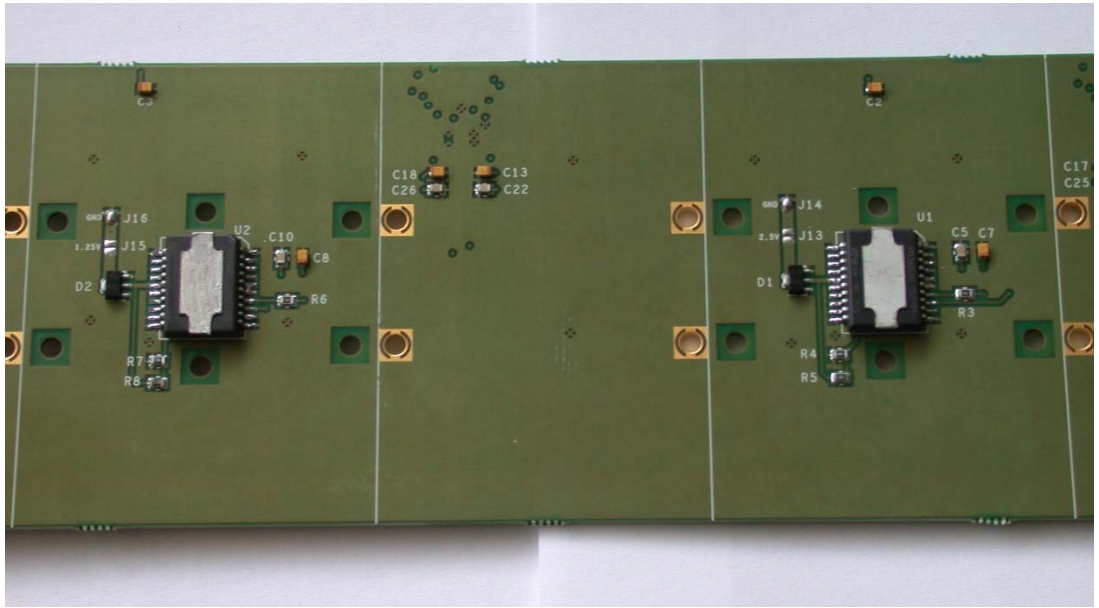
- Two Patch Panel passive boards have been produced
  - Digital: distribute the control signals to 2 independent backplanes (I^2C is common)
  - Analog: arrange up to 3 x 5 channels into 4 HDMI-A cables



Digital Patch Panel
in the latest test beam
@ DESY

RAD HARD LVPS TESTING

- LHC4913 Rad Hard LVPS have been put on a backplane and powered some front-ends during latest DESY test beam
- Noise not degraded



MPD v 4.0 firmware update

- Revised memory mapping
  - Older map was too fragmented and A32 only
  - New release adopt A24 addressing for configuration and debug and A32 for data readout
- VME interface state machine rewritten
  - D64 read only cycles: MBLT, 2eVME, 2eSST
  - 2eSST simulated peak speed: 148, 222, 296 MB/s
- TBD
  - Slave termination
  - Multiboard block transfer

MPD v 4.0 VME interface testing

- A32D64 cycle tested with STRUCK SIS-3104
  - 2eSST not supported
  - Dedicated implementation: test module with LFSR data generator and system clock = 106.67 MHz
  - Average speed measured by software: 100 transfer 4MB each. Data integrity checked for each block.

CYCLE	DTACK period	Peak Speed	Average Speed
BLT (32 bit)	16 ck = 150 ns	26.6 MB/s	24.3 MB/s
MBLT	17 ck = 159 ns	50.3 MB/s	47.8 MB/s
2eVME	10+10 ck=93+93 ns	86.1 MB/s	73.6 MB/s

Next Steps

- Test 2eSST:
  - STRUCK has a firmware upgrade: try to use it
  - use different controller
- Implement slave termination and multiboard block transfer

- Start production for front-ends and MPDs Backplanes already assembled, equipped with LHC4913 rad-hard LVPS.

Cost Estimation

BOARD	Quantity	Unit Price (€)
APV Front End	5 (prototypes)	320-390
APV25 & bonding	100	120-150
not included	600	110-130
Backplane	5 (prototypes)	320-360
	30	160-190
	120	120-140
MPD	1 (prototype)	3900-4500
	10	2300-2700
	40	2100-2400

Estimation based on what we paid
Some discount can be negotiated with EES for large quantities
VAT, other taxes, customs duties, transportation not included