# SBS DAQ

SBS collaboration Meeting

Alexandre Camsonne

July 13th 2017

# Outline

- GMn ERR
- GEp plan
- GEM data reduction
- HCAL progress
- Fastbus
- Network upgrade
- DAQ disks
- SILO capability
- Tape cost
- TDIS TPC
- Manpower
- Simulation work
- Conclusion

# Expected trigger rates GMn

Preferably single electron trigger to avoid biased in neutron detector

| Q^2<br>GeV^2 | n+p QE xsec<br>fb | L(per atom)<br>10^38/cm^2/s design | QE rate<br>Hz | Beam time<br>Hours | Total<br>Hz |
|---|---|---|---|---|---|
| 3.5 | 6700 | 0.35 | 235 | 12 | 2100 |
| 4.5 | 1015 | 0.7 | 70 | 12 | 1400 |
| 5.7 | 97.9 | 1.4 | 13.5 | 18 | 140 |
| 8.1 | 47.4 | 1.4 | 6.6 | 18 | 390 |
| 10.2 | 31.6 | 0.7 | 1.5 | 24 | 210 |
| 12 | 5.04 | 1.4 | 0.7 | 36 | 200 |
| 13.5 | 6.25 | 1.4 | 0.87 | 96 | 100 |

Maximum trigger rate 2.1 KHz, assume factor 2 safety margin for 4.2 KHz for low $Q^2$

less than 500 Hz at high $Q^2$

Single electron trigger is a good option

( possibility to add Cerenkov in the trigger if needed )

# GEM occupancy and data rates

- occupancies from Q2 = 13.5 GeV2, with luminosity 2.8 10^38 $A^{-1}$ $cm^{-2}$ $s^{-1}$ (44uA on 10cm LD2 target) and rates from low Q2 point : 1.3 KHz

| | Rate per (KHz/cm2) | Rate per plane (MHz) | hits in 325 ns | Occupancy (%) | strip hits | x2 XY (strips) | x6 samples | Evt size (bytes) | Rate MB/s |
|---|---|---|---|---|---|---|---|---|---|
| **1** | **89.6** | **537.6** | **174.72** | **27%** | **612** | **1223** | **7338** | **29357** | **123.30** |
| **2** | **101.6** | **609.6** | **198.12** | **31%** | **693** | **1387** | **8321** | **33284** | **139.79** |
| **3** | **101.4** | **608.4** | **197.73** | **30%** | **692** | **1384** | **8305** | **33219** | **139.52** |
| **4** | **98.1** | **588.6** | **191.295** | **29%** | **670** | **1339** | **8034** | **32138** | **134.98** |
| **5** | **89.3** | **535.8** | **174.135** | **27%** | **609** | **1219** | **7314** | **29255** | **122.87** |
| | | | | | | | | **Total** | **660.46** |

Worse case scenario using High Q2 occupancies with low Q2 rates

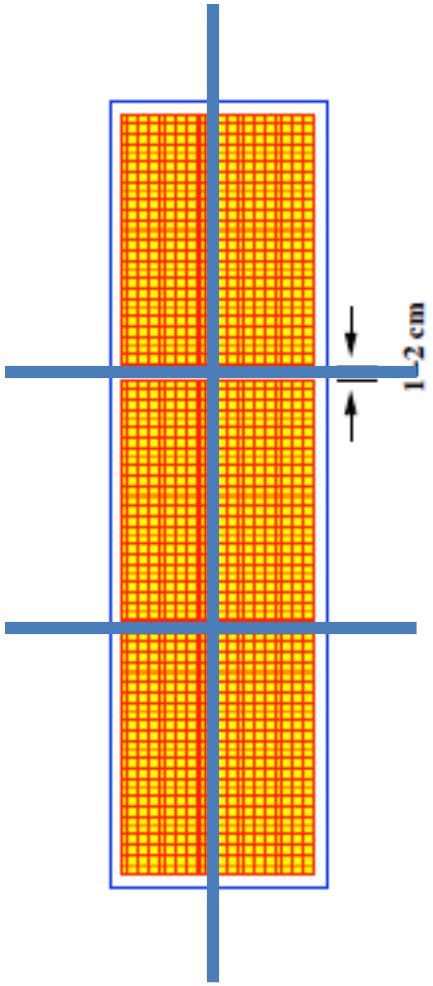
Deconvolution on SSP : **expect factor of 3 reduction about 220 MB/s**

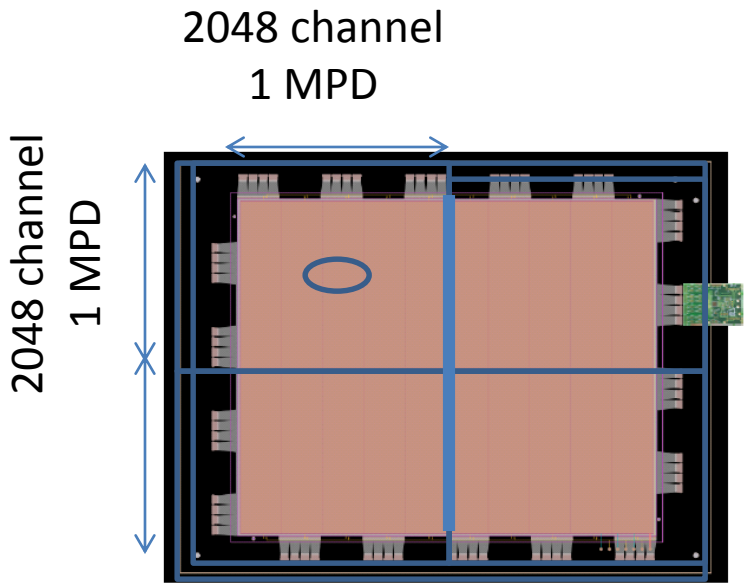
# Data rates GEp5

| Detector | Rate | Channels | Occupancy | Data size Bytes | Data rate MB/s 5 KHz 3 samples | Geometrical factor | Data size geo Reduc MB/s | Double for 6 samples MB/s |
|---|---|---|---|---|---|---|---|---|
| Front Tracker | 400.00 | 49000.00 | 1 | 589149 | 2946 | 3.00 | 919 | |
| Second Tracker | 130.00 | 61440.00 | 1 | 738720 | 3694 | 5.00 | 660 | |
| Third Tracker | 64.00 | 61440.00 | 1 | 738720 | 3694 | 5.00 | 660 | |
| **Total** | | **171880.00** | | **2066589** | **10332** | | **2459** | **4918** |

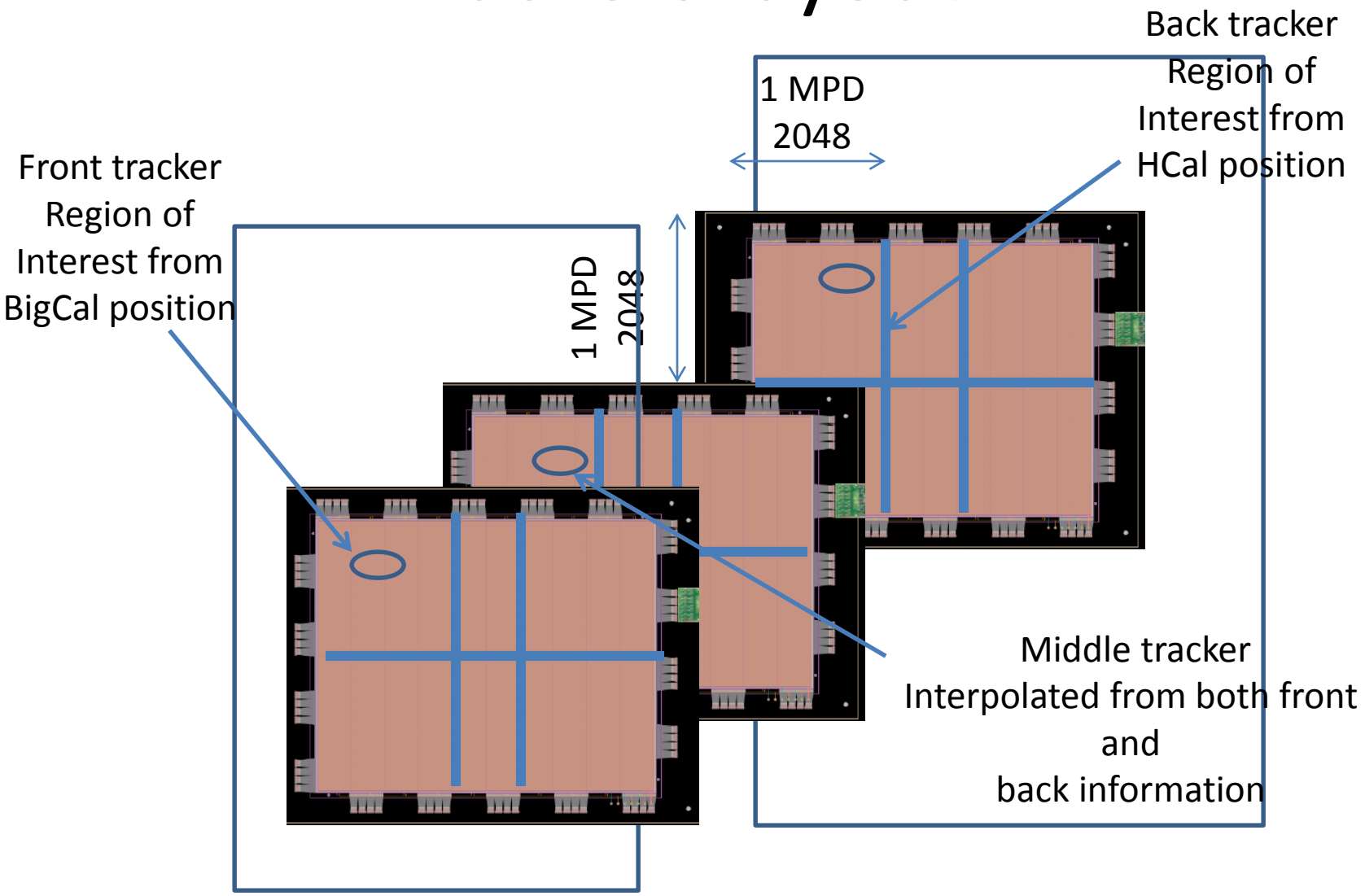
Need further reduction by using deconvolution and maybe clustering on SSP

# Front Tracker layout

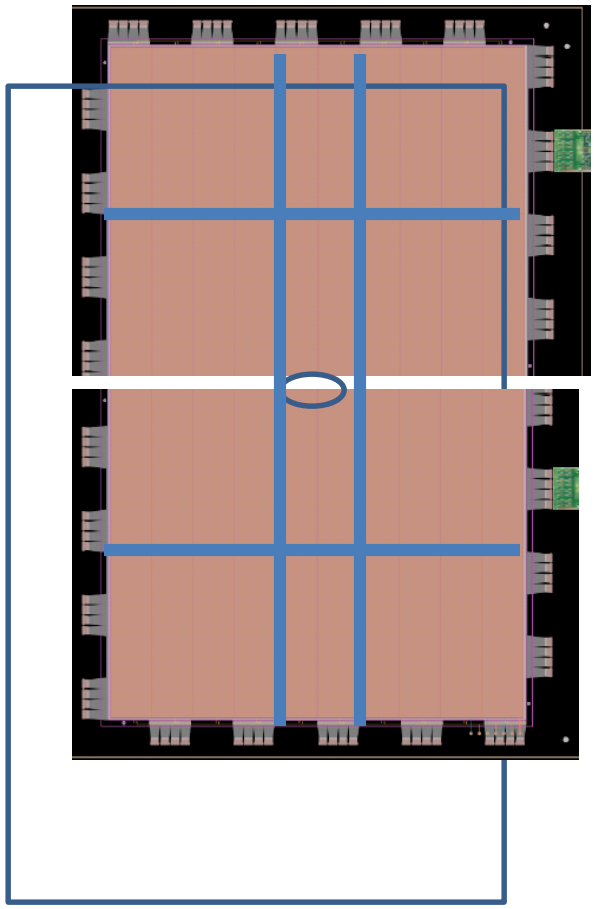


# Trackers layout

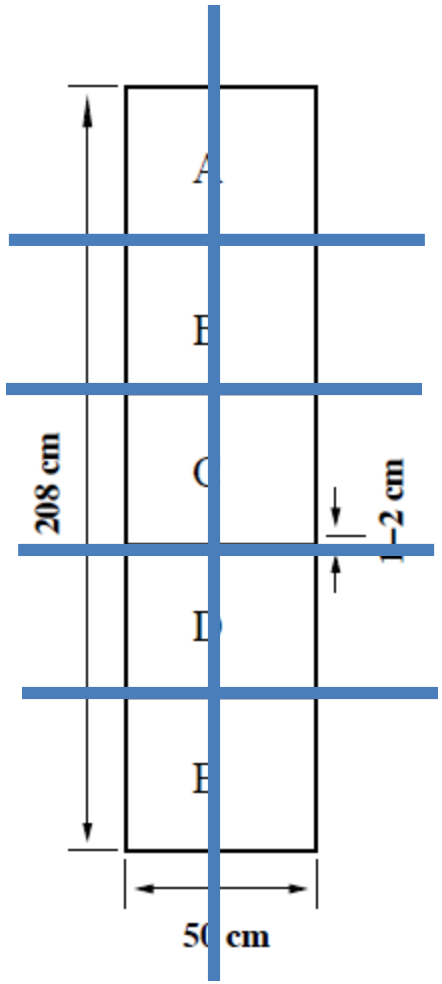


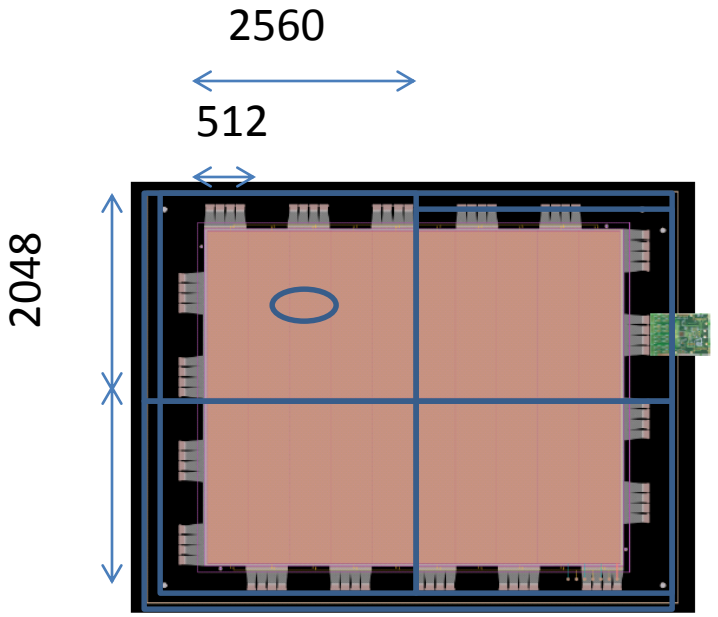
# Trackers layout



Worst
case
configuration

# FPP Tracker layout

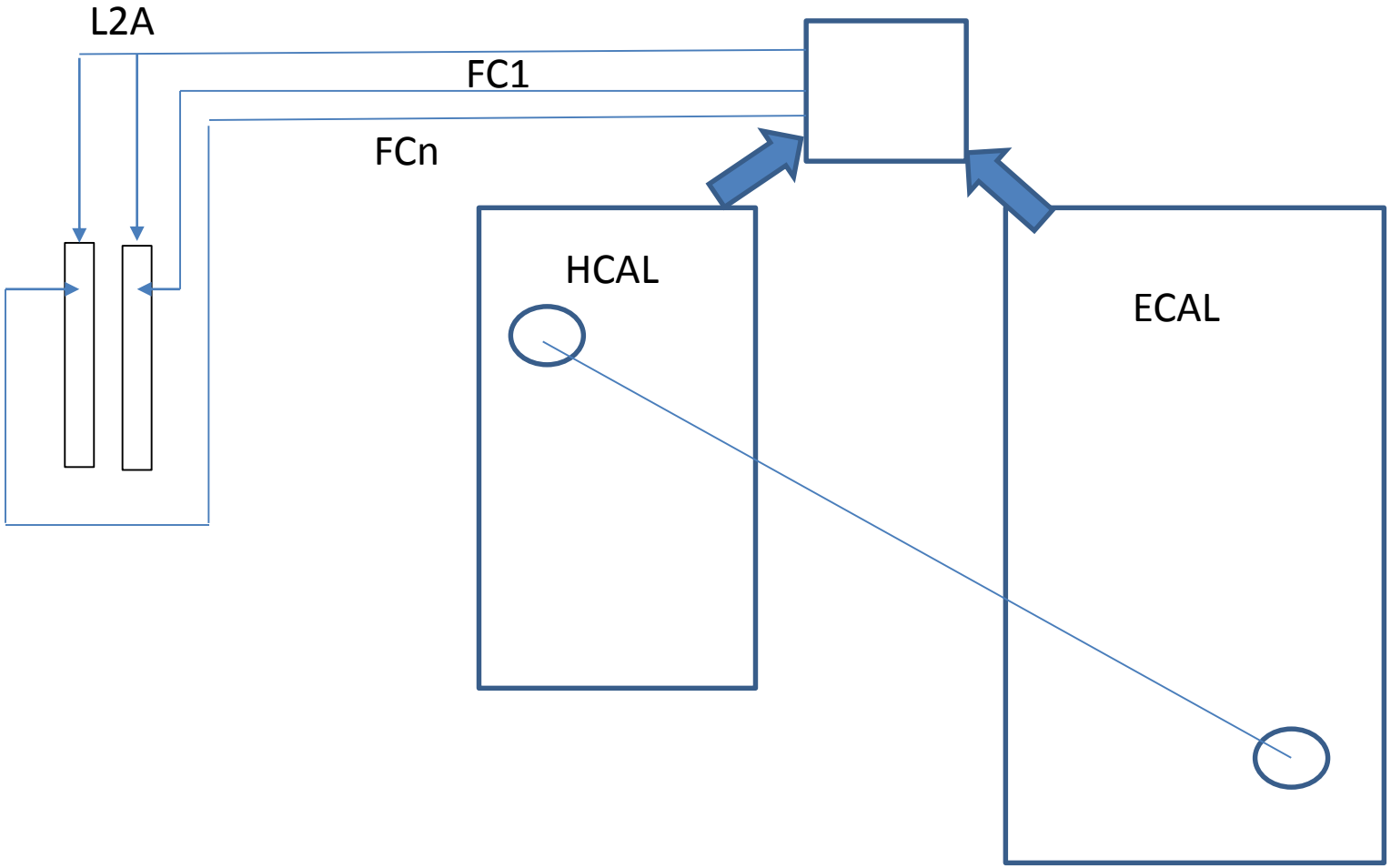


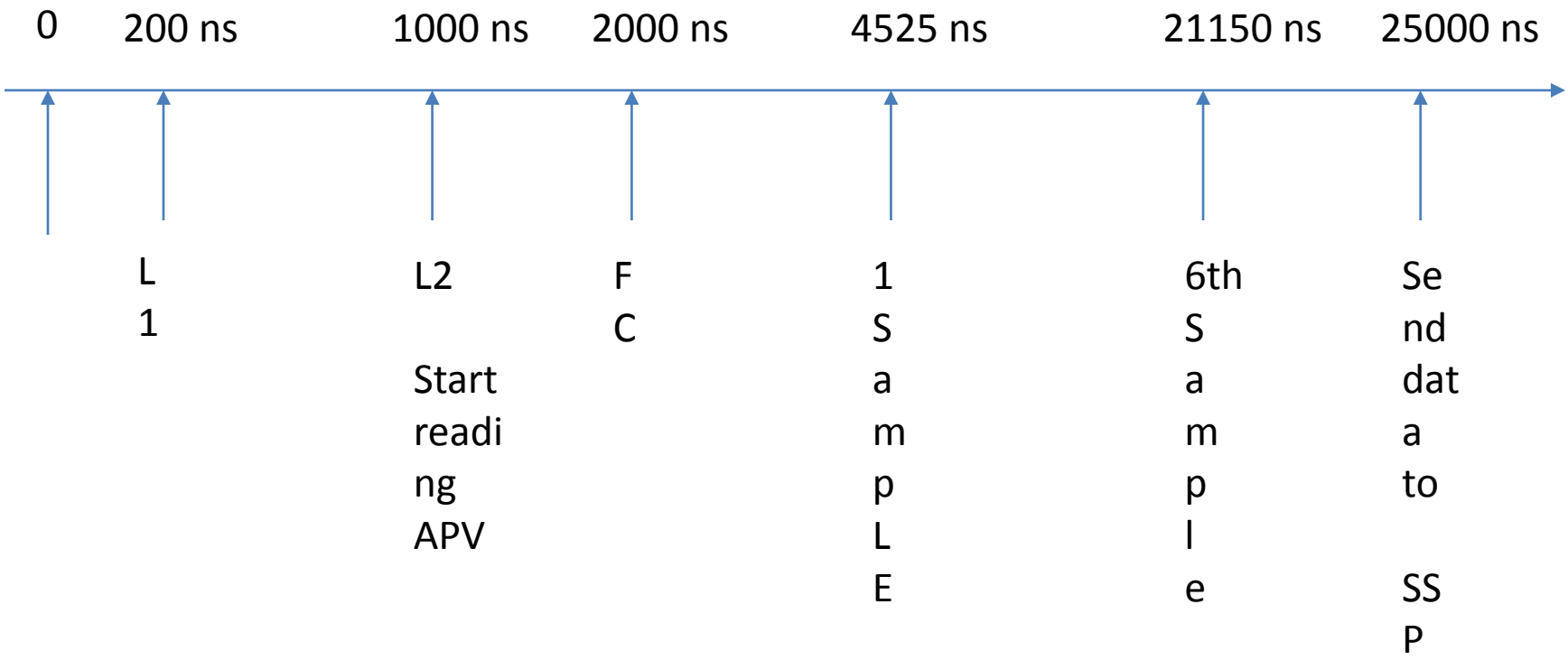
# Geometrical MPD suppression

- Different methods
  - Use on user input Fast clear MPD
    - pro : MPD stay in synch
    - con : need more MPD firmware work
  - only issue trigger for modules of interest and have SSP keep track of number of events to be read
    - pro : no change to MPD
    - con : MPDs out of synch and rely on SSP for synchronization, more firmware work
  - do on SSP or VTP
    - pro : no hardware change
    - con : resource intensive, synchronization issues, more work for Ben !

# MPD fastclear



# MPD Fastclear timing



# SSP readout performances

1 backplane, 3 APVs, no zero suppression

| Nb samples | Blocklevel | Rate (kHz) | Effective rates (kHz) | Effective rates 8 APV (kHz) | Data rate | |
|---|---|---|---|---|---|---|
| 1 | 1 | 23 | 23 | 8.6 | 26 | |
| 3 | 1 | 15 | 15 | 5.6 | 50 | |
| 3 | 2 | 15 | 15 | 5.6 | 100 | |
| 3 | 4 | 7 | 28 | 10.5 | 85 | |
| 3 | 4 | 10 | 40 | 15 | 100 | No transfer |

Disk speed : 98.2 MB/s
Network : 117 MB/s
Backplane VME : 100 MB/s

Can saturate backplane
Expected rate around 15 KHz per MPD

# Timeline GEM

- Implement first pass SSP data reduction this summer: common noise suppresion running average, 6 samples discard first and 6$^{th}$ sample if highest amplitude
- Second pass if required January 2018 with higher priority from Electronics group

( CLAS12 run in October )

# Fastbus readout

- Time : 1877S
- Amplitude 1881M
- Fastbus max transfer speed : 40 MB/s can use either Intel or Old vxworks VME CPU

- ECal : 4 sets of 3 crates, will be able to test performance about 50 MB/s at 100 % occupancy
- Cdet : 9 Fastbus crates about 11 MB/s at 10 % occupancy

# Fastbus

- Good progress from Bob
- Tools to check synchronization available
- still development to handle event blocking in decoding

# HCAL readout

- 288 channels
- 2 VXS crates , 18 FADCs
- 1.5 MHz singles
- 16 block clusters
- FADC 250 MHz 12 bit = 2 bytes
- 10 samples : 320 bytes , 57.6 MB/s at 100 % occupancy
- VETROC or F1 : high resolution TDC, need NINO
- VTP need to developped
- 2 VETROC for ECAL sums input and MPD fast clear

# VTP

- New Hall B CTP
- Larger FPGA than GTP
- 2x10 Gig optical links
- Plan development of VXS readout for FADC and possibly SSP
- 7 K$
- Have 2 for HCAL

# HCAL trigger status

- VTP installed
- Firmware loaded, need testing

- No CODA ROC planned for CODA 2.6 only for CODA3 so no VTP readout
  - Need to negotiate with DAQ group for CODA 2.6 for readout
  - Or need to upgrade all Fastbus CPU to Intel for VTP readout ( 10 GigE )
  - or readout VTP with a CPU or PC at 10 gigE

# Network upgrade

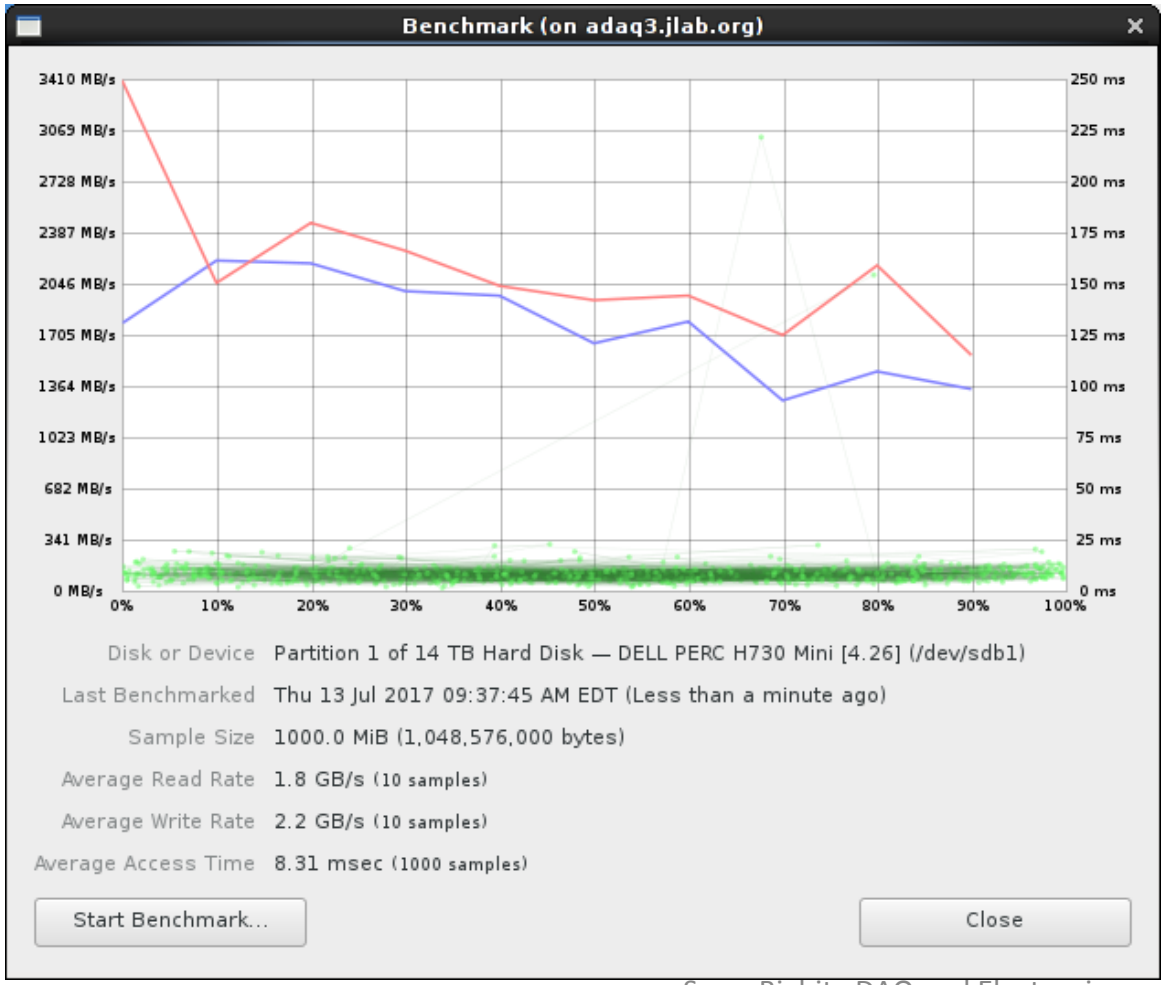
- Replace hall A router with an Arista switch, reuse existing hall A router as the switch for the racks. This provides dense 10Gig aggregation, with 40Gig expandability. Estimate $30K, 3 month lead time.

- Single Mode Fiber Installation in the hall ( required for any speeds>1Gbit/sec), rough estimate $30K, 6 month lead time.
  Counting House to left arm, 24 strand
  Counting House to right arm, 24 strand
  Counting House to Labyrinth, 24 strand
  Counting House to Hall Floor Rack Area, 24 strand

- 40Gig uplinks to CEBAF center ($20K upgrade to item 2).

- Bottomline : 10 Gig capability 30 K$ + temporary fiber 10 gigE

# Counting house DAQ disks




- Raid array on adaq3
- several disks

- 1GB/s seems doable

- Might need to upgrade to hold 72 hours of data : 259 TB

( Hall D about 28 K$ per raid array )

# SILO capabilities

- Mix of LTO 5 and 6
  - 14 drives LTO 5 and 6 = 2 GB/s
  - up to 16 drives
  - each LTO7 drive is 300 MB/s about 10 K$ each
  - Max : 16 * 300 = 4.8 GB/s
  - to handle 1 GB/s : 4 drives about 30 K$
  - increase to 4 GB/s ( 1GB + dup + read ) about 120 K$
  - need to write and read at same time
  - LTO8 available in 4 to 5 years
  - Need to let IT know our real needs might need more drives

# Tape cost

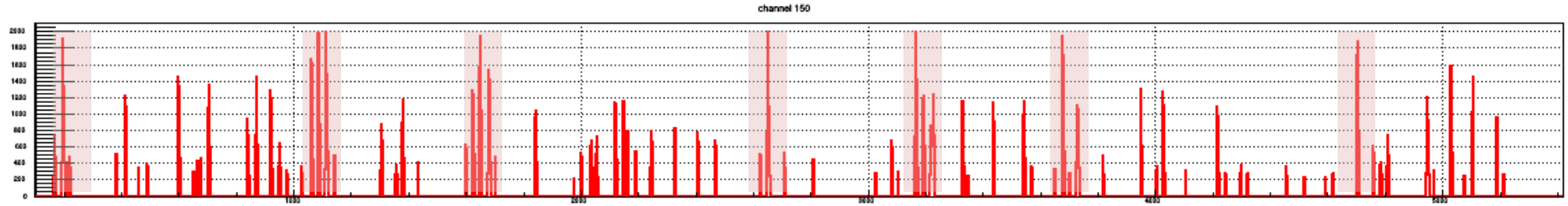
| | | Days | Weeks | Data rate | Seconds | Total data TB | Double | LTO5 in k$ | LTO6 in k$ | LTO7 in k$ | LTO8 in k$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| E12-12-09-019 | GMN | 25 | 3.57 | 500 | 2160000 | 1080 | 2160 | 108 | 65 | 27 | 13 |
| E12-09-016 | GEN | 50 | 7.14 | 500 | 4320000 | 2160 | 4320 | 216 | 130 | 54 | 25 |
| E12-07-109 | GEP/GMP | 45 | 6.43 | 1000 | 3888000 | 3888 | 7776 | 389 | 233 | 97 | 46 |
| E12-09-018 | SIDIS | 64 | 9.14 | 1000 | 5529600 | 5529.6 | 11059.2 | 553 | 332 | 138 | 65 |
| | | | | | | | | | | | |
| | Total | 184 | 26.29 | | 1589760 | 12657.6 | 25315.2 | 1,265.76 | 759.46 | 316.44 | 148.33 |

# TDIS

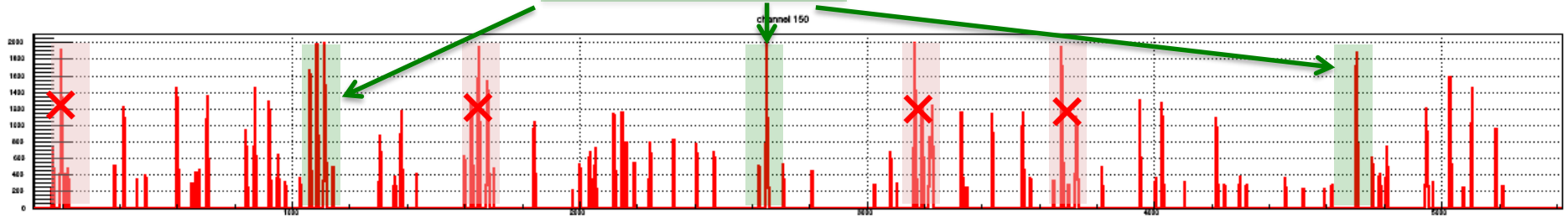
- BNL TPC readout
- https://eic.jlab.org/wiki/index.php/Trigger/Streaming_Readout
- streaming TPC readout

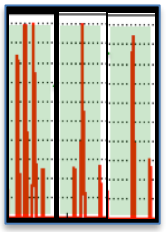
# Streaming Readout concept

The streaming data are recorded all the time, and broken up in chunks above threshold




Only chunks correlated with triggered events are then kept

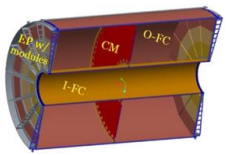


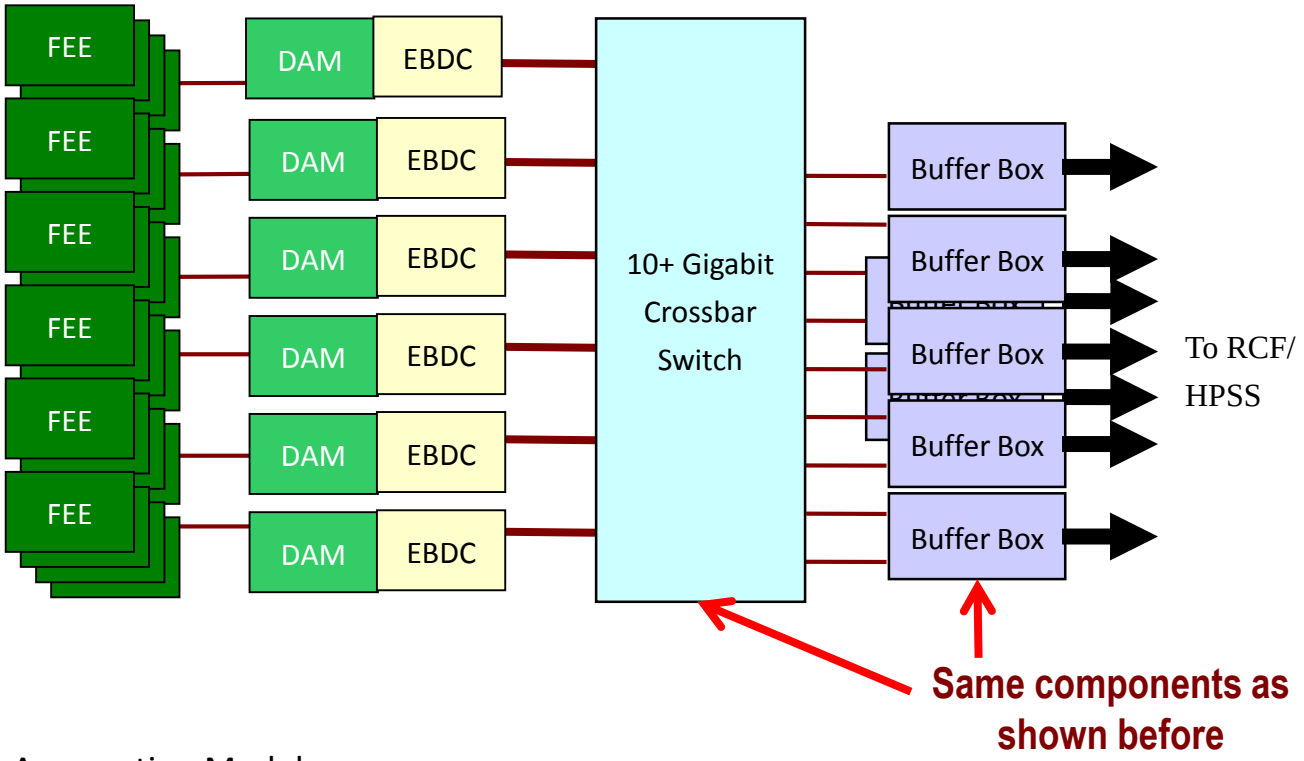
This results in a greatly reduced data stream

The real-time processing demands are very high

# The streaming TPC readout




TPC




- DAM Data Aggregation Module
- EBDC Event Buffering and Data Compressor

# Front-End – ALICE SAMPA Chip

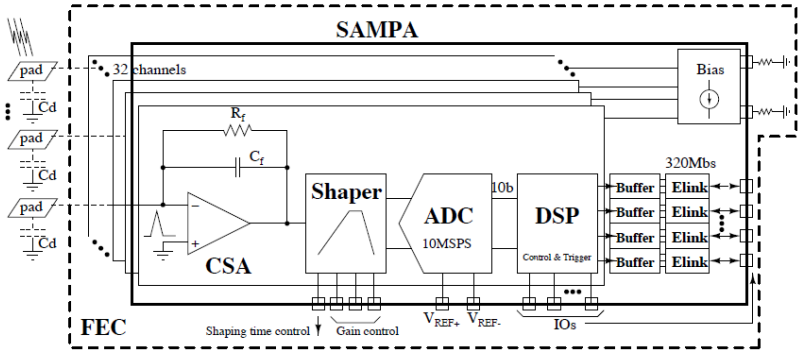



Figure 6.4: Schematic of the SAMPA ASIC for the GEM TPC readout, showing the main building blocks.

ASIC developed for ALICE for the TPC

More functionality than we would need while streaming

10Ms/s @ 10Bit -> 100Mbit/s internally, 32channels

This oversubscribes its external links

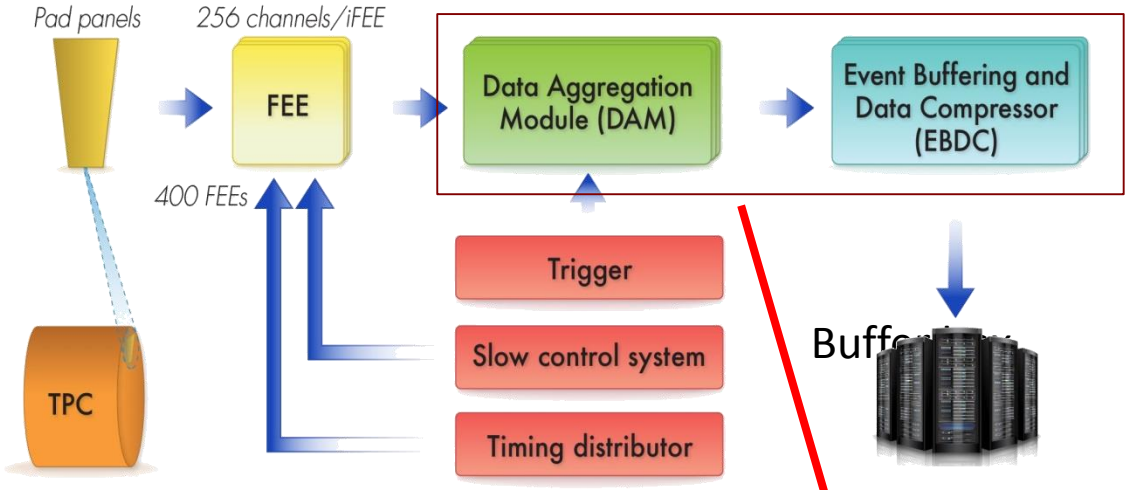
Above-threshold waveform delivery – send chunks of the waveform around samples “sticking out” above a threshold + bookkeeping

Estimate 5 samples/channel/hit and 3 channels -> 15 samples/”hit”

8 Sampa chips on one Front-end card – 256 channels

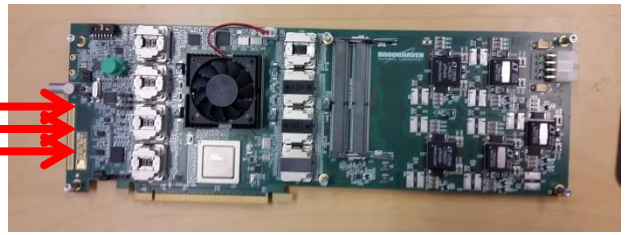
~400 FEE cards

# Data path overview




About 10 PCs (EBDC) with one FELIX card each


Up to 48 FEE->Card (48 fibers)



ATLAS Felix PCIe card

+

# Man power

- Fastbus/ECAL
  - M. Jones, B. Michaels, J. Gu, B. Moffit
- HCAL
  - B. Raydo, A. Camsonne
- GEM readout
  - E. Cisbani, B. Moffit, A. Camsonne, P. Musico, B. Raydo, S. Riordan, D. Di
- BigBite : E. McLelan

# Simulation work

- Test data reduction algorithm on simulated data for GEM

- Occupancies different detectors GMn, Gep for different kinematics start to look at SIDIS, TDIS

# Conclusion

- Need evaluate data rates after reduction for all experiments especially GEp5 aiming at 500 MB/s (no major upgrafe )
- If more than 1 GB/s need network/SILO/disks upgrade need to discuss with IT
- Ongoing development on SSP : first iteration end of summer
- HCAL trigger in testing
- Good progress Fastbus
- Look ahead future experiments SIDIS, TDIS