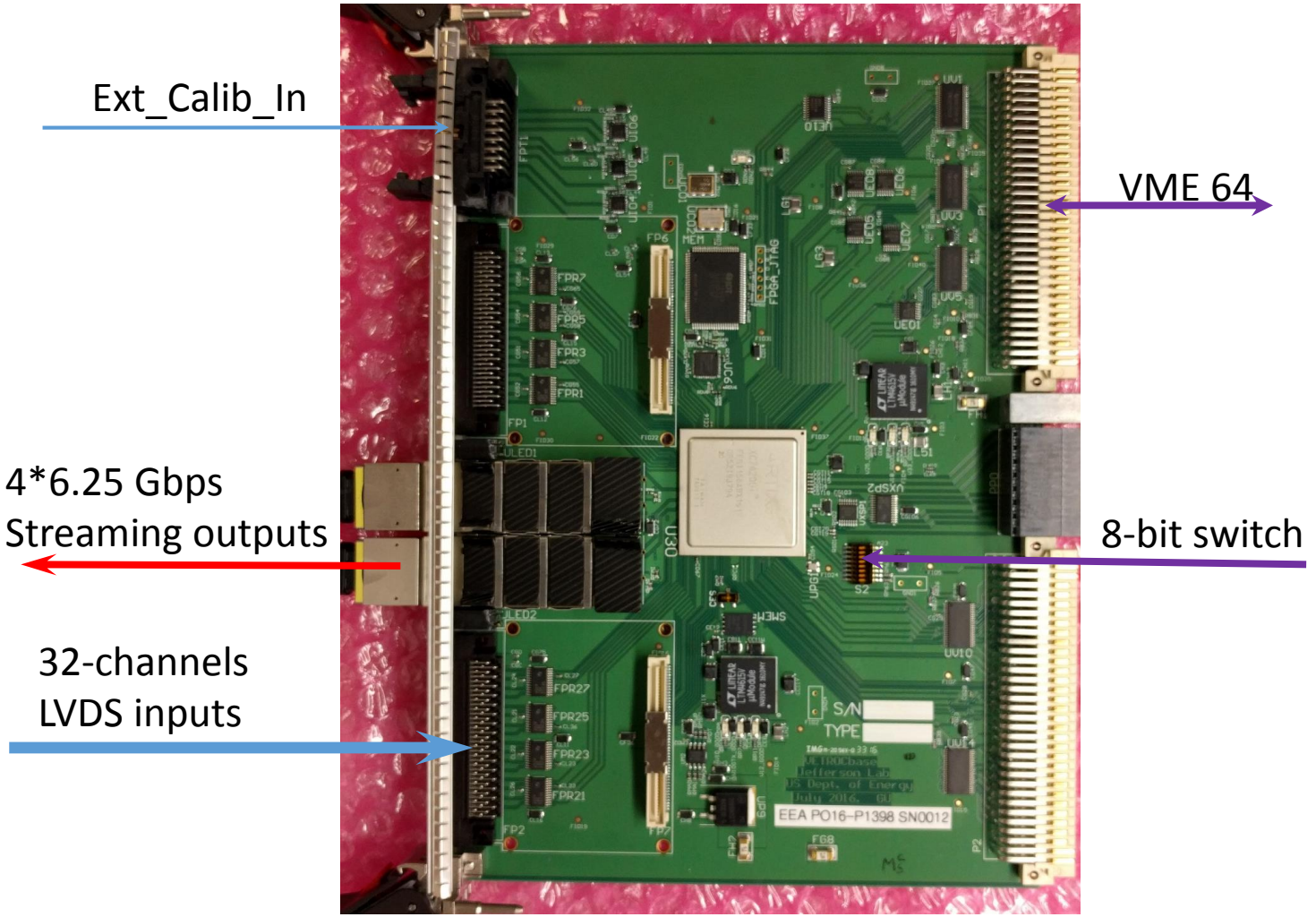
Streaming readout TDC (STDC)

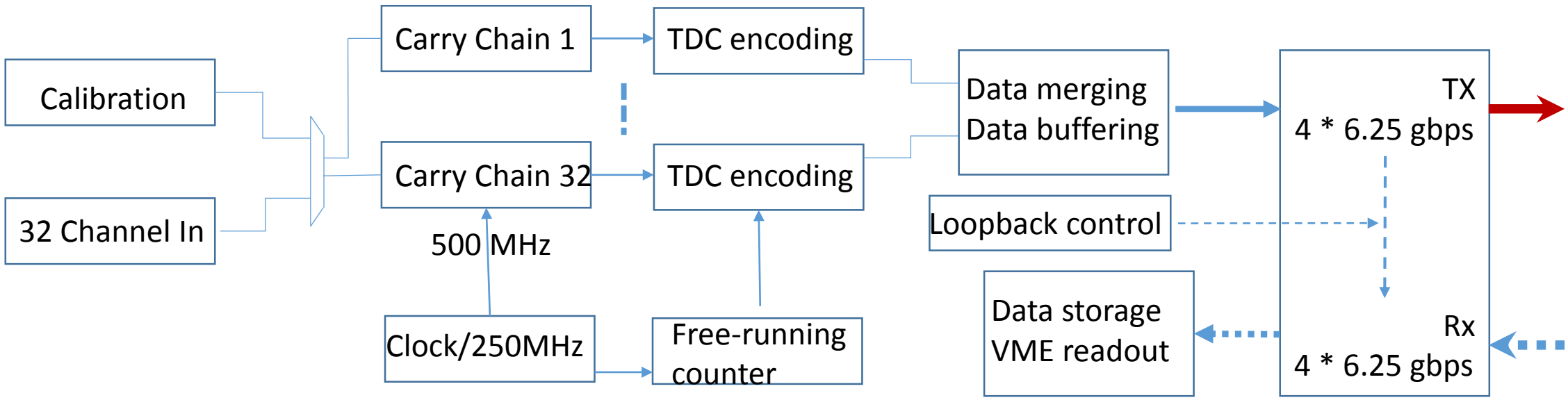
The Streaming Readout TDC (STDC) is based on the VETROC base board (PCB), with streaming readout TDC FPGA firmware.

Board features used by STDC:

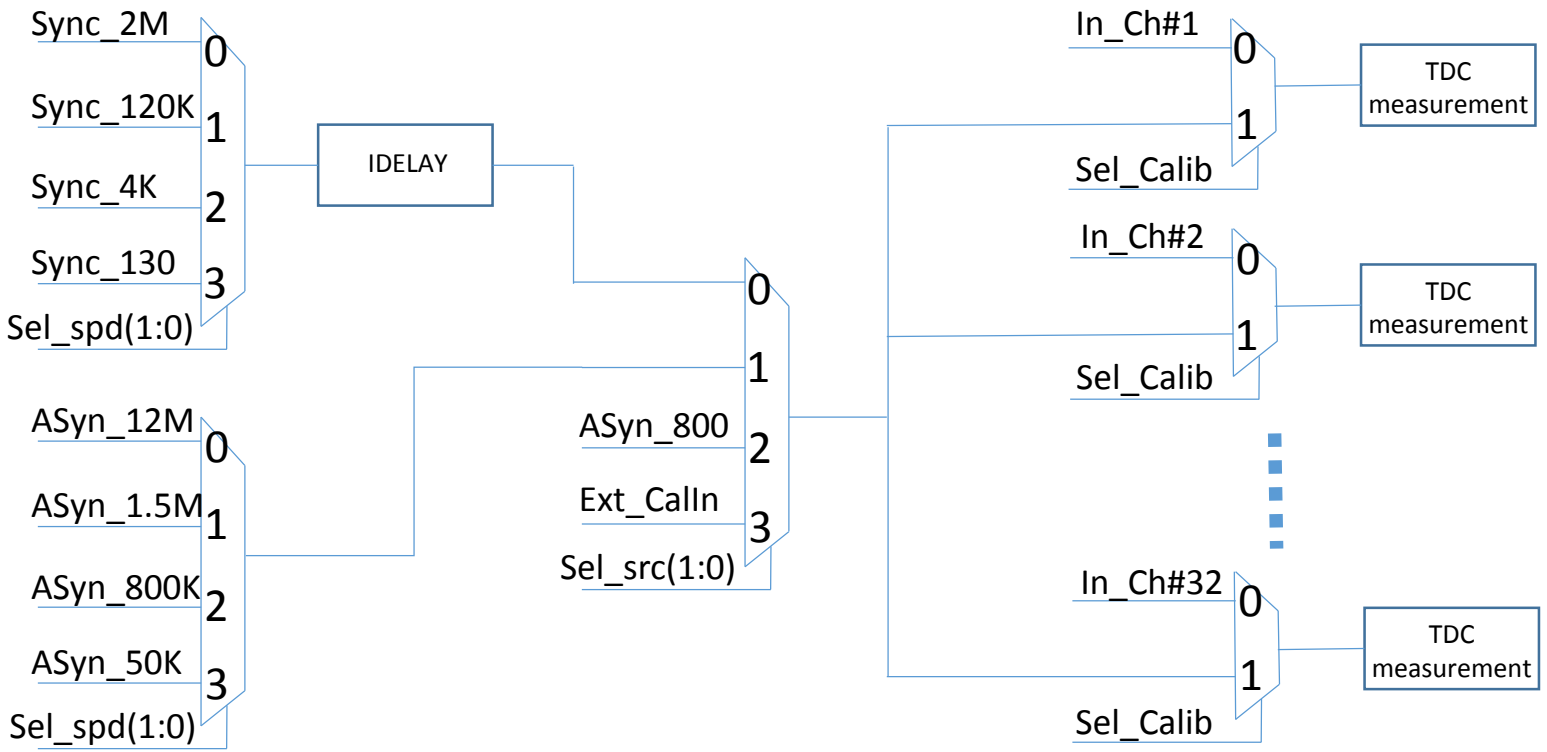
- Lower front panel connector: 32-channel LVDS inputs;
- Lower QSFP optic transceiver: 4 channels 6.25 gbps streaming TDC data output
- Top front panel connector pin#25/26: external calibration in;
- Backplane VME64, slow control; or, on-board 8-bit switch



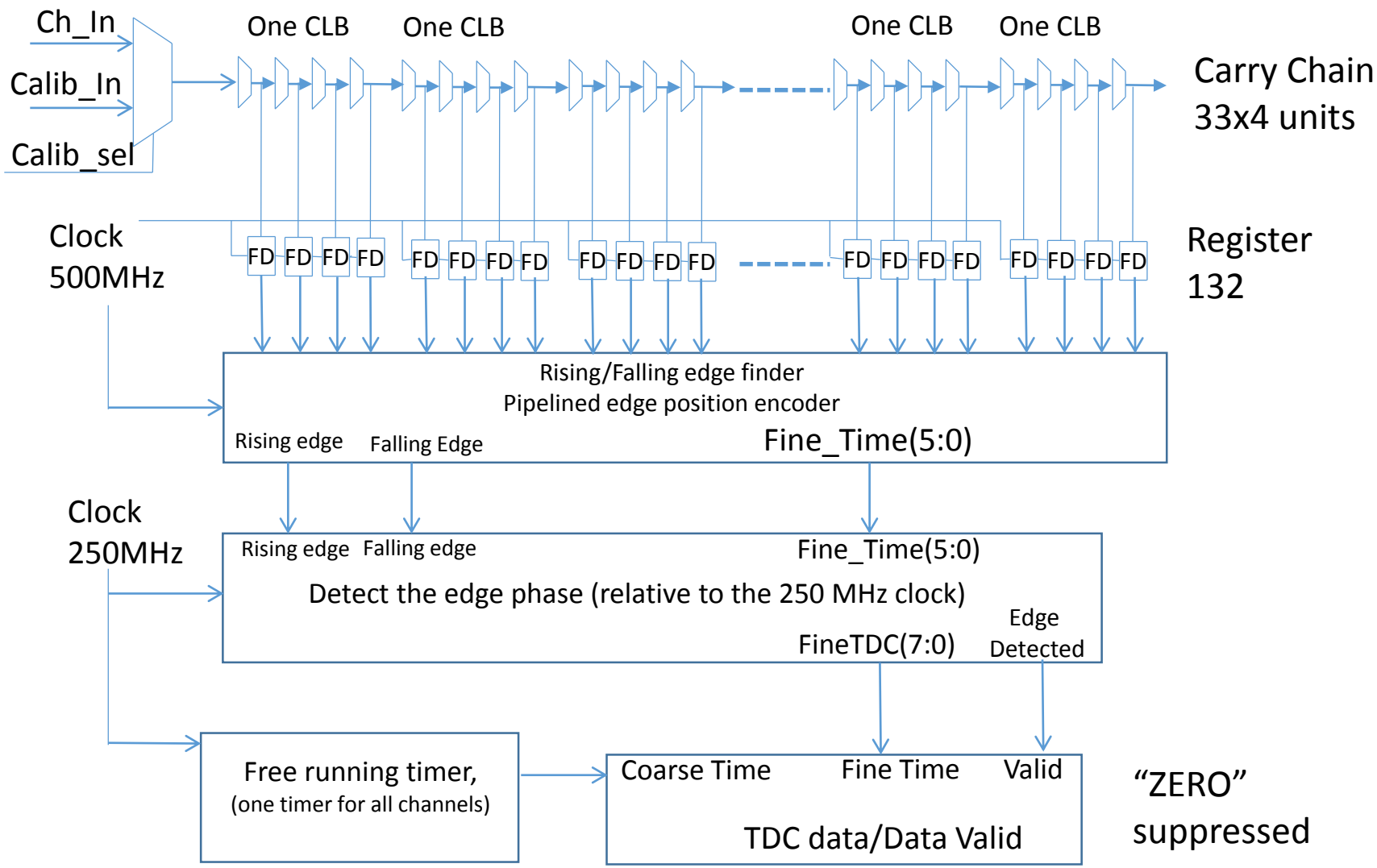
Functional Diagram



Calibration

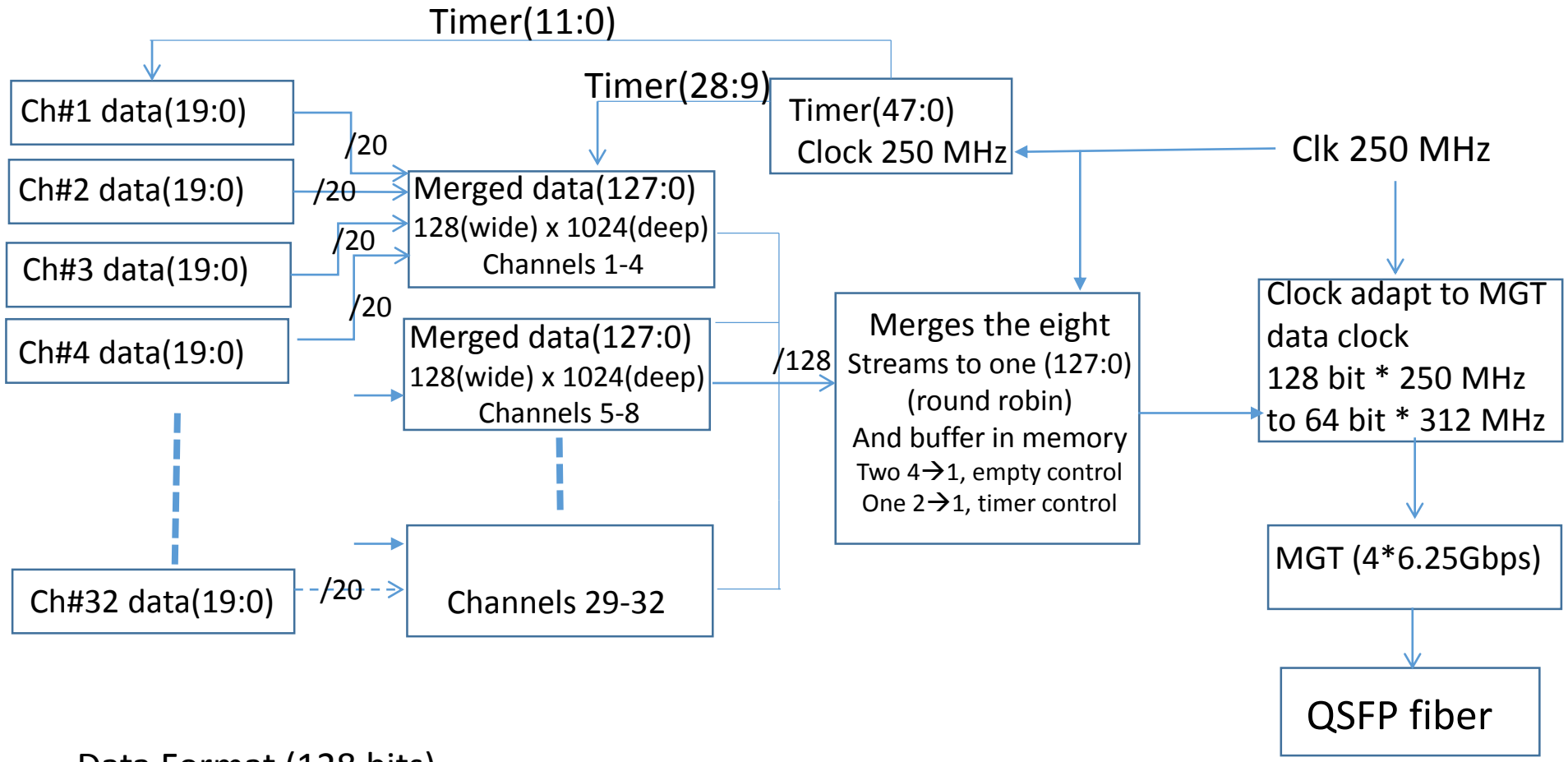


TDC encoding



*TDC data format: Bit(25:20): Channel#; Bit(19:8): Time in 4ns (250MHz)
Bit(7): Time in half of 4ns; Bit(6): Pulse edge type; Bit(5:0): time in ~35 ps;

Streaming output



Data Format (128 bits)

Bits (127-124) (123:104) (103:78) (77:52) (51:26) (25:20 : 19:8 : 7 : 6 : 5 : 0)

TYPE Timer Ch#A Ch#B Ch#C CH# Coarse_time Clk250 pulse Fine_time

Timer(28:9) 0-63 Time(11:0) edge edge ~40ps

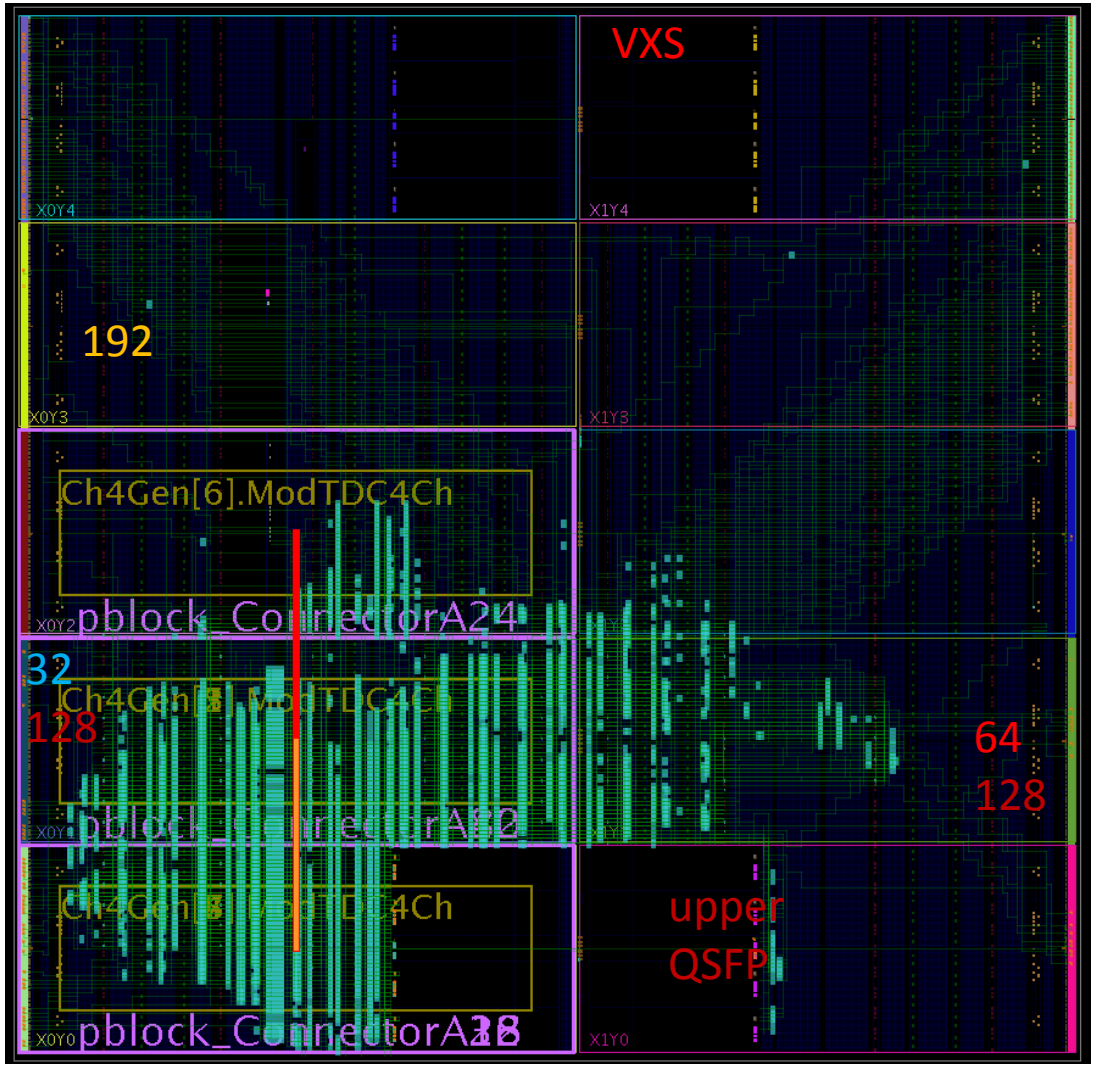
Depending on the TYPE, the bit(123:104) could also be the Timer(47:28) to extend the TDC range to more than ten days, or the TDC of the reference channel to sync multiple STDC boards.

Summary

- Streaming data rate: 2.5 Gbyte/second (4 * 6.25 gbps 8b/10b encoding);
- TDC data: ~4.5 Bytes/edge;
- TDC resolution: LSB ~35ps;
- TDC range: 36bit → ~8 seconds;
- Edge separation: <2.5ns;
- Channel counts: 32.
- Edge occupancy: 16 M/channel (average)

Other possibilities

- Increase channel counts from 32 to 64, to 128, or to 192 for low occupancy;
- Double the streaming data rate by adding the VXS output path;
- Increase the streaming data rate 50% by adding two channels of upper QSFP output path;
- TDC range increase to “days”;



STDC FPGA usage