Hall A DAQ meeting

April 6th 2015

Alexandre Camsonne

Agenda

- budget Compton (Bob / Alex / Dave)
- new BCM receiver / BCM calibration (Luke ?)
- BigBite DAQ status (Alexandre)
- silo file transfer errors (Bob / Ole ?)
- SoLID review outcome DAQ recommendations (JP / Alexandre)
- upcoming experiment preparation (GMp/DVCS, Ar ee'p, APEX) (Alexandre)
- SBS Fastbus status and plan (Dasuni ?)
- SBS trigger distribution scheme (Alexandre)
- SBS cerenkov trigger and readout using VETROC (Alexandre - same as what was presented at SBS meeting)

Budget Compton

- for integrating mode DAQ
- 1 ..... Gate Generator, 2 VME scalers, ... 19
- Spare V1495, spare V538A

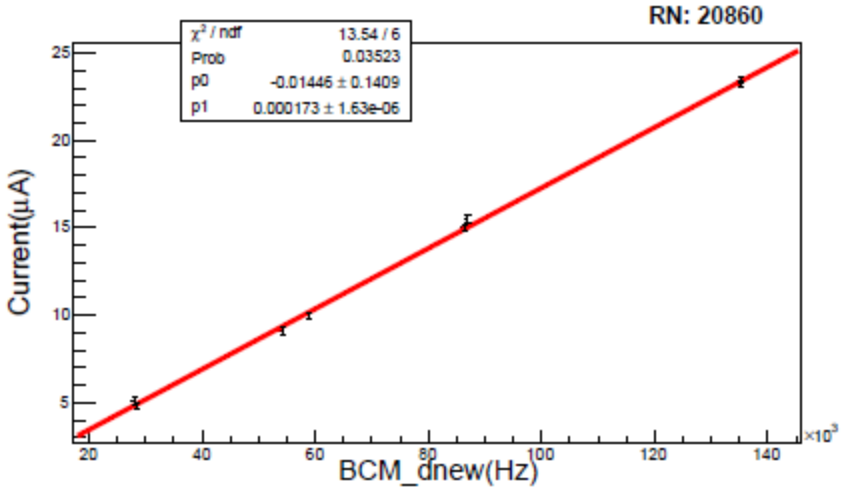
- for counting mode DAQ;
- assume we use existing FADC
- 2 ..... VXS Crate, cpu, TI 22

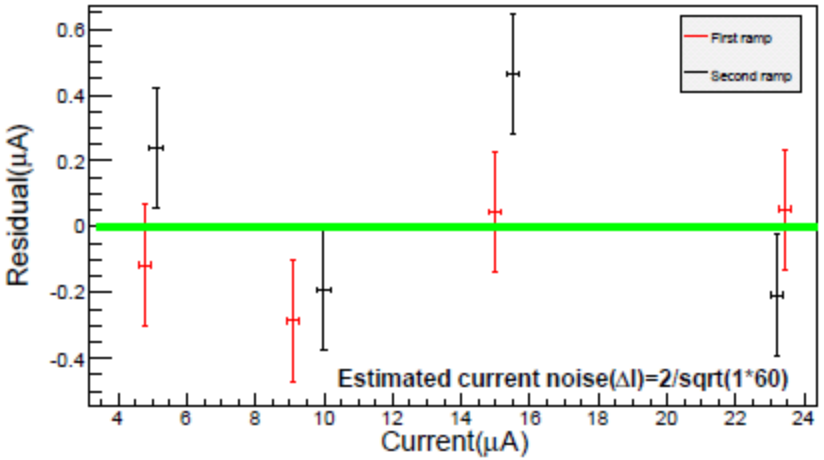
- 3 ..... Prototype VETROC 5
- (~ 1 year later need 5 production
- boards for a total of 40K$)

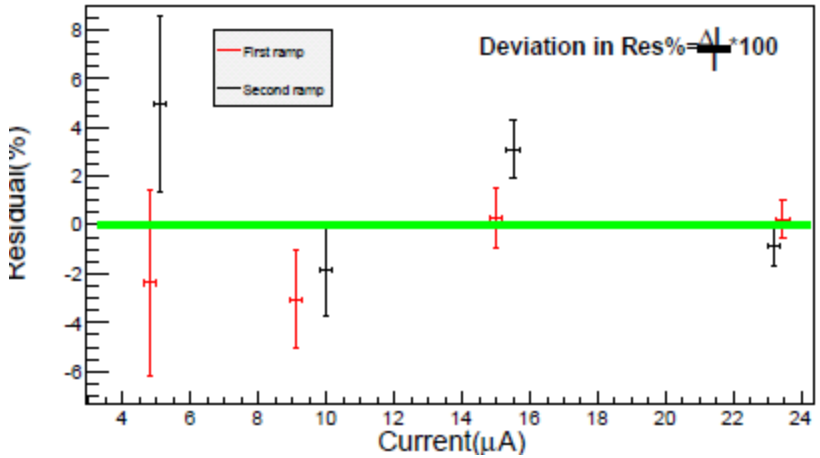
- To buy after the single plane recently installed
- is demonstrated to work
- 4 ..... Thick silicon for E-det 38

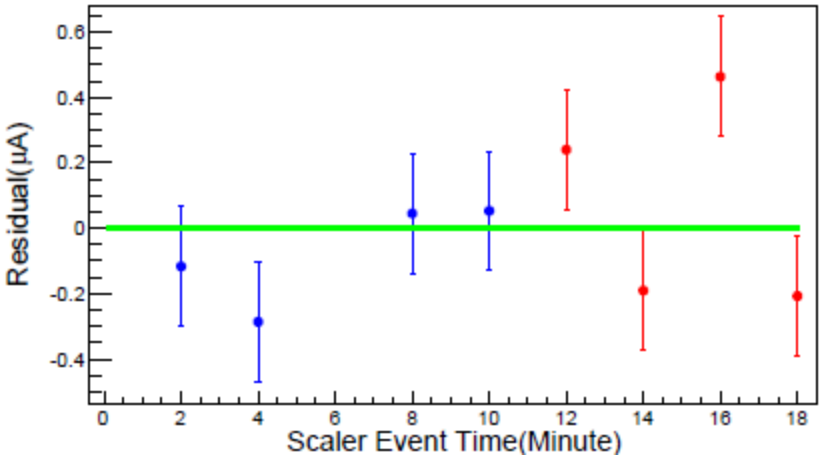
- 3 planes for 26K$
- 7 for 35K$
- 10 for 38K$ (preferred)

BCM new receiver down

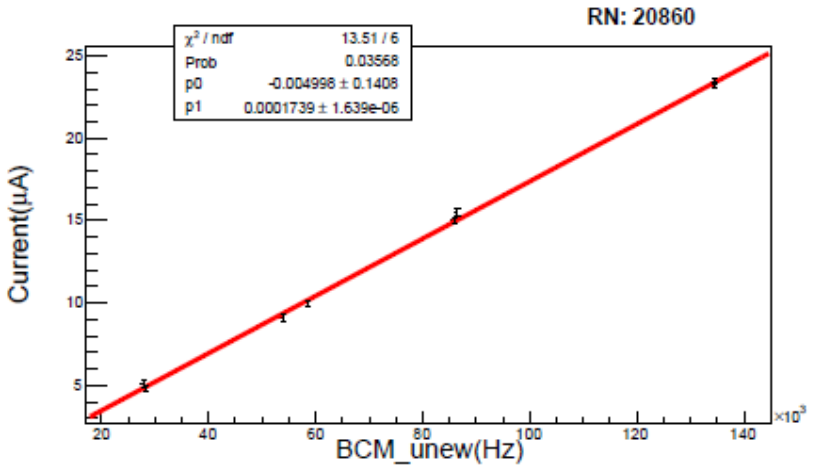


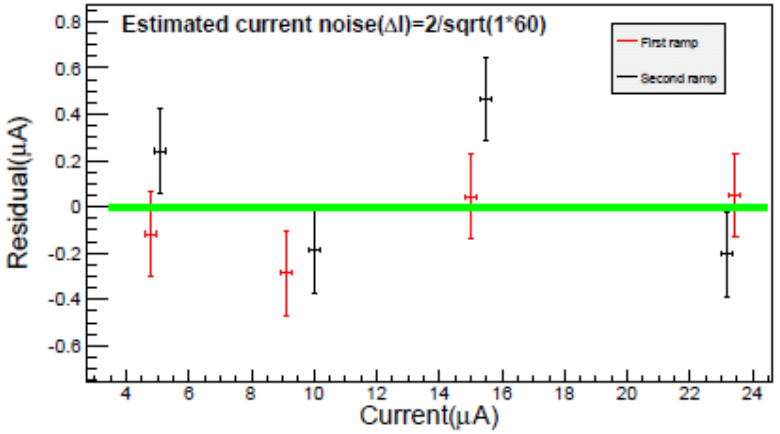


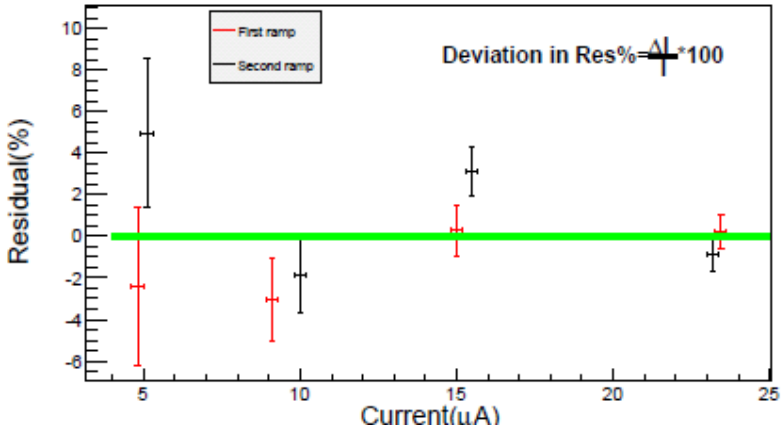


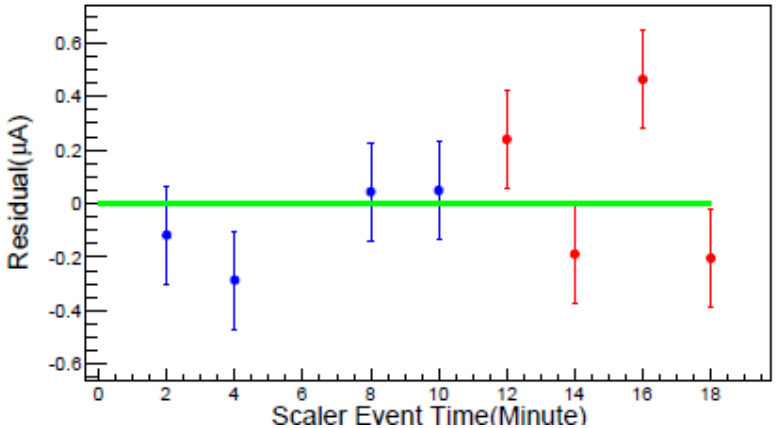


BCM new receiver up



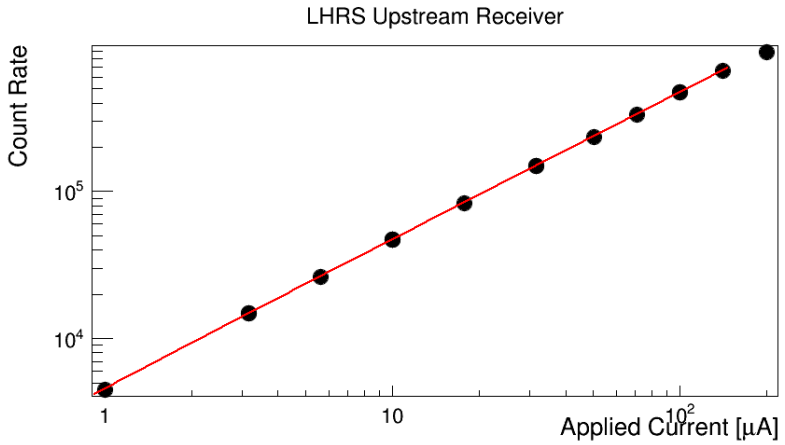


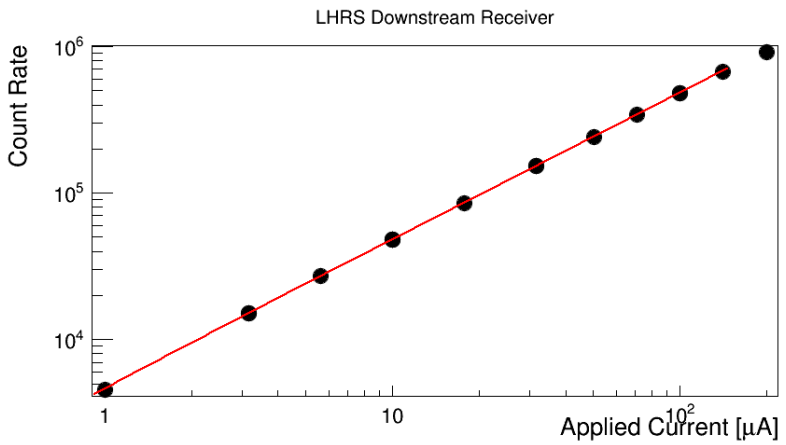


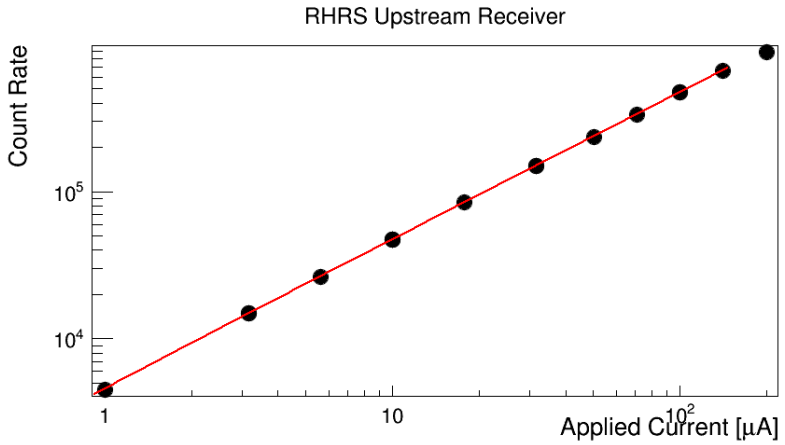


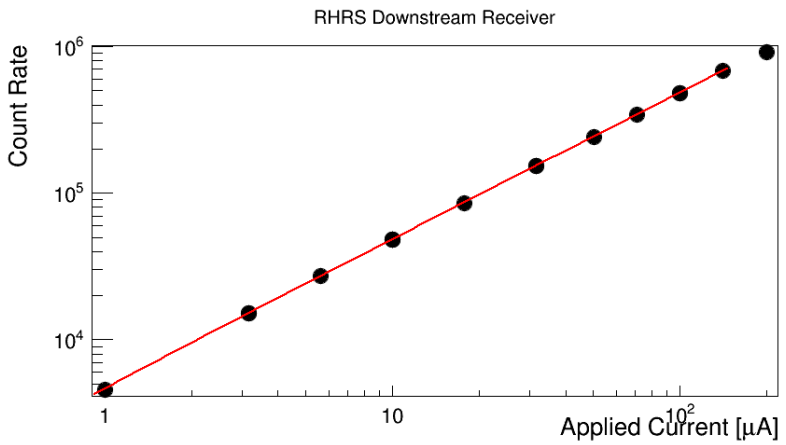
BCM new receiver RF source

- https://logbooks.jlab.org/entry/3322081

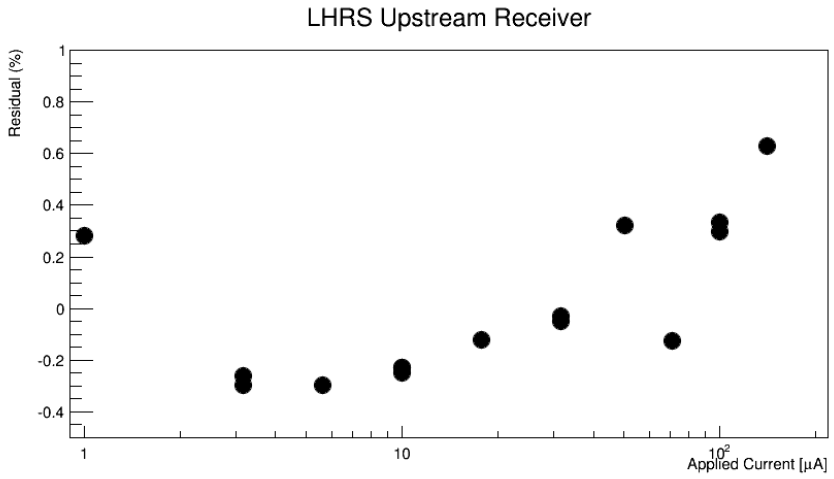


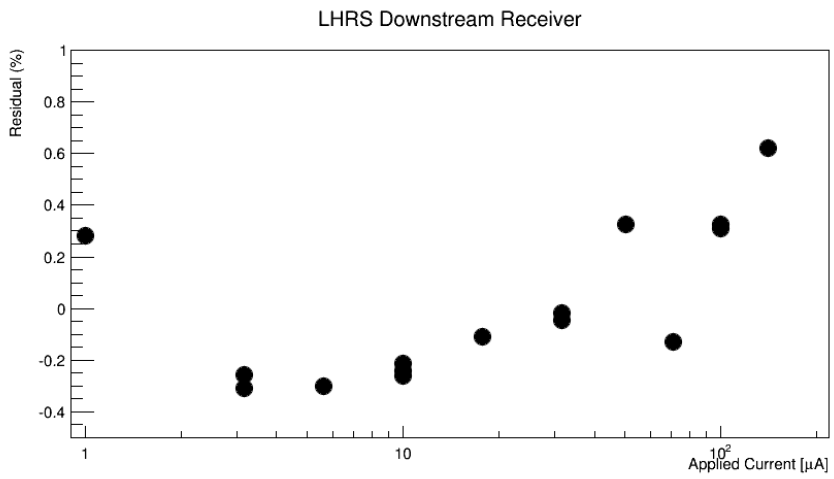


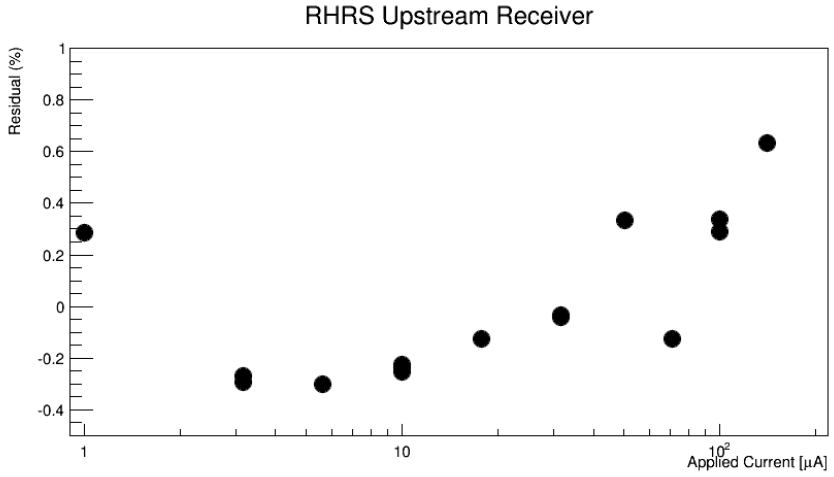


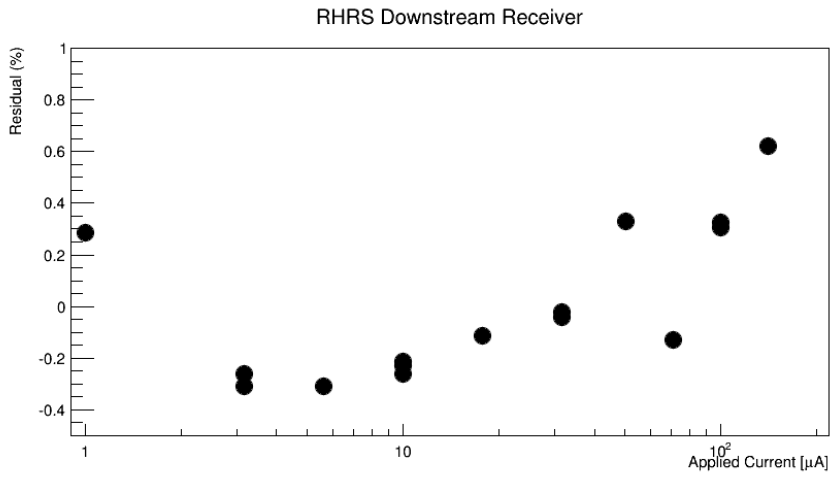


BCM new receiver RF source









Standard 1MHz BCM

- Offset from 1 MHz box about -15 mV
- Added linear fan
- x3 saturates at about 15 uA
- x10 saturates above 5 uA
- Need to check overlap of different gains
- Need low current data for calibration linearity check
- 3 options
  - Keep this way if x10,x3 and x1 cover whole range
  - Revert back no fan (should be ok 15 mV = 0.2 uA)
  - Get Musson to open the 1 MHz box and adjust offset

BigBite DAQ status

- 3 CPUs
- 1 crate trigger with new TI with 1877S
- 1 crate triggering from back with 1877S
- 1 crate bad 5V PS fixed
- Few bad slots will replace bin when tests done

- Need program V1495
- New computer would be handy

SoLID review DAQ

Observations

- SoLID plans to use much of the current 12-GeV electronics from Jefferson Lab.
- Plans for using the APV25 chip for GEM readout were presented.
- The Level 3 trigger was not described and no costs were included.
- The slow control needs of the experiment were not presented and no costs were included.
- The SoLID collaboration currently has some simulation and limited reconstruction.
- The manpower currently associated with software for SoLID is estimated to be 6 FTE-years. Numbers from both Hall-B/CLAS-12 and Hall-D/GlueX are in the range of 30 to 50 FTE-years.
- The data scale expected from SoLID is similar to that anticipated in Halls B and D, while that in the early Hall-A experiments have a much smaller data footprint.
- No plan for data handling was presented.
- Data storage needs for Monte Carlo simulations were not included.

Findings

- Consultation with appropriate people from the other halls would be useful to get a more accurate estimate of software needs, including manpower.
- Early exploration of the tools available at Jefferson Lab that can handle the data at the expected scale of SoLID will be crucial in minimizing the false starts in software development

SoLID review DAQ

Recommendations

- The plans for the High Level Trigger and the needs for slow control need to be worked out in detail and the implications for resources need to be evaluated.
- The implications of the need for these resources in the context of availability of resources at the laboratory need to be understood.
- Closer communication with the other JLab experiments and the JLab computing center is strongly encouraged.
- Having a functional simulation and reconstruction routines as soon as possible should be a high priority in the software effort. Such software will pay off many times over in experimental design and avoiding pitfalls.

SILO transfer errors

- A few files did not get transferred regularly
- Second script to check and resubmit : works fine

- Ole might have found the issue

Upcoming experiment

- Low energy runnning
  - Coincidence trigger for Ar (ee'p) ?
  - 1 DAQ for both HRS
  - Need Aerogel ?
  - Need efficiency trigger for proton

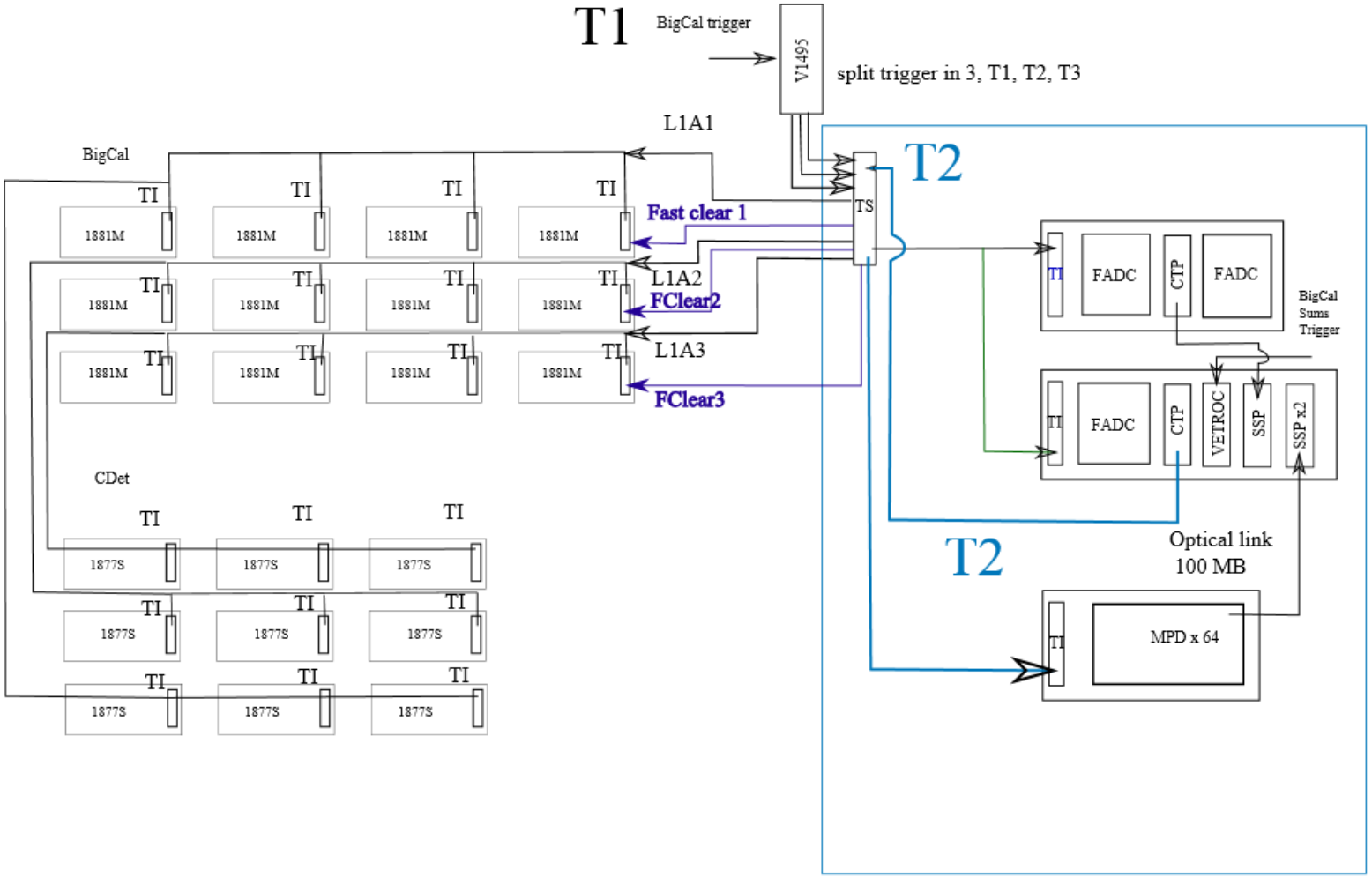
APEX plan

- Mostly same as Gmp
  - Coincidence trigger
  - FADC for SciFi detector : install VME64X crate in Right HRS (11 FADC for HCAL , need 8)
  - Need implement TDC sparsification
  - Include FPP ?

  - Optional : deploy new TI in parallel to standard TI to have event blocking option

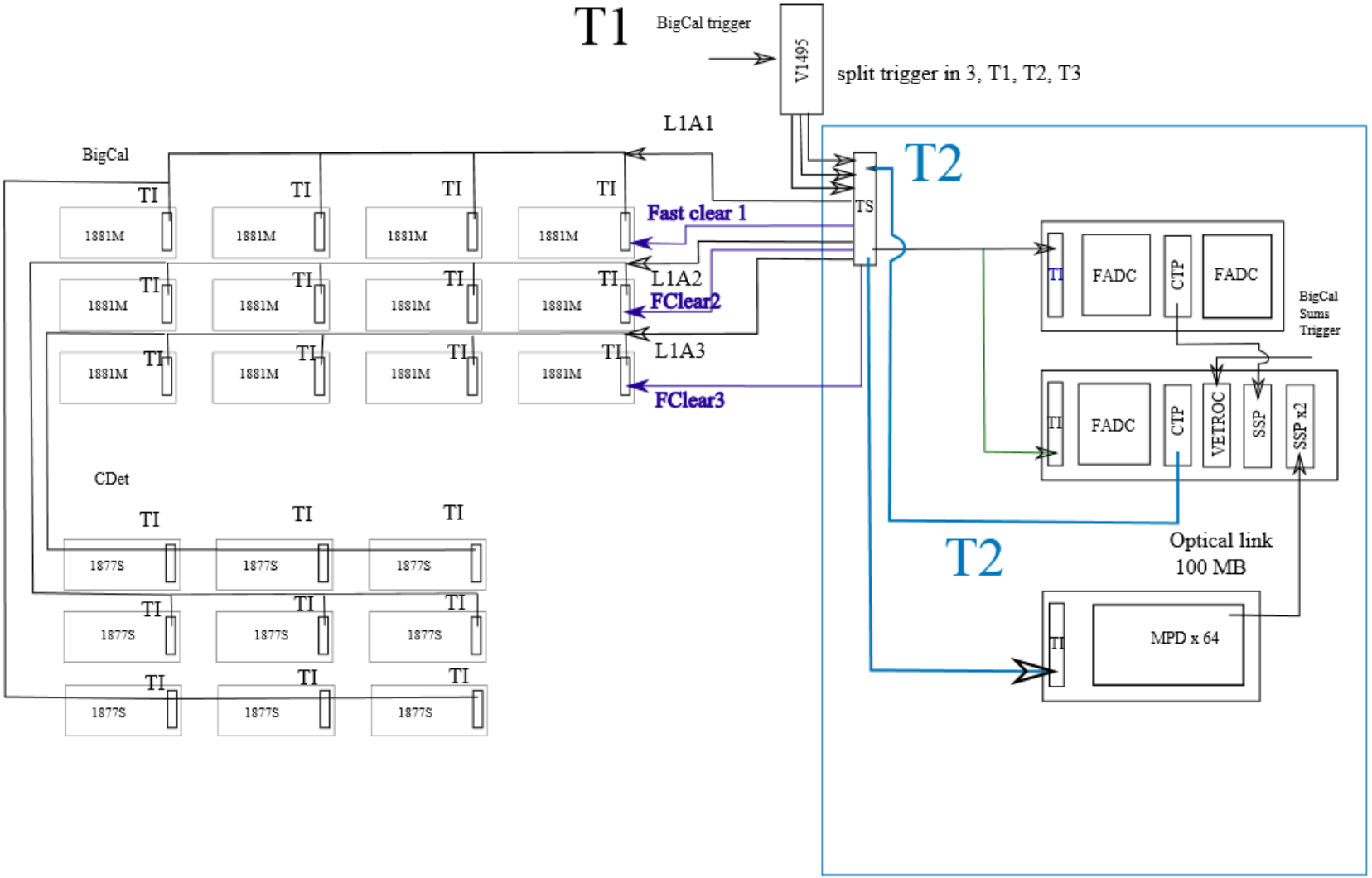
SBS Trigger scheme

- Presented to SBS review



SBS Trigger scheme

- New TI scheme



SBS Trigger scheme

- Use on TS for pipeline DAQ and Fastbus
- Use trigger partitioning (trigger part of DAQ depending on the trigger) feature of new TS
- Need new TI

- Advantage :
  - TS takes care of flipping (could try to get rid of V1495 and do in TS)
  - One data stream

SBS Cerenkov Trigger

SBS meeting
VETROC application for Cerenkov triggering

Alexandre Camsonne

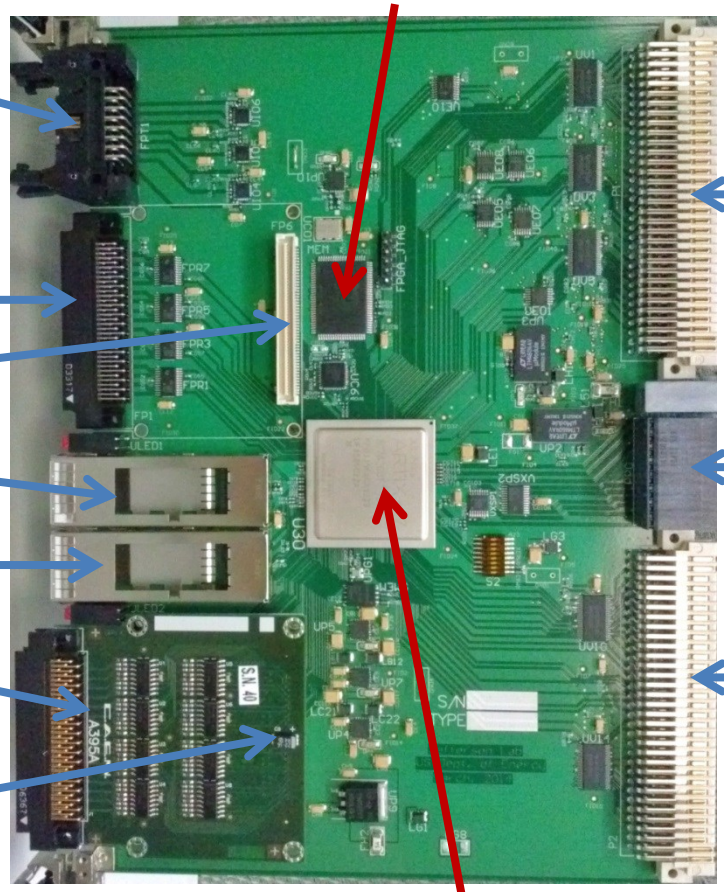
March 18th 2015

VETROC board

- Developped for Compton and SoLID MRPC
- 64 input + 8 input and 8 output
- Extension with mezannine to 128 channels (compatible with V1495 mezzanines)
- Optical link
- VXS link for triggering purpose
- Will try to develop high resolution TDC (possibly 25 ps resolution)
- Estimate price around 2.5 K$ for 64 channels and about 4 K$ for 128 channels

vXS fPGA-based Time to Digital Converter (vfTDC)

preliminary



Pipelined electronics

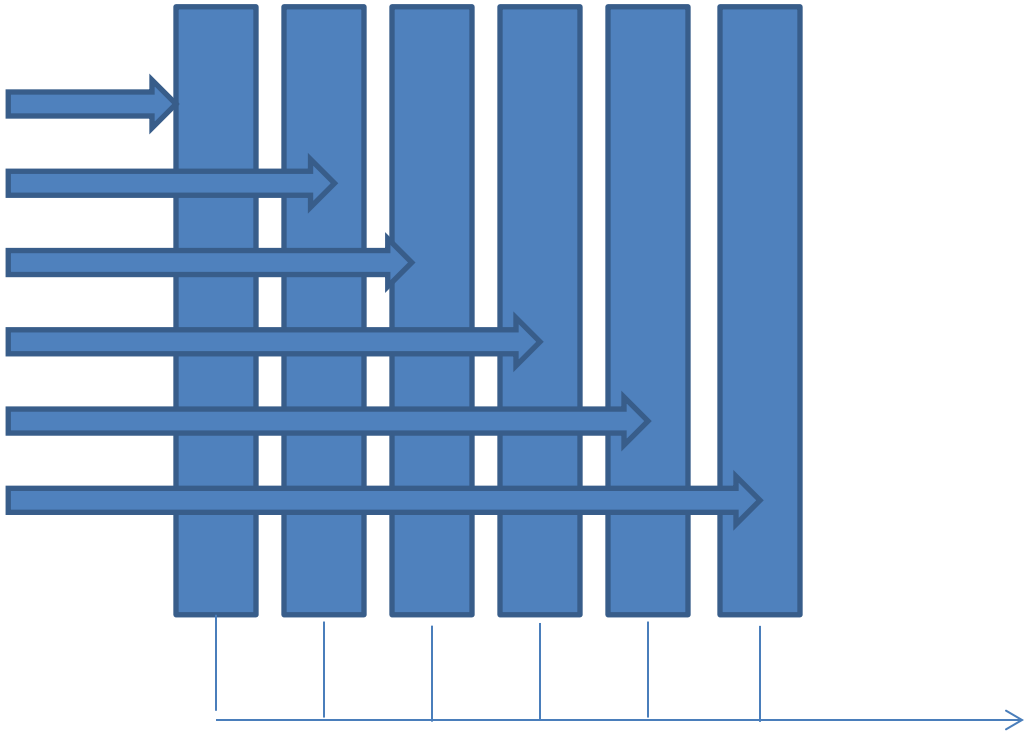
- 250 MHz sampling
- 4x 3 GBps Optical fiber link

- Can process hits every 4 ns or 8 ns

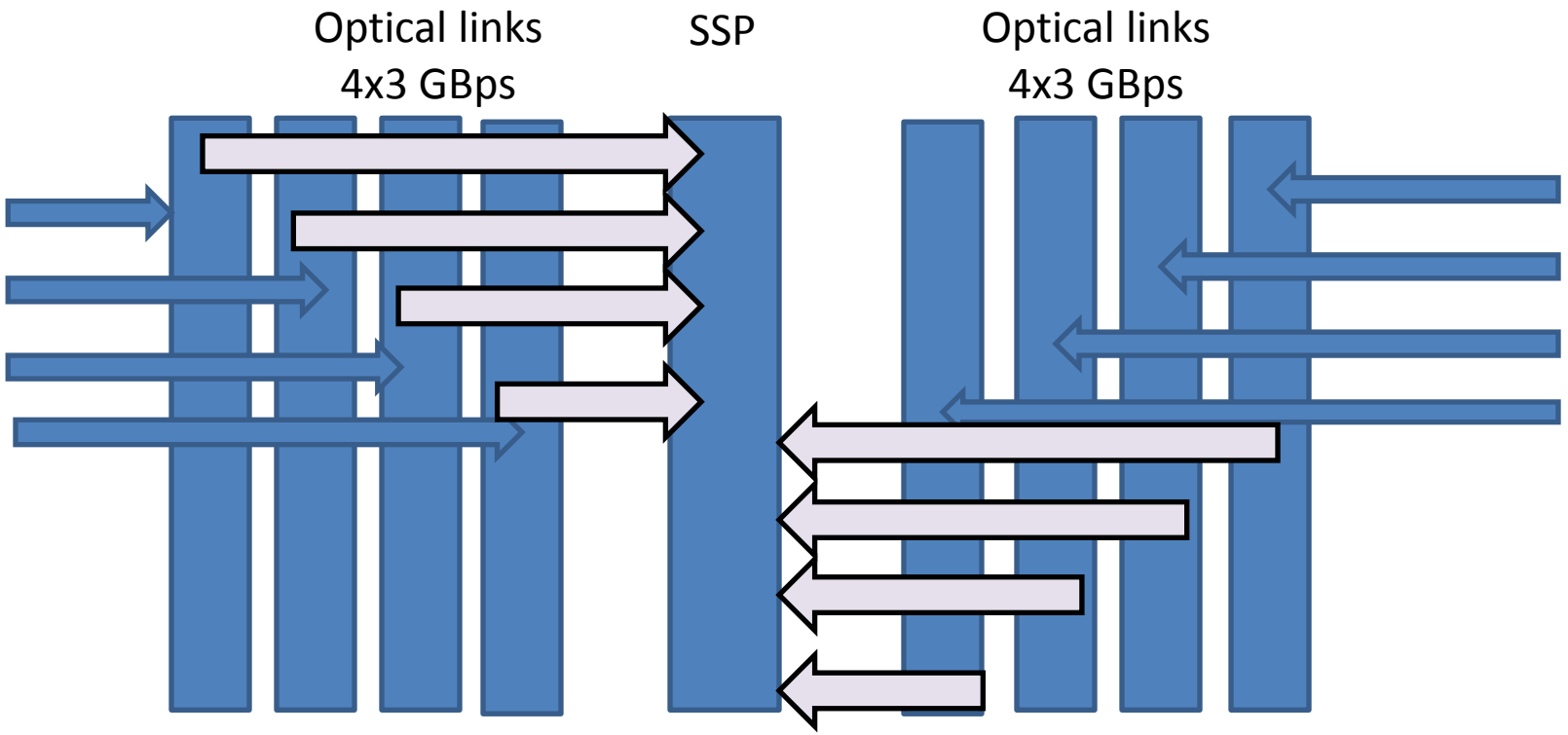
- Readout VME320 : 200 MB/s (5 times faster than Fastbus)

(1) Simple FPGA logic

- Fast, potentially no crate
- OR of all AND of a 3 channels

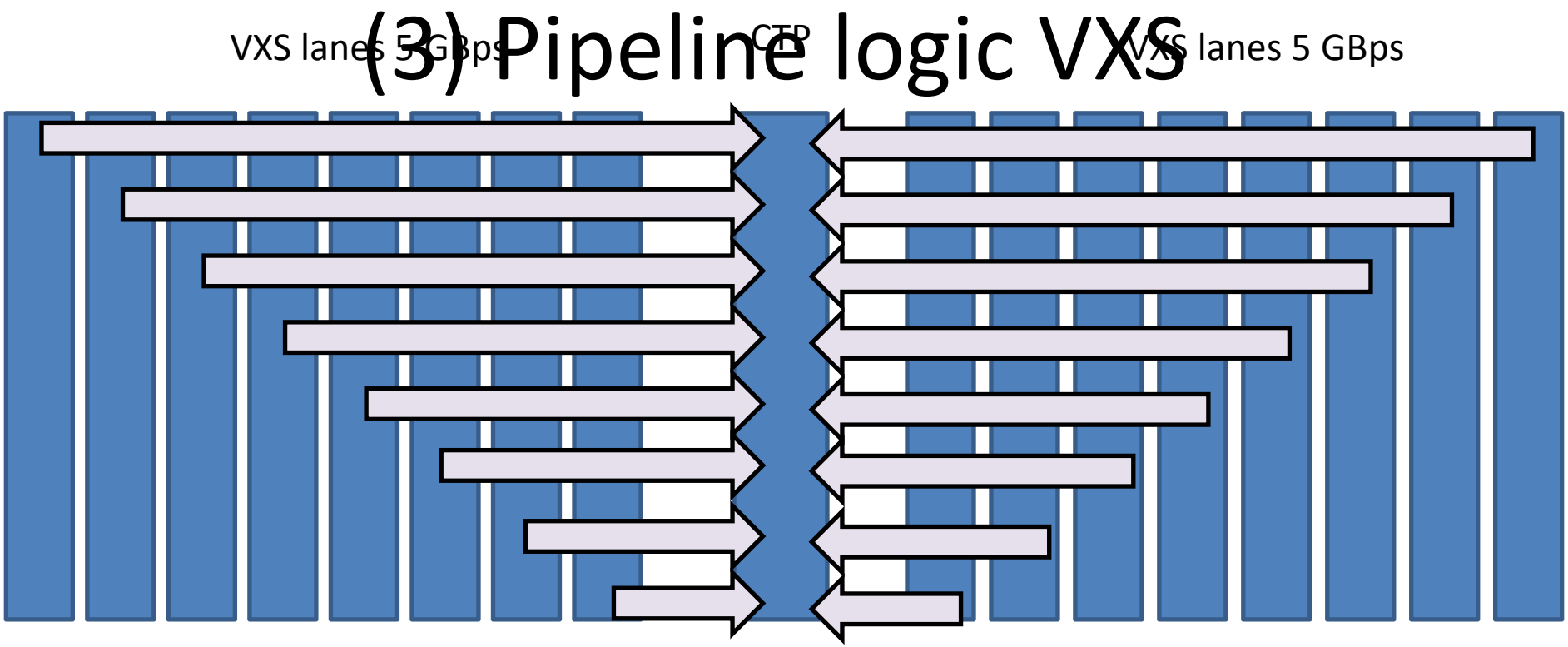


(2) Pipeline logic VME64X



Trigger latency :
250 ns (serialisation / deserialisation)
15 ns data
50 ns Processing
Trigger in about 350 ns for 1024 channels

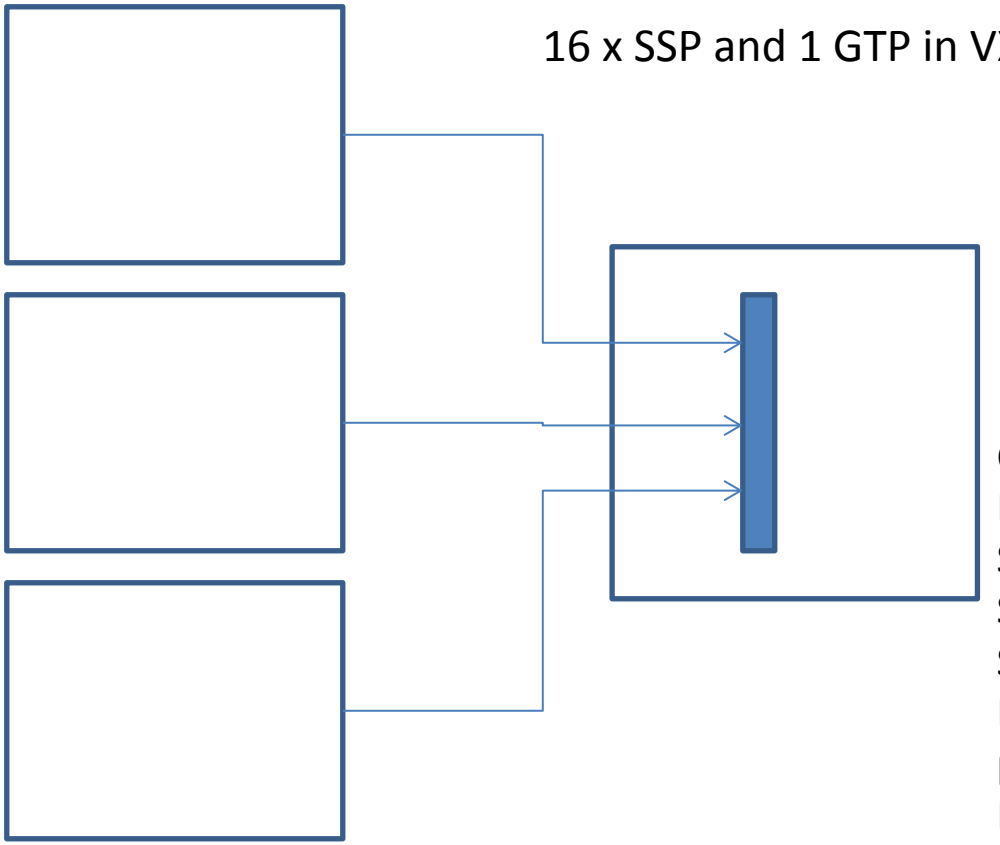
(3) Pipeline logic VXS



Up to 16 VETROC per VXS crates : 2048 channels

Trigger latency :
250 ns (serialisation / deserialisation)
15 ns data (128 bits per board)
50 ns Processing
Trigger in about 350 ns

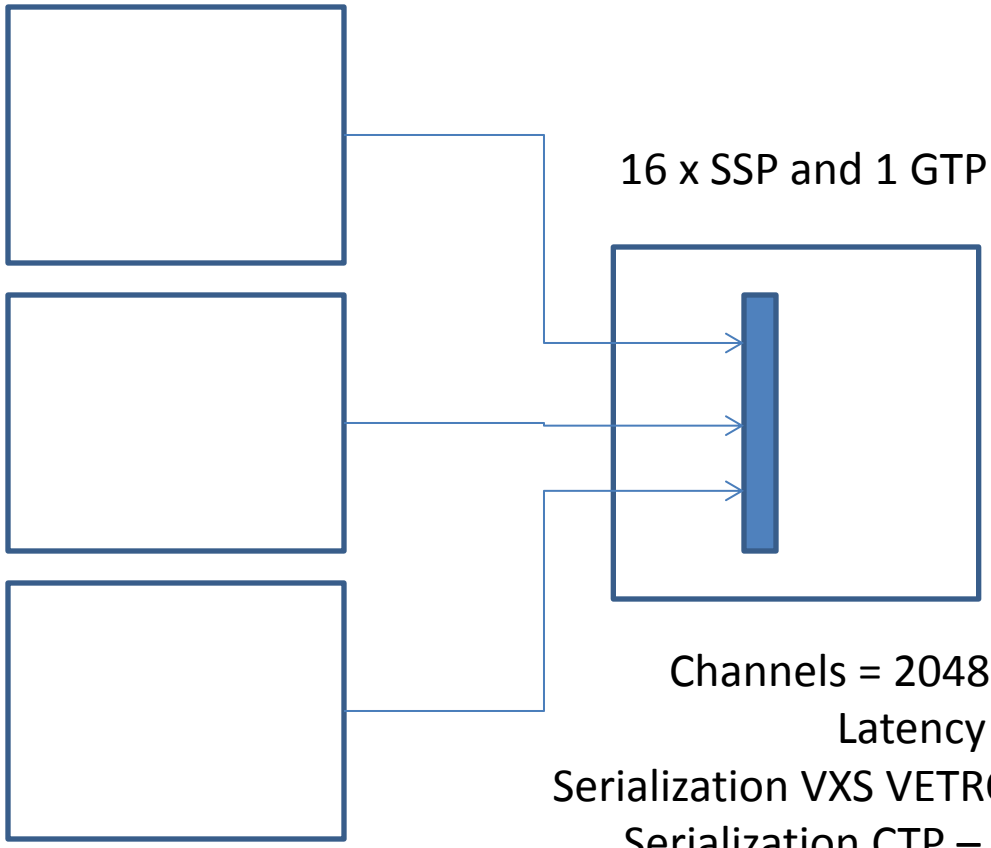
(4) Hybrid pipeline logic VXS



Channels = 2048 * crates
Latency
Serialization VXS VETROC-SSP 250 ns
Serialization SSP 250 ns
Serialization VXS SSP-GTP 250 ns
Data transfer = 2048 / 8 GBps = 256 ns per crate
Processing 500 ns
Trigger latency about 2 us for 2 crates

Up to 16*8=128 VETROC = 16384 channels

(5) Full fledge pipeline logic VXS



VETROC
VXS
Crates
16 VETROC
Per crate
=
2048

Up to 128 x 2048 channels
=
262,144

Channels = 2048 * crates
Latency
Serialization VXS VETROC-CTP 250 ns
Serialization CTP – SSP 250 ns
Serialization SSP-GTP 250 ns
Data transfer = 2048 / 8 GBps = 256 ns per crate
Processing 500 ns
Trigger latency about 2.3 us for 2 crates

Readout

- High resolution TDC available at readout stage (could be made available at trigger level but need redesign) : preliminary resolution 20 ps on 128 channels
- VME320 ：140 MB/s sustained
- Can fully take advantage of event blocking

GRINCH

- 550 PMT
- Option (2)
- 5 x VETROC = 5x4K$ =20 K$
- 1 VME64X crate = 8 K$
- 1 SSP = 5 K$
- 1 TI = 4 K$
- 1 CPU = 4 K$
- Total about 41 K$

RICH

- 2400 channels
- Option (4)
  - 1 VME64X crates = 8 K$ = 8 K$
  - 1 VXS crate = 15 K$
  - 2 CPU = 2 x 4 K$ =16 K$
  - 1 GTP = 6 K$
  - 2 TI = 2 x 3 K$ = 6 K$
  - 3 SSP = 3 x 5 K$ = 15 K$
  - 1 TD = 4 K$
  - 19 VETROC = 19 x 4 K$ = 76 K$
- Total = 146 K$

RICH

- 2400 channels
- Option (5)
  - 3 VXS crate = 3x 15 K$ = 45 K$
  - 2 CTP = 2 x 5 K$ = 10 K$
  - 3 CPU = 2 x 4 K$ =12 K$
  - 1 GTP = 6 K$
  - 3 TI = 2 x 3 K$ = 6 K$
  - 1 SSP = 5 K$
  - 19 VETROC = 19 x 4 K$ = 76 K$
- Total = 160 K$

RICH triggers

- Have all PMTs every 4 ns
  - Clustering
  - Ring ?
- If redesign of firmware logic to have high resolution at L1
  - Could have time over threshold and have amplitude at L1
  - Cut on single PMT amplitude
  - Threshold on digital sum all PMTs
  - Threshold on digital sum on ring or clusters

Conclusion

- VETROC can form prompt trigger and do readout
- Pipeline logic can be used for more complicated triggers (more latency around 300 ns) might be still fast enough for L1A within a crate, can be used for L2 with HCAL
- Cost ranges from
- High resolution readout developed 25 ps resolution
- Might be able to have high resolution at trigger level with investment