# Status of the Flash ADC Installation in Hall A

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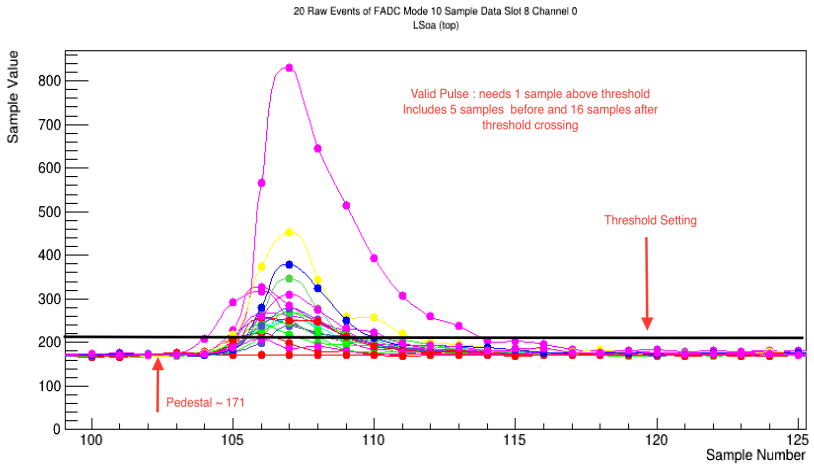
# Overview

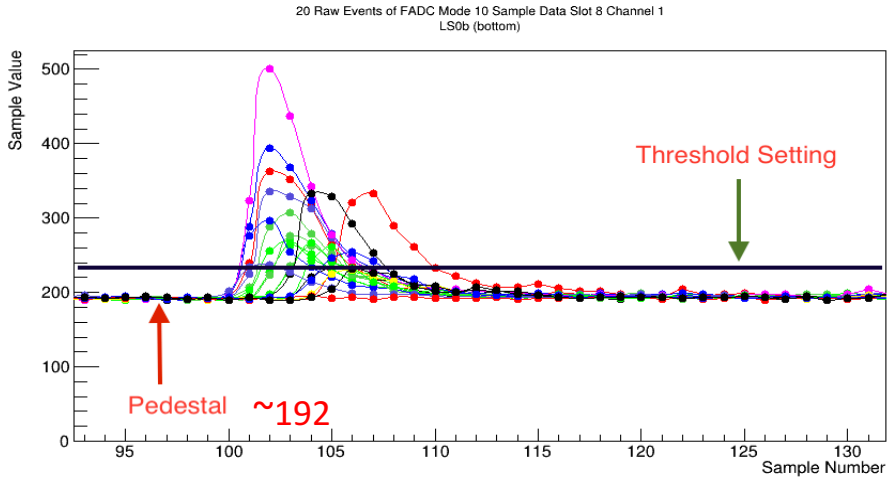
- Proposed to install 3 Flash ADCs in both LHRS & RHRS
  - Large pedestals in Cerenkov & Calorimeters due to delay cables
- Move S0, S2m, & Cerenkov to FADCs (44 channels)
  - Replace “bad” delay cables in calorimeter with those from S0, S2m, or Cerenkov

# Status

- All boards have been updated to the newest firmware : 0x0C0D
- Updated /modified readout lists
- Both arms in Block Readout mode
- Created coda configurations including FADC crates working on both LRHS and RHRS
- Taking cosmic data in LHRS & RHRS to confirm performance

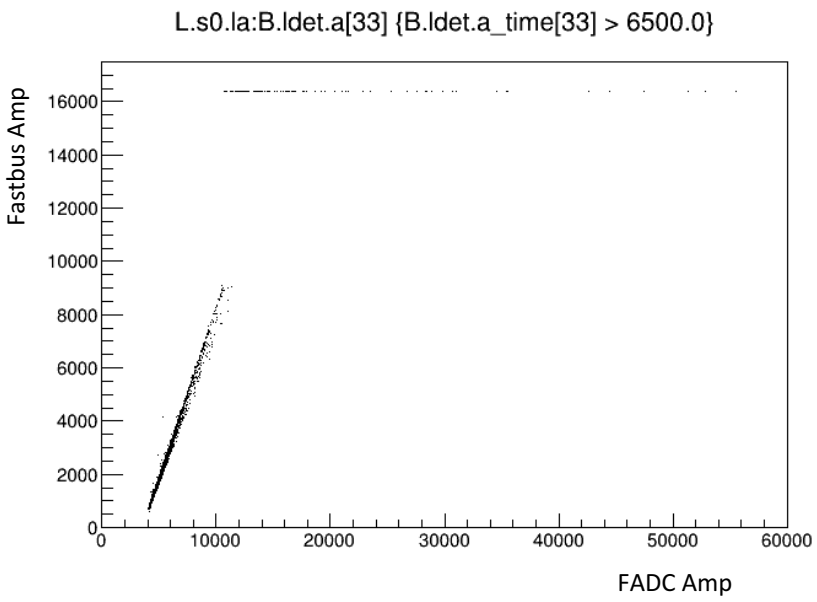
# S0 in LHRS


20 Raw Events of FADC Mode 10 Sample Data Slot 8 Channel 0
LSoa (top)
Sample Value
Sample Number
Valid Pulse : needs 1 sample above threshold
Includes 5 samples before and 16 samples after
threshold crossing
Threshold Setting
Pedestal ~ 171

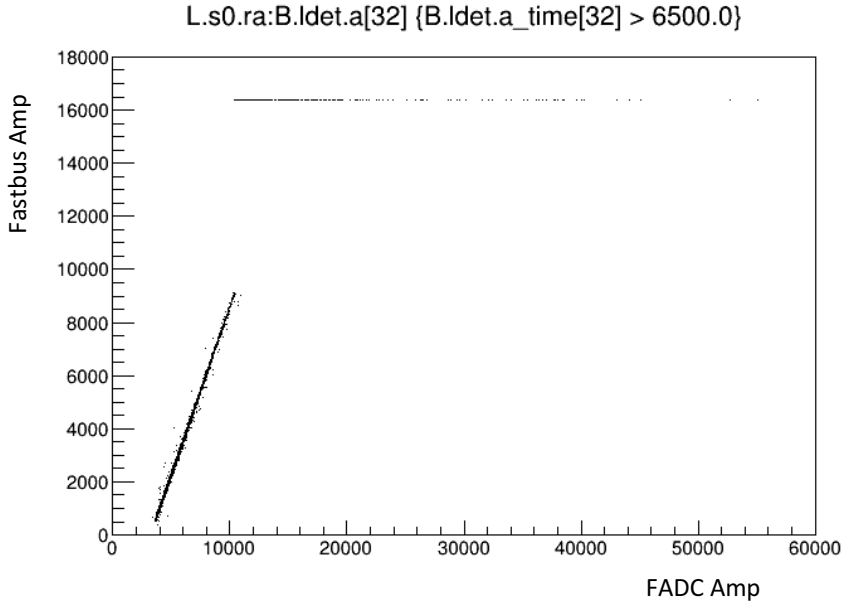

20 Raw Events of FADC Mode 10 Sample Data Slot 8 Channel 1
LS0b (bottom)
Sample Value
Sample Number
Threshold Setting
Pedestal ~192

# LHRS
# Fastbus Amp vs. FADC Amp

S0 top

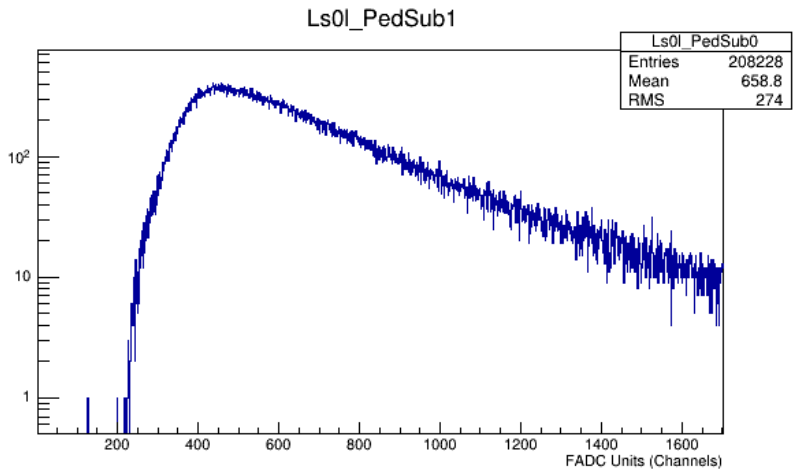



S0 bottom

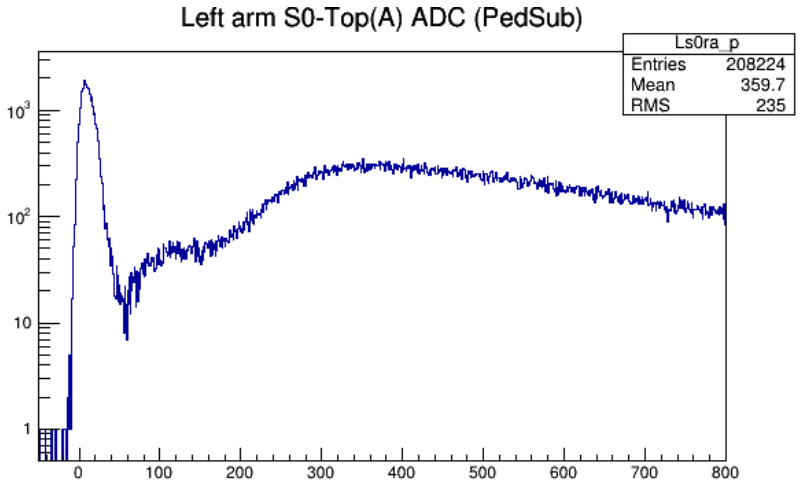


# LHRS : S0 (top)

Flash ADC

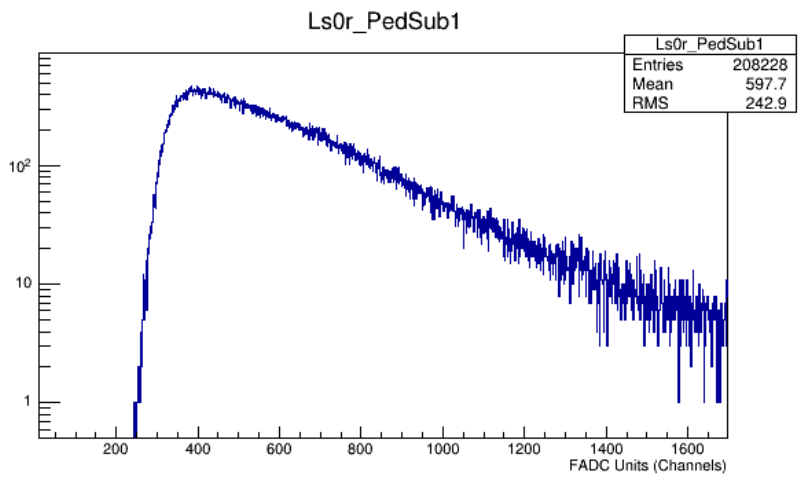



Fastbus ADC

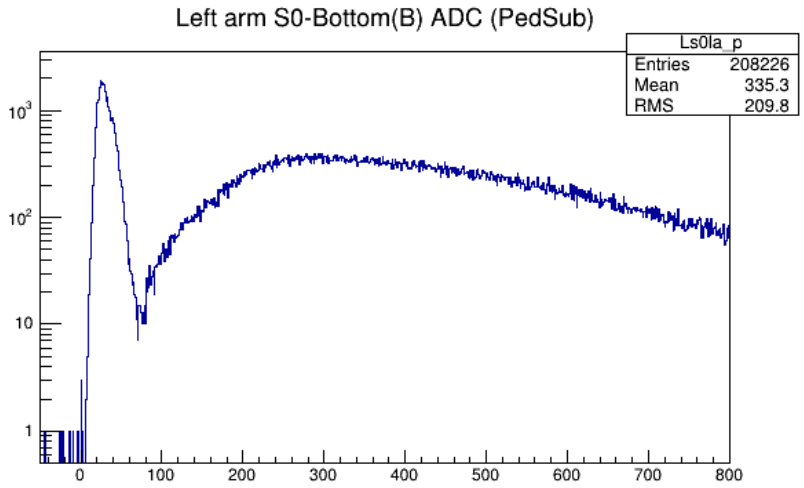


# LHRS : S0 (bottom)

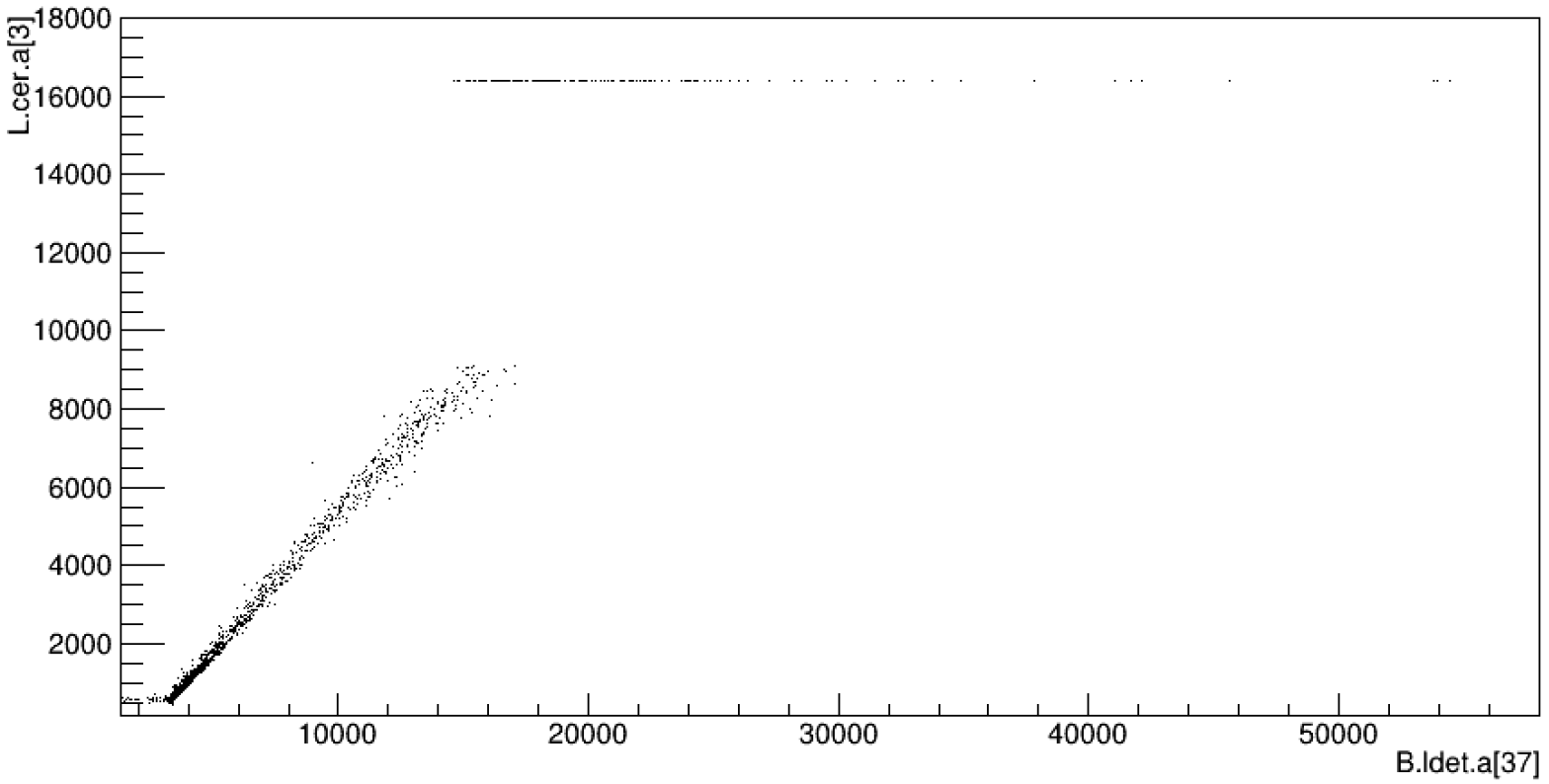
Flash ADC




Fastbus ADC

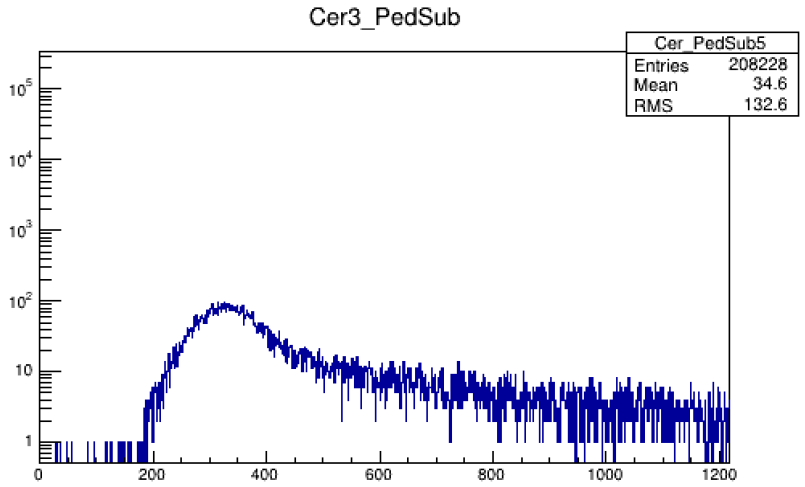


# LHRS Cerenkov : Channel 3

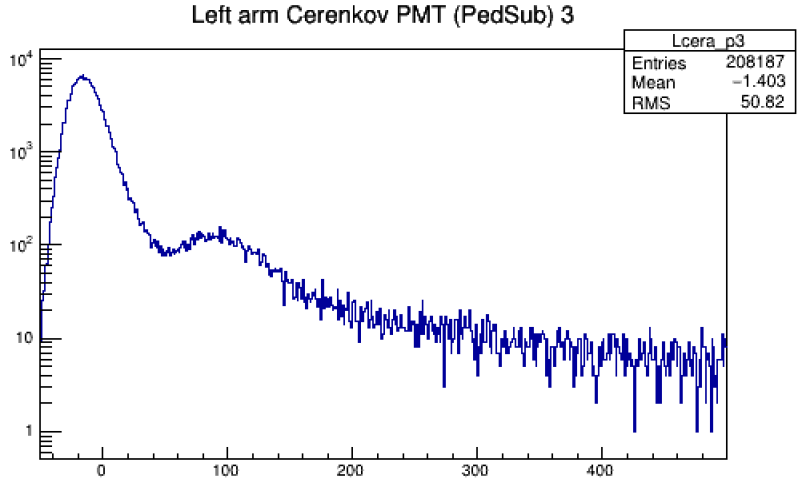


# Cherenkov

**FADC**




**Fastbus**



# Moving Forward…

- Working on new FADC Cerenkov and Scintillator classes for replay
- Include busy signal from SD board (?)
  - Confirm busy signal is/can being generated
- Add FADCs to Fastbus TS branch (currently on separate branch)
  - Needs to be done for coincidence experiment
- Reduce / optimize Latency and Window
- Continue taking cosmic data

# Aknowledgements

Alexandre Camsonne, Ed Jastrzembski, Robert Michaels, & Bryan Moffit

# Thanks

Suggestions / Questions ?