SAMPA Test Stand

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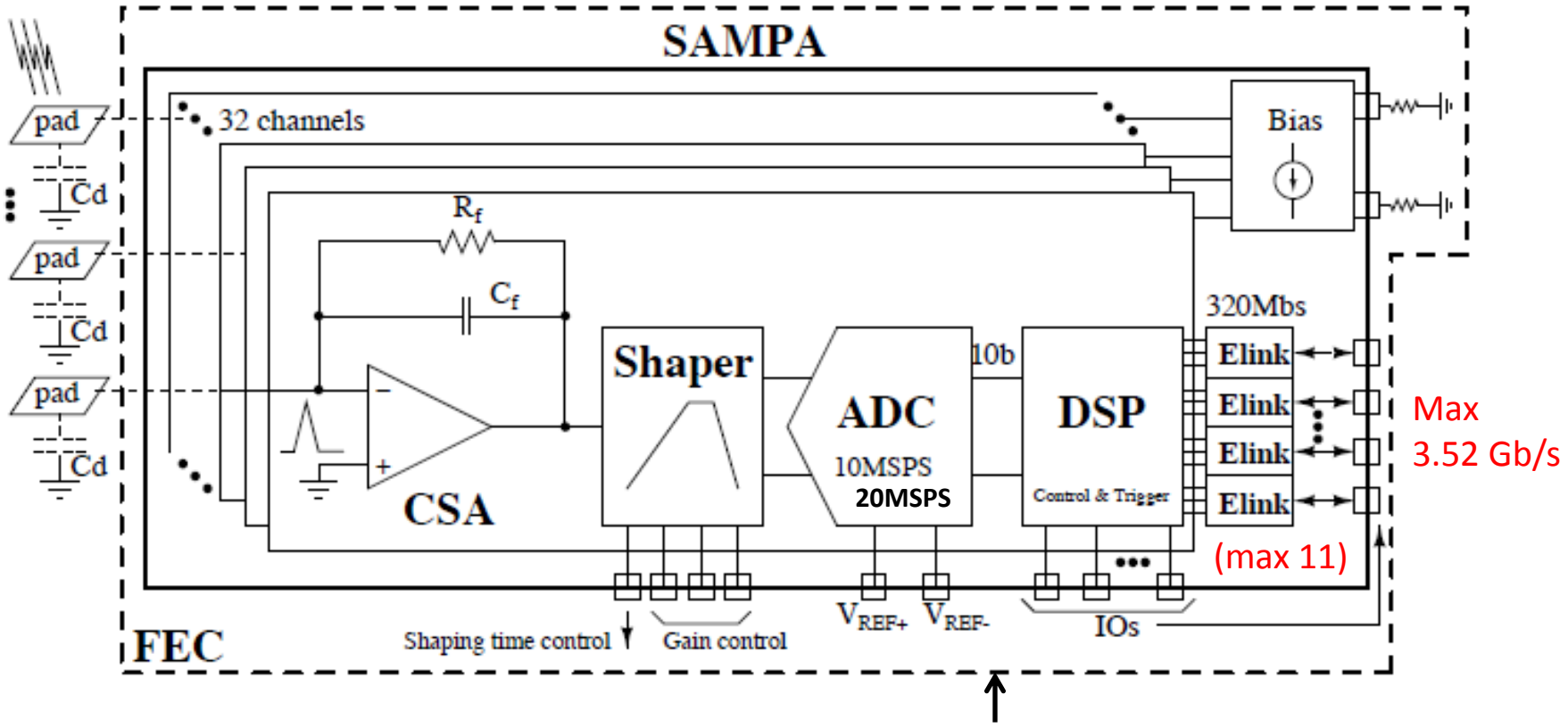
Jefferson Lab DAQ Group – 9/28/18

“SAMPA” - nickname for the city of São Paulo, Brazil

- New ASIC for the ALICE TPC and Muon Chamber (MCH) upgrades
- Combines functions of the **PASA** (analog) and **ALTRO** (digital) chips currently being used
- Design effort led by University of São Paulo, Brazil
- Chosen for TPC readout by sPHENIX and STAR upgrade at RHIC
- ALICE alone > 50,000 chips (1.5 M channels)
- All plan to use **continuous readout mode** for their TPCs

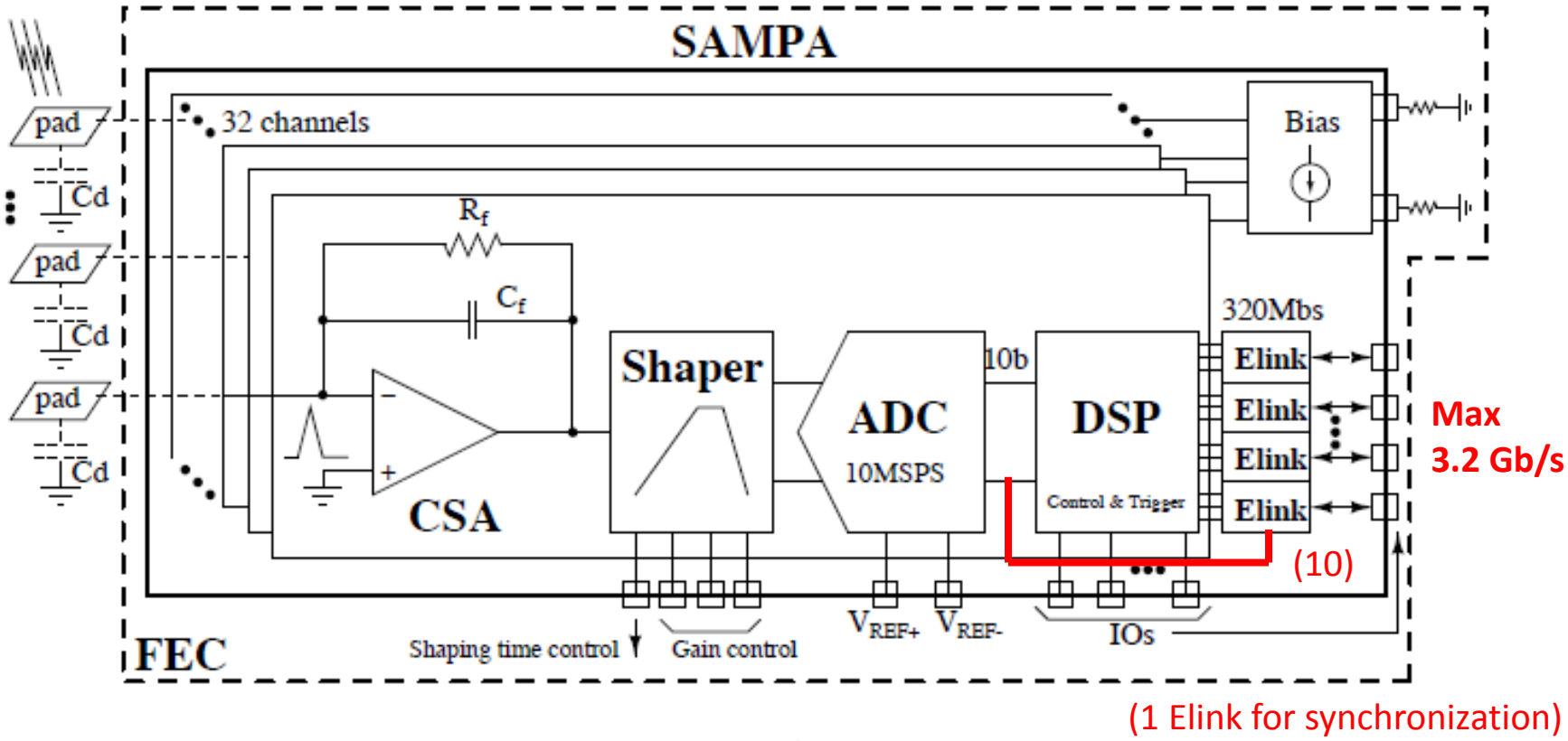
SAMPA Block Diagram



Raw data rate (10MHz) = 32ch x 10b x 10M/s = 3.2Gb/s

(20MHz) = 6.4Gb/s

SAMPA Block Diagram



Direct Mode – bypass DSP

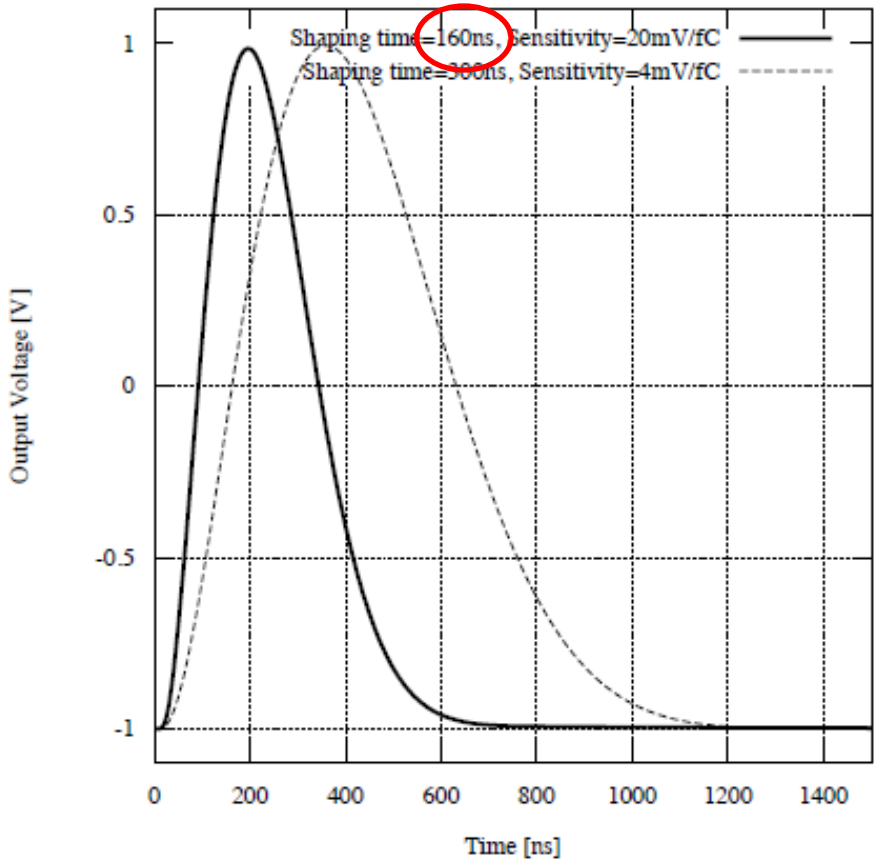
(Raw data rate (10MHz) = 3.2Gb/s = MAX output of chip)

Functional Blocks

- Charge Sensitive Amplifier (CSA)
  - Integrates and amplifies short current pulse
  - Output is a Voltage signal with amplitude proportional to the total charge Q
  - Tail of Voltage pulse is long (T = Rf*Cf)
  - Vulnerable to pile-up unless followed by a shaping filter

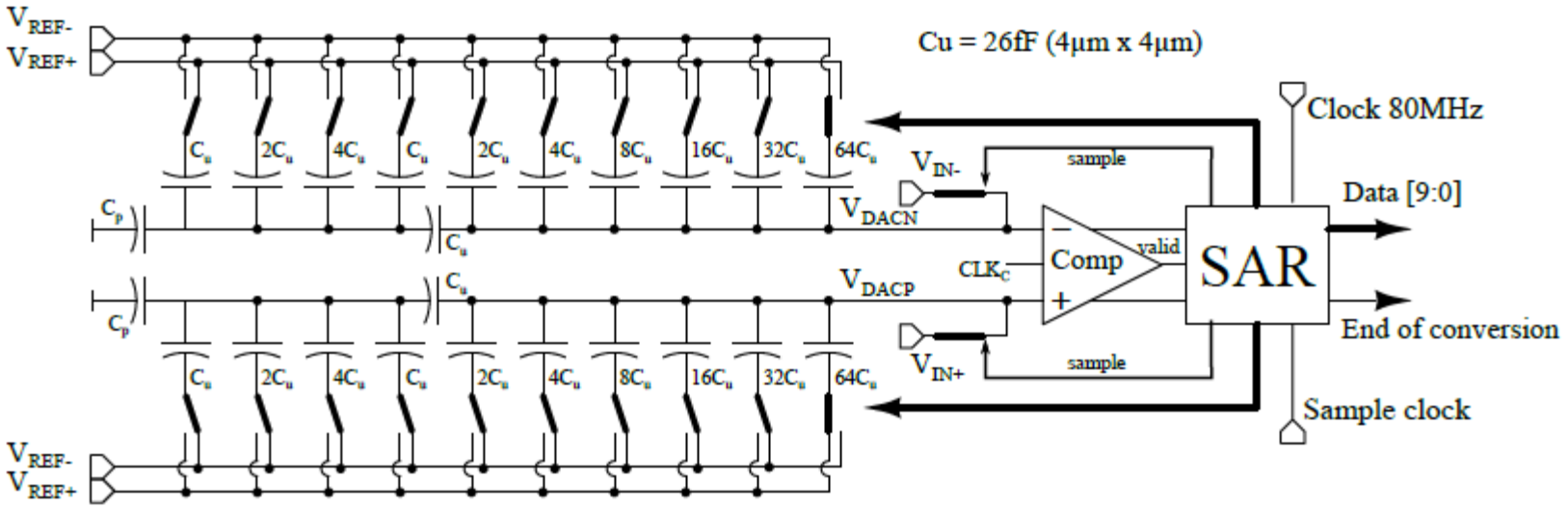
- Shaper
  - Creates a 4^{th} order semi-Gaussian pulse shape
  - Available shaping times (TS): ~~80~~, 160, 300 ns
  - Permits sampling by ADC at reasonable rates (10, 20 MHz)
  - 80 ns option eliminated in order to reduce noise in CSA

Pulse from Shaper



Functional Blocks

- ADC
  - 10 bit precision
  - 10 MSPS or 20 MSPS (5 MHz for ALICE TPC)
  - Split capacitor fully differential SAR architecture (low power)
  - ADC data rate = 10 MSPS * 10 bits * 32 channels = 3.2Gb/s (6.4 Gb/s)



Successive Approximation Register

Functional Blocks

- DSP
  - Baseline Correction 1 (BC1) – removes low frequency perturbations and systematic effects
  - Digital Shaper (DS) – tail cancellation or peaking time correction (IIR filter)
  - Baseline Correction 2 (BC2) – moving average filter
  - Baseline Correction 3 (BC3) – slope based filter (alternative to BC2)
  - Zero suppression – fixed threshold
  - Formatting; encoding for compression – Huffman
  - Buffering (16K x 10 bit)

Functional Blocks

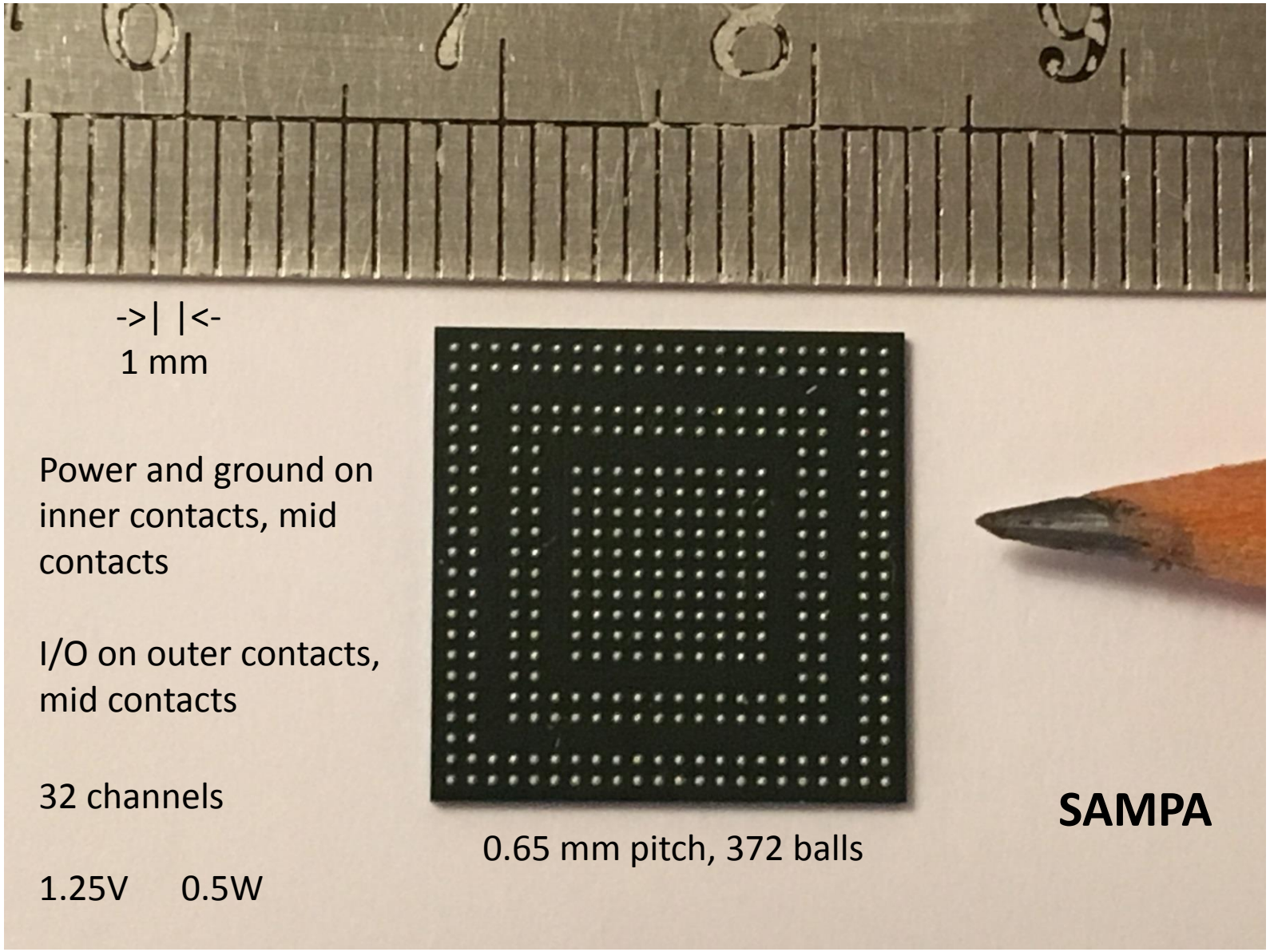
- e-link
  - Electrical interface for transmission of serial data over PCB traces or electrical cables, for distances of several meters
  - Up to 320 Mb/s
  - Developed by CERN for the connection between Front-end ASICs and their GigaBit Transceiver (**GBTx**) chip
  - Based on SLVS standard (Scalable Low-Voltage Signaling) – supply voltage as low as 0.8 V
  - Radiation-hard IP blocks for integration into ASICs
  - SAMPA: 11 e-links → 3.52 Gb/s max data output
  - Number and speed of SAMPA e-links used is programmable

SAMPA Specifications (ALICE)

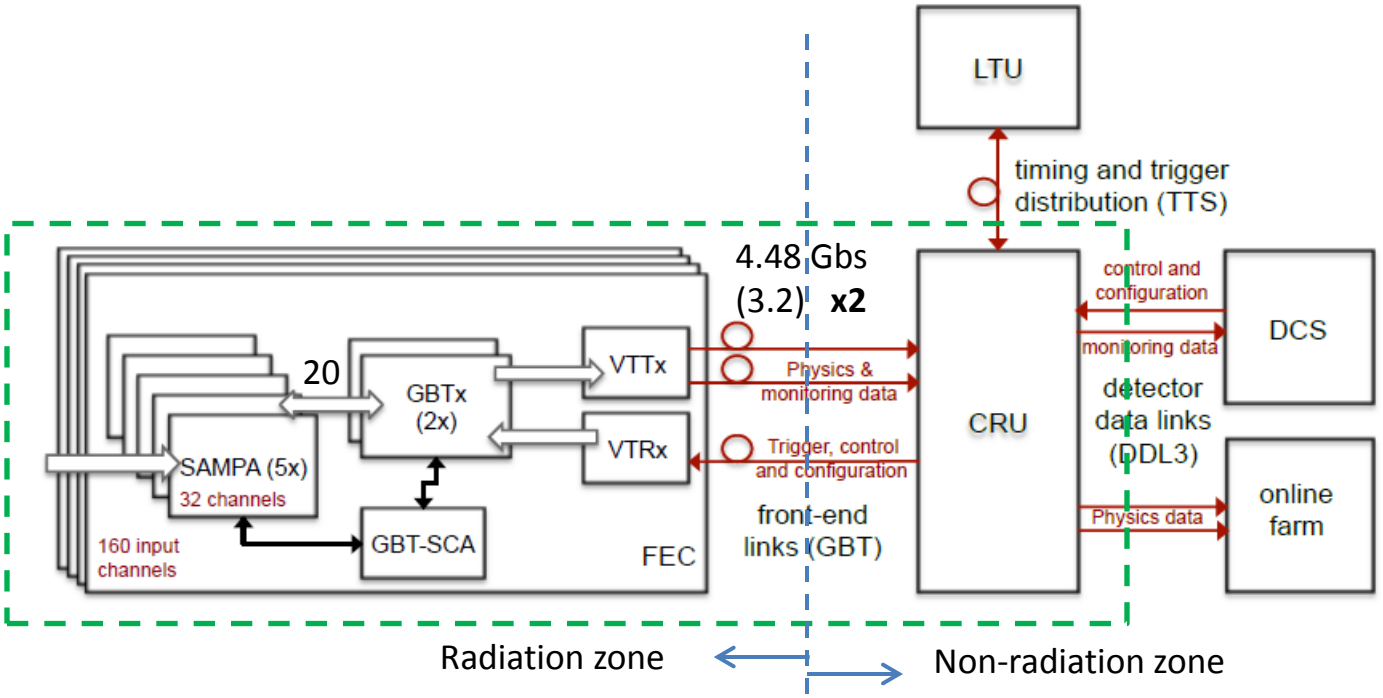
Specification	TPC	MCH
Voltage supply	1.25 V	1.25 V
Polarity	Negative	Positive
Detector capacitance (Cd)	18.5 pF	40 pF - 80 pF
Peaking time (ts)	160 ns	300 ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 600e@ts=160 ns*	< 950e @ Cd=40 pF* < 1600e @ Cd=80 pF*
Linear Range	100 fC or 67 fC	500 fC
Sensitivity	20 mV/fC or 30 mV/fC	4 mV/fC
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts=160 ns	< 0.2%@ts=300 ns
ADC effective input range	2 Vpp	2 Vpp
ADC resolution	10-bit	10-bit
Sampling Frequency	10 (20) Msamples/s	10 Msamples/s
INL (ADC)	<0.65 LSB	<0.65 LSB
DNL (ADC)	<0.6 LSB	<0.6 LSB
ENOB (ADC)**	> 9.2-bit	> 9.2-bit
Power consumption (per channel) CSA + Shaper + ADC	< 15 mW	< 15 mW
Channels per chip	32	32

*R_{esd} = 70Ω

** @ 0.5MHz, 10Msamples/s


->| |<-
1 mm
Power and ground on inner contacts, mid contacts
I/O on outer contacts, mid contacts
32 channels
1.25V 0.5W
0.65 mm pitch, 372 balls
SAMPA

ALICE SYSTEM



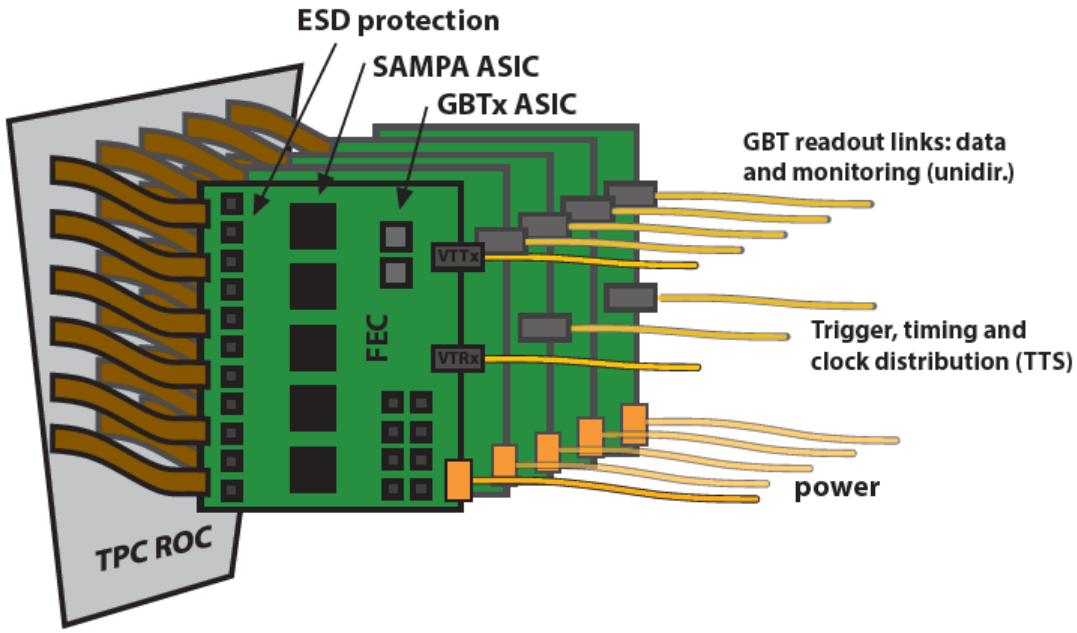
FEC – Front End Card (160 ch / FEC)

CRU – Common Readout Unit (12 FECs / CRU = 1920 ch / CRU

DCS – Detector Control System

LTU – Local Trigger Unit

ALICE Front-end Card (FEC)



Schematic of the readout system of the GEM TPC. Each FEC supports 5 SAMPA chips (160 ch). The **20 e-links** from the SAMPAs are routed into 2 GBTx chips (**10 per**). Each GBTx drives a fiber transmitter (VTTx) at 3.2Gb/s. Trigger, timing, clock, configuration data, and control commands are received on a separate fiber by a pair of FECs. (**Original plan**)

Common Readout Unit (CRU)

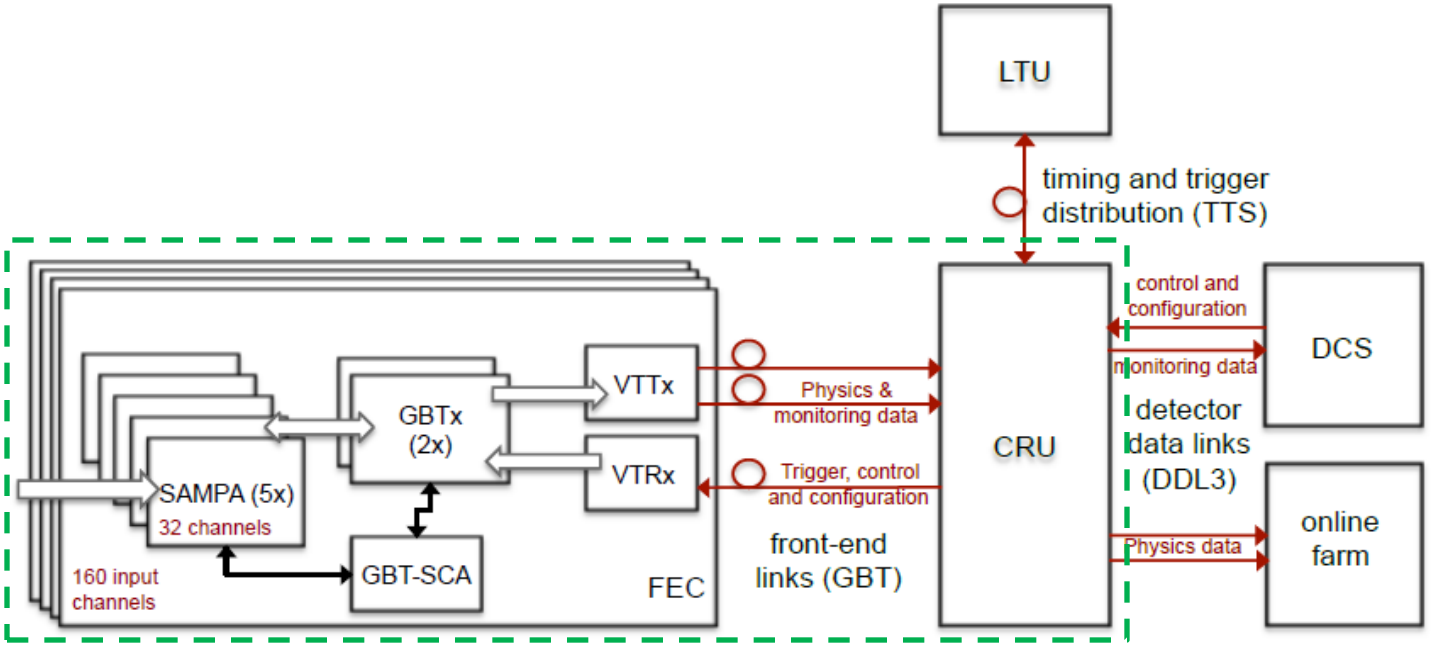
- Interface between the on-detector systems, the online computing system, and the Central Trigger Processor
- Multiplexes data from several front-end links into higher speed data links
- Can do processing on data
- Sends trigger, control, and configuration data to front-ends
- Based on commercial high-performance FPGA
- Located outside of radiation area, so no worry of SEUs
- **PCIe** platform

JLab Test Stand Goal

- Determine if the **SAMPA** chip is appropriate for the TDIS TPC as well as other detectors systems at JLab
- To achieve this goal we should:
  - Understand the SAMPA front end response to detector signals
  - Learn how to utilize the complex SAMPA DSP functionality to reduce data volume
  - Deal with a continuous readout data stream and link it with triggered data streams from other sources
- The last point goes beyond the SAMPA chip. Continuous readout systems are expected to be used in many future experiments.

- Ideally we should have a test system that can be scaled up and used for the final detector
- We should be able to connect the test system to an existing detector (e.g. prototype GEM detector at JLab or UVA)
- We should have a mechanism to pulse the inputs in a controlled fashion to study the effects of pileup and high rates on the SAMPA's DSP functions

- **Fast Track** – use as many components of the ALICE TPC readout/control chain as possible



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Advantages of Fast Track Solution

- System components have been verified and tested together.
- Almost “plug and play”.
- Development is reduced to coding (VHDL for data processing and formatting in FPGA, and software integration into CODA).
- Although the FEC would have to be redesigned to match the detector, the data transport model and sub-components (GBTx, GBT-SCA, VTRx, VTTx) can be used in the final solution.
- The CRU can be used in the final solution.
- What we learn from the test setup can be carried over to the actual system implemented.

- **We are acquiring 5 FECs and 1 CRU**

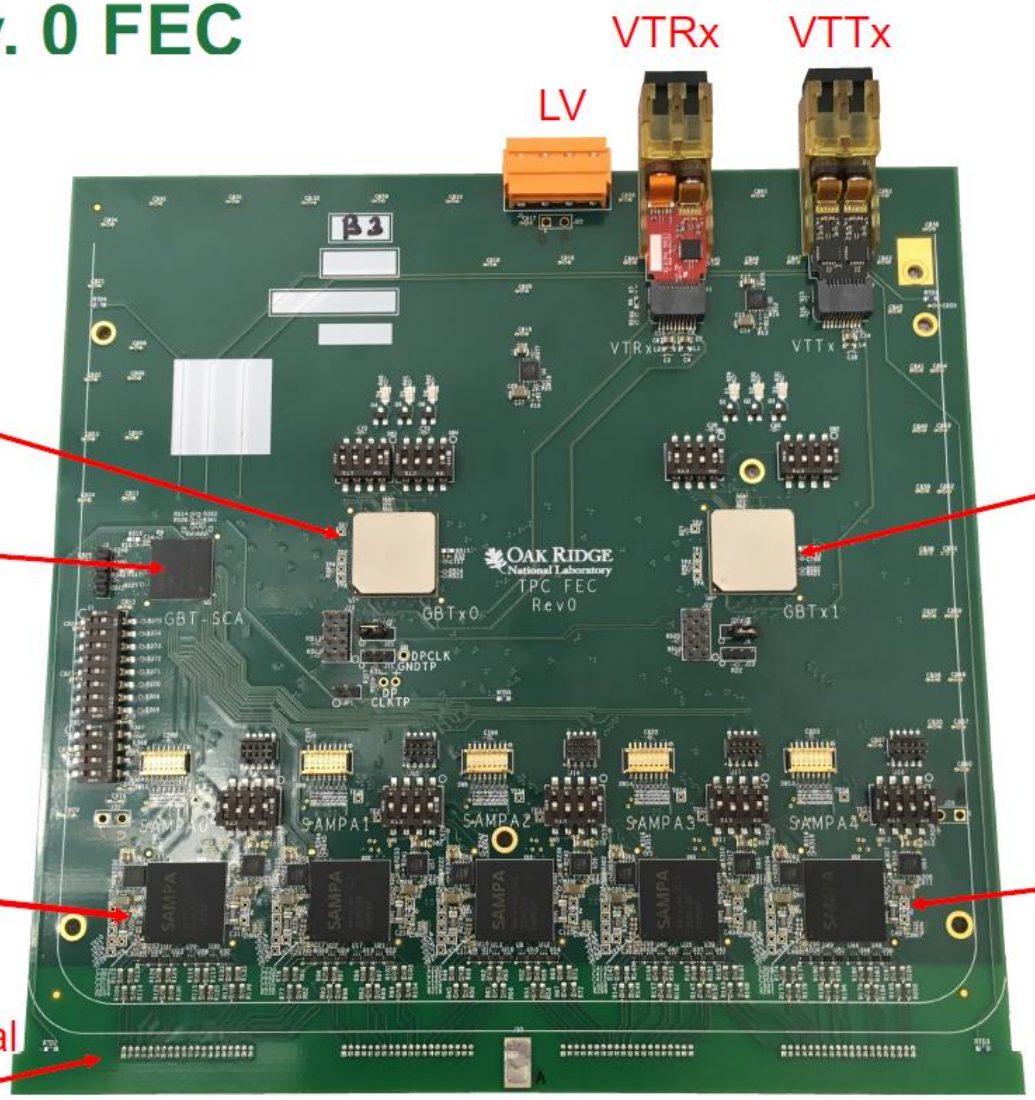
ALICE Front End Card (FEC)

- **Contact** - Chuck Britton, Oak Ridge National Lab (ORNL) (brittoncl@ornl.gov)

- **Plan**
  - ORNL gives us all manufacturing files and details necessary to duplicate FEC circuit board
  - We purchase the specialized components (SAMPA, GBTx, …) and have the board assembled
  - Request ORNL to run our assembled FECs through their rigorous testing station

  - **5 FECs shipped - delivery <u>October 2</u>**

TPC Rev. 0 FEC



assembled Rev. 0 FEC (board #3, top)

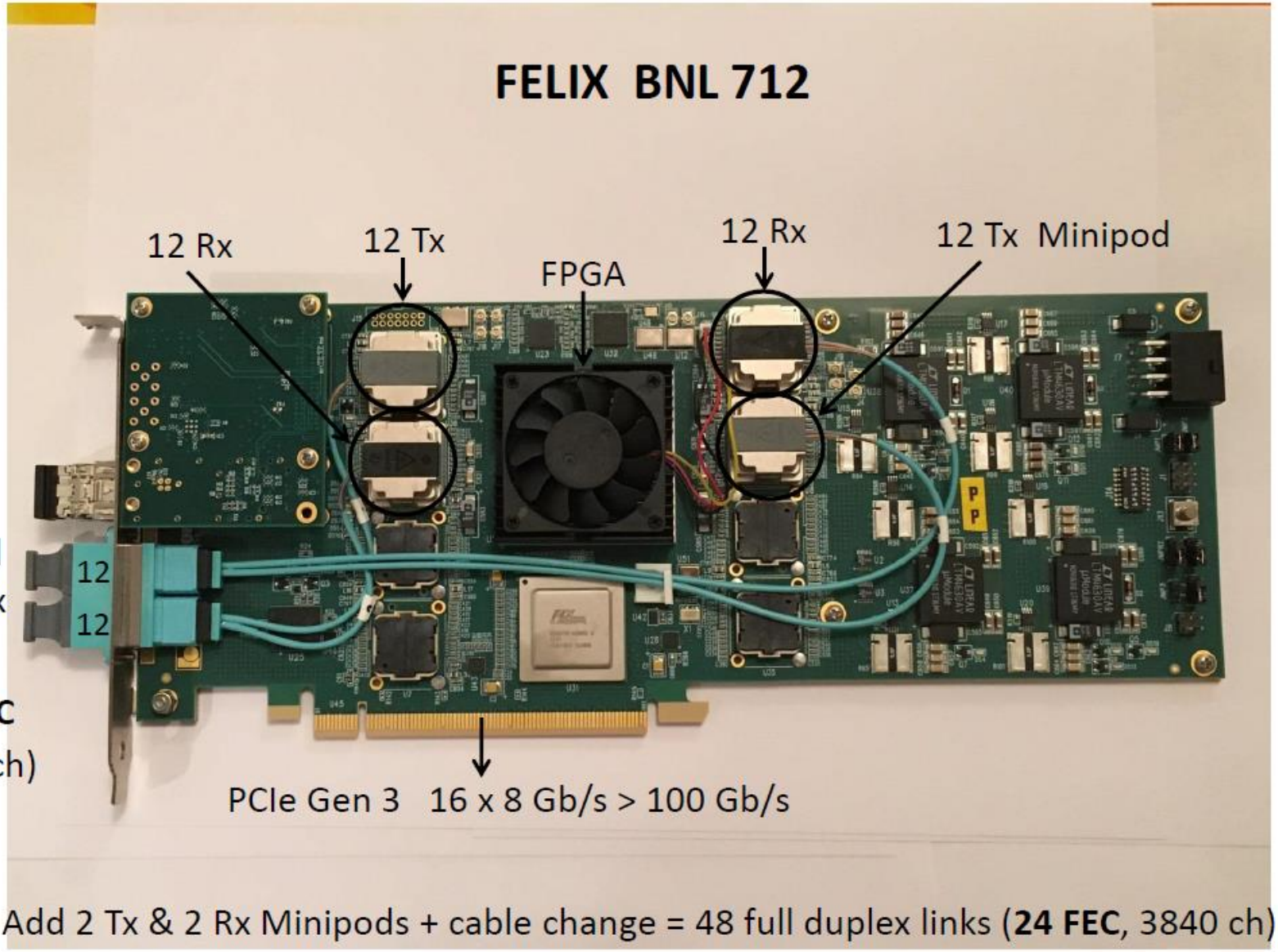
OAK RIDGE National Laboratory

Alternative to ALICE CRU

- ATLAS Readout Unit (**BNL-712**)
- **Contact** – Hucheng Chen, BNL, ATLAS (chc@bnl.gov)
- Part of their **FELIX** (**F**ront-**E**nd **LI**nk e**X**change) system
- PCIe based – custom designed - identical in concept to ALICE CRU
- Firmware exists to implement GBTx custom protocol and PCIe interface

- **Currently installed in high-end PC in DAQ lab**

FELIX BNL 712



Add 2 Tx & 2 Rx Minipods + cable change = 48 full duplex links (**24 FEC**, 3840 ch)