Hall A Compton DAQ Upgrade to CODA 3.0

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July 2012

I INTRODUCTION

The Hall A Compton Polarimeter has a counting-mode DAQ and an integrating-mode DAQ. The counting-mode DAQ was built in the 1998-1999 time frame. Although it has served us well, it needs to be modernized; many of the components can no longer be bought and several components are no longer well supported. There is also a prospect for making improvements, e.g. the old counting DAQ cannot handle helicity flip rates of 1 kHz.

The integrating-mode DAQ is relatively new, having been developed in 2008 by the CMU group, in collaboration with JLab, for the Parity experiments. We have fairly good knowledge of this system and can maintain it. The integrating DAQ will be merged with the counting DAQ so that they have synchronized data. We want to retain both DAQ systems because they have different advantages and different systematic errors.

See fig 1 for the preliminary concept of the upgrade. The goals of the upgrade are :

- Replace the obsolete counting-mode DAQ with new CODA 3.0 technologies based on the 250 MHz FADCs and pipelining electronics.
- Replace the slow part of the DAQ for processing signals from BPM, BCM, laser state, and control system state.

- Merge these DAQ systems with the integrating-mode DAQ. The result goes to a single Event Builder which correlates the data.
- Associated with this project, new analysis software will be required. Some of the old software could possibly be reused.

II SPECIFICATION OF THE NEEDS FOR COMPTON

The Hall A Compton Polarimeter is described at

http://hallaweb.jlab.org/compton

There are two detectors : a scintillating crystal calorimeter for detecting photons and a silicon microstrip tracking detector. In addition, one needs to record information about the beam position and beam current, the laser polarization state, the beam helicity state, and other controls-system signals.

At a minimum, there are four triggers :

- Photon singles trigger
- Electron singles trigger
- Coincidence of photon and electron
- Helicity trigger (fixed rate)

We need two kinds of DAQ systems. Each can probably fit in one VME (VXS) crate.

- A Fast DAQ to process the 100 kHz trigger rates in counting mode.
- A Slow DAQ with helicity trigger and possibly other low-rate triggers.

The detailed final design of the system will depend on the results of the prototype and the evolving understanding of the performance specifications and the needs. We provide below a preliminary concept of the design, see also fig 1.

The Fast DAQ will be based on the VME modules being built for the 12 GeV upgrade, specifically the JLab FADCs, Crate Trigger Processor (CTP), Subsystem Processor (SSP), and Trigger Interface and Distribution board (TI/D). The signals from the photon detector (one analog signal) can go into a single FADC module. The electron detector presently has amplified and

discriminated signal outputs from 768 channels; we foresee these going into an SSP module. The input to the SSP is a serialized fiber-optic signal train. Since we presently have 768 channels of discriminator output it will be necessary to gather those and convert them to the fiber-optic input for the SSP. To handle this gathering and conversion, we will need a custom board to be built by the electronics group; this is listed as "fiber converter" in tables 1 and 2. The SSP is an FPGA-programmable device that can form triggers from the electron detector (edet). This will replace the existing ETROC system. An edet trigger could be, for example, the coincidence of two or more planes, or a track requirement; the FPGA programming will need to be specified at a later date.

Both the FADC and the SSP passes information for crate trigger formation to the CTP (Crate Trigger Processor). The CTP has FPGA-based programming to decide on a trigger. For example, it could be programmed to require an electron detector trigger (which came from the SSP) or a photon trigger which is a hit above threshold in the photon detector (FADC). Another trigger could be a coincidence of photons and electrons. The crate will also have an SD board (signal distribution) necessary for communicating information such as the clock to the FADCs. The trigger output of the CTP goes the the TI/D board (trigger interface and distribution). The TI/D board is somewhat similar to the old TIR boards, except that it has some additional capability: it can prescale the triggers (up to six triggers allowed), it supports the multi-block readout mode which reduces the deadtime, and it synchronizes multiple crates (up to 8 crates). In this sense, the TI/D board is like a "miniature trigger supervisor" (TS) and we don't need a real TS for this system.

The Slow DAQ will read information that is either integrated over the helicity period or doesn't need to be recorded more frequently. This would include BPM, BCM, laser state, control system state, and scaler data. In addition, the CMU/JLab integrating FADC can be put into this slow DAQ. At a minimum, the trigger is just the helicity trigger, but we might devise other triggers, too. We think it will be necessary, however, to not miss any helicity triggers, so the deadtime logic needs to ensure that.

The two DAQs will be tied together and synchronized in hardware via their TI/D boards. The events will pass to a single Event Builder on a fast network.

III PROTOTYPING AND TEST PLANS

We propose to develop a prototype DAQ at a minimal cost (partly by scrounging what we bought for SOLID) and test the performance using a hardware simulation of the Compton process. Based on our understanding we

TABLE 1. Compton DAQ CODA 3.0 Prototype

Item	Units	Cost Ea (K$)	Borrow SOLID	Line Cost (K$)
VXS Crate	1	8	yes	0
cpu	1	3.5	yes	0
FADC 250	1	4	yes	0
SSP	1	5	no	5
CTP	1	5	no	5
SD	1	2.5	no	2.5
TID	1	3	no	3
fiber converter	1	5	no	5
misc		2	no	2
TOTAL COST				22.5 K$
COST if *not* borrow from SOLID				38 K$

can envision how to build the final DAQ system.

We can set up a test stand in Hall A near the existing DAQ. The prototype Fast DAQ can consist of one crate with cpu, FADC, SSP, CTP, SD, and TI/D boards. We can create signals that mimic the photon detector, electron detector, and coincidences. These may have variable random rates which we can control. We need to learn how to program the SSP and the CTP to make the triggers we want. This will involve some work with the engineers in the Fast Electronics Group (Chris Cuevas). Measurements of the deadtime will be important.

Once we have the Fast DAQ working we can combine it with the Slow DAQ to make a unified DAQ.

IV ESTIMATES OF COST AND TIME

In the tables 1 and 2 we show the items needed and the costs for the prototype and a rough estimate for the final design (we don't really know the final design yet). Some of the items we already have as they were bought for SOLID, so these will either need to be re-purchased for SOLID, or the cost of this project will increase if we move those items to SOLID as originally intended. This is why we show both the cost assuming we can borrow from SOLID and not assuming it. We think that there is a synergy between the development of this Compton DAQ and the tests needed to develop the SOLID DAQ, so these projects can be combined somewhat, at least in the beginning. The final design of the full system for Compton awaits the tests of the prototype, and therefore what is presented here is very preliminary. In table 3 we show an approximate timeline for this project.

TABLE 2. Compton DAQ Final Upgrade – Totals including prototype

Item	Units	Cost Ea (K$)	Line Cost (K$)
VXS Crate	2	8	16
cpu	2	3.5	7
FADC 250	1	4	4
SSP	1	5	5
CTP	2	5	10
SD	2	2.5	5
TID	2	3	6
fiber converter	1	5	5
misc		4	4
spares			24
TOTAL COST			86 K$
COST if we use what we have from SOLID			55 K$

TABLE 3. Timeline for the Compton DAQ 3.0 Upgrade

Approx. Completion Date	Milestone
Sep 2012	Initial set up of crate and infrastructure in Hall A
Nov 2012	Purchase remaining items for prototye (table 1)
Feb 2013	Initial tests of components. Spec CTP FPGA programming.
Jun 2013	Mock-up of Compton Signals, Tests with Triggers.
Jul 2013	Merge Fast and Slow DAQs
Aug 2013	Based on tests, specify full DAQ (an update on table 2)
Nov 2013	Purchase remainder of DAQ components.
Dec 2013	Finalize trigger definitions.
Mar 2014	Finish full-system tests. DAQ is ready for beam.

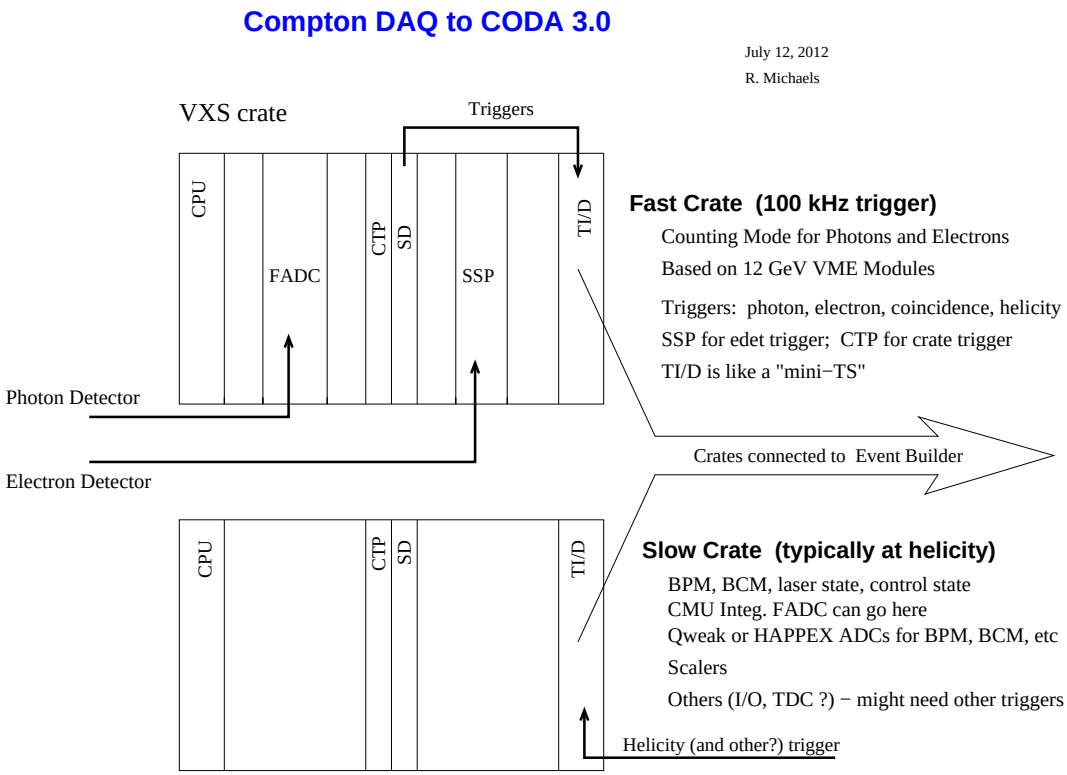

FIGURE 1.
Concept of the Proposed Compton CODA 3.0 DAQ