FADC DAQ upgrade
for Hall A Moller Polarimeter

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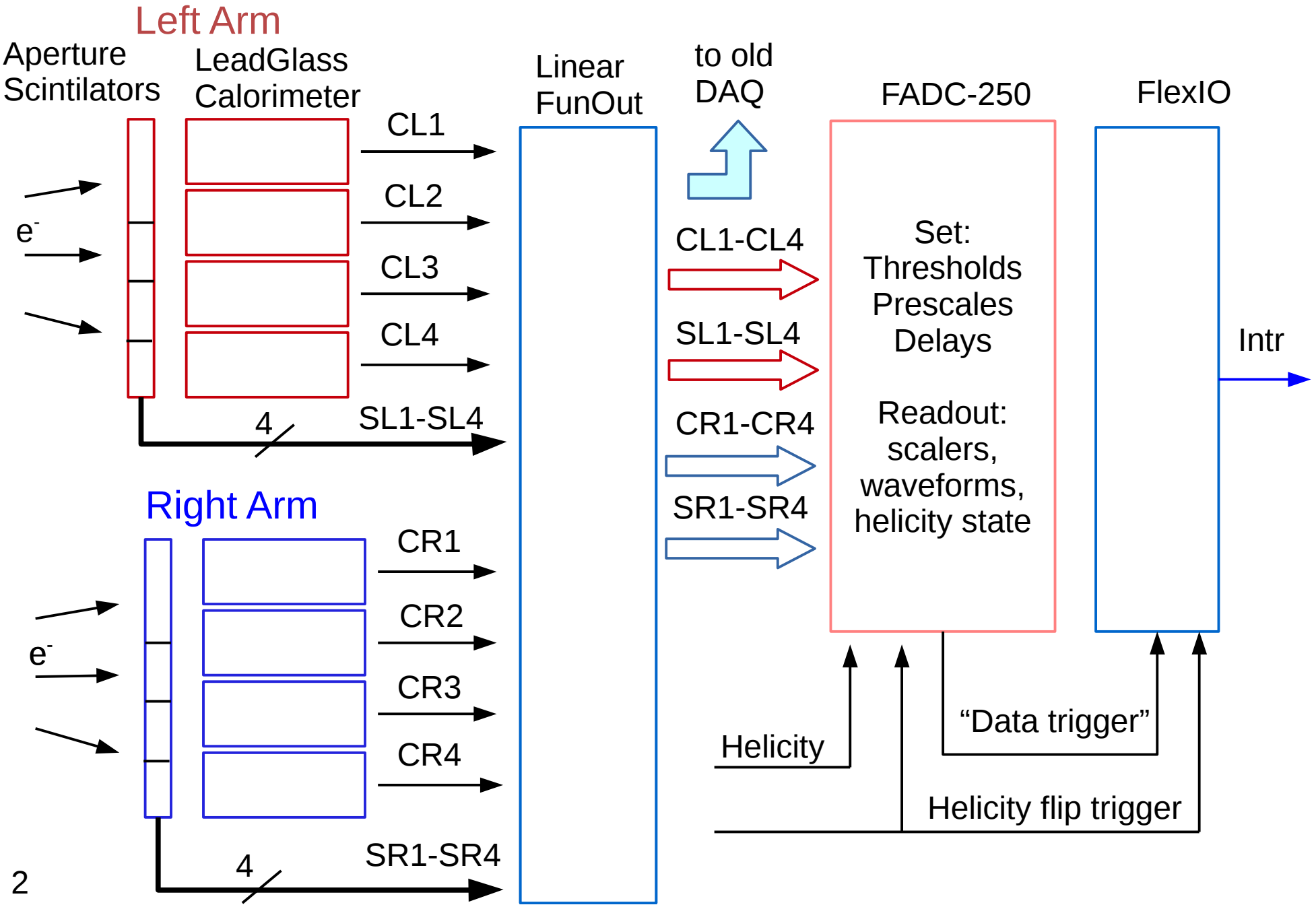
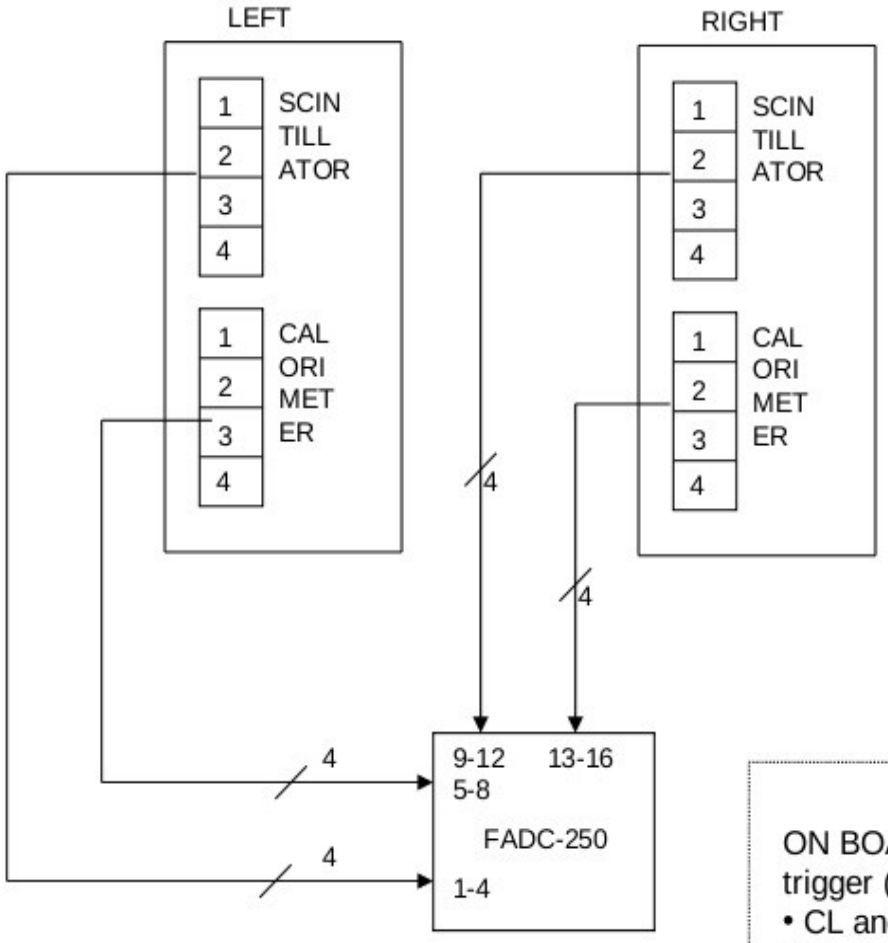
Hall A Moller Polarimeter FADC DAQ



Moller Polarimeter FADC DAQ
Signal Processing Logic

The input signals are typically -2 Volts and ~40 nsec wide with a fall time of 5 nsec.



When TRIGGER condition is met, send data that cause TRIGGER.

TRIGGER condition (or):
CL.AND.CR prescaled from 1 to at least 1000
CL prescaled from 1 to at least 1000
CR prescaled from 1 to at least 1000

$CR = \Sigma_{I=1,4}\Sigma_{j=1,2} P^J_I > \text{threshold}$

$CL = \Sigma_{I=1,4}\Sigma_{j=1,2} P^J_I > \text{threshold}$

$SL = (\Sigma_{J=1,2} S1^J > \text{threshold})$ or $(\Sigma J=1,2\ S2^J > \text{threshold})$ or $(\Sigma J=1,2\ S3^J > \text{threshold})$ or $(\Sigma J=1,2\ S4^J > \text{threshold})$

$SR = (\Sigma_{J=1,2} S5^J > \text{threshold})$ or $(\Sigma J=1,2\ S6^J > \text{threshold})$ or $(\Sigma J=1,2\ S7^J > \text{threshold})$ or $(\Sigma J=1,2\ S8^J > \text{threshold})$

ON BOARD SCALER (COUNTER) to be read out by a separate trigger (helicity and gate bits) at the helicity cycle of 30 to 2kHz.

- CL and CR
- CL and SL
- CR and SR
- CL and CR and SL and SR
- ~~CL and CR and (SL and SR delayed > 100 ns)~~
- (CL and CR and SL and SR) delayed > 100ns
- CL
- CR

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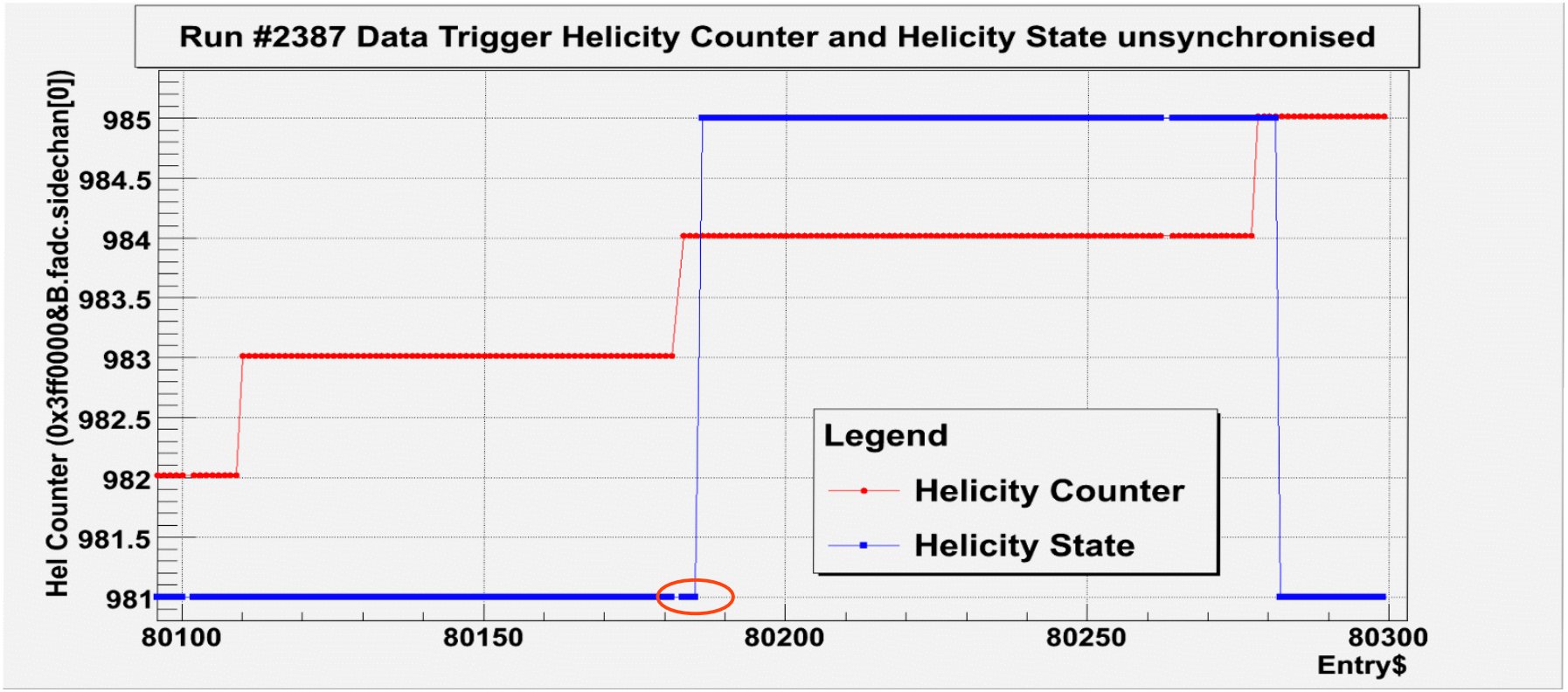
- The FADC implementation does the following:
- Make logical signals when combination of the input signals exceed certain thresholds;
- Write out the FADC “event" data using a logical signal for the trigger with an adjustable prescaler, at a rate up to the maximum rate allowed by the existing FADC systems (160kHz);
- Makes internal scalers in the FADC unit counting the coincidence signal; the scalers are readout at every helicity cycle;
- The readout includes the “event triggers" (or “data_triggers” <160kHz) and the “helicity triggers" (30 – 2000Hz). Both additionally contain the helicity bit, the QRT bit, helicity window counts;
- The “helicity trigger" readout includes additional external scalers/ADC for the BCM, pulser, BPM, encoders etc.

“Data trigger” issue



1. There is 10 bits counter of helicity windows in data stream and helicity state bit for “event trigger”. During run the state of helicity window and helicity counter are lost synchronization: helicity counter is incremented by one for next helicity window (with opposite sign, for example), but helicity state bit is still unchanged for few next events. It gives wrong helicity state for that windows.
Number of events with this issue for one window is changed during the run in range 0-50% of all triggers per window. For 1000Hz helicity rate it is more frequently situation than for 30Hz.

2. After Hall A runs long time with high beam current >20uA on target, FADC data trigger timestamps for chip#1 and chip#2 (two 48-bit free-running counters) are lost synchronization:

ERROR: time1= 41E D2236 time2= 41E D2237
time1= 41E 10EC7A time2= 41E 10EC7B

We are suppose that this error is due to radiation in Hall A.

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FADC firmware upgrading

We would like to have some kind of programable logic unit (PLU) on the board of FADC to set different coincidence combinations between single calorimeter channels and counting it on the scalers: CL1-CL4, CR1-CR4, SL, SR.
For example: SL.and.CL2.and.CR2, SL.and.CL2.and.CR, ...

The module type of LeCroy-2365 can be used as prototype for this PLU.

Preliminary PLU parameters:

10 inputs by 8 outputs, with possibility to provide the connection of any inputs to output through the logic function of (OR), (AND) for inputs and function (NOT) for outputs.

The programmable registers (read/write):

8 registers (10-bit) for AND function (every bit is corresponded to one input, the register number is corresponded to the output number),
8 registers (10-bit) for OR function (every bit is corresponded to one input, the register number is corresponded to the output number)
One (8-bit) register for NOT function of output (every bit is corresponded to one output).

Scalers:

8 channels of 32-bit counters connected to the corresponded outputs of the PLU.
The scalers are readout at every “helicity trigger”.

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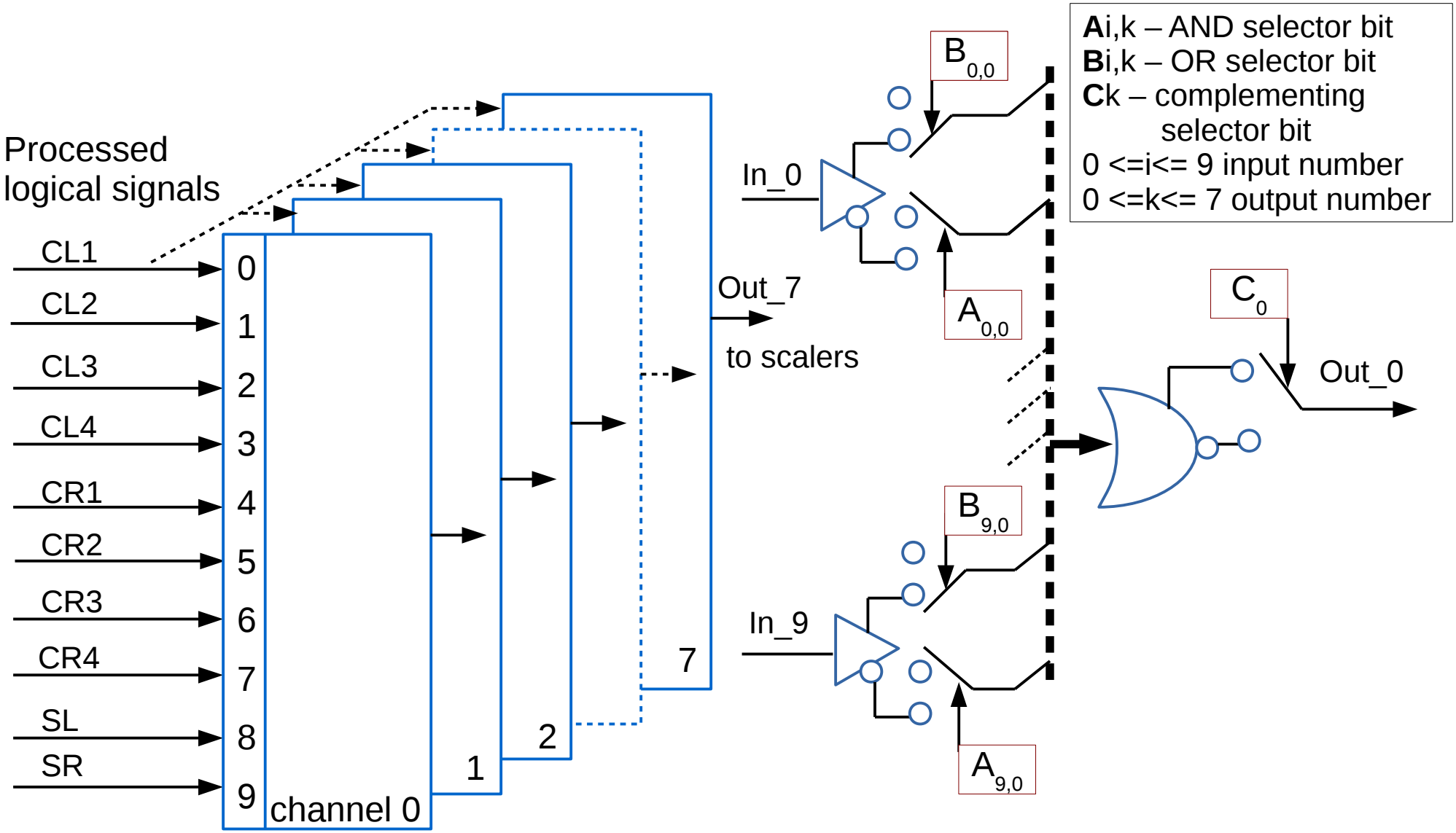
PLU unit (from LeCroy 2365)



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Summary for upgrade

1. Possibility to disable “data trigger” at all and use only “helicity trigger”. It is useful for rutine measurements.
2. A. Implemetation of PLU unit with 10 inputs, 8 outputs with scalers (8-channels). The scalers are readout at every “helicity trigger”.
3. B. If PLU implementation is not possible, then add more logical combinations and scalers: **SL, SR, SL.and.CL2.and.CR2, SL.and.CL.and.CR2, ...**
4. Resolve issue with “data triger” (lost synchronization helicity state).

Thank you for attention!!!

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Scalers on board

The FPGA produces a kind of a scaler, counting:

- CL
- CR
- CL.AND.CR
- CL.AND.SL
- CR.AND.SR
- CL.AND.CR.AND.SL.AND.SRCR.AND.SR
- (CL.AND.CR.AND.SL.AND.SR) delayed>100ns

These scalers are readout by a separate trigger at the helicity cycle at 30Hz to 2kHz. The scalers are a deadtime-free integration of the data, integrated over the helicity period. The integration time is defined by externally supplied helicity gate.