Moller DAQ with the FADC250

CR: CALORIMETER RIGHT [1-4]

SR: SCINTILLATOR RIGHT [1-4]

CL: CALORIMETER LEFT [1-4]

SL: SCINTILLATOR LEFT [1-4]

A: [HELICITY, HELICITY_FLIP] (NIM or ECL)

a: [HELICITY, HELICITY_FLIP] (LVDS)

b: [HELICITY_TRIGGER, DATA_TRIGGER] (LVDS)

B: [HELICITY_TRIGGER, DATA_TRIGGER] (ECL)

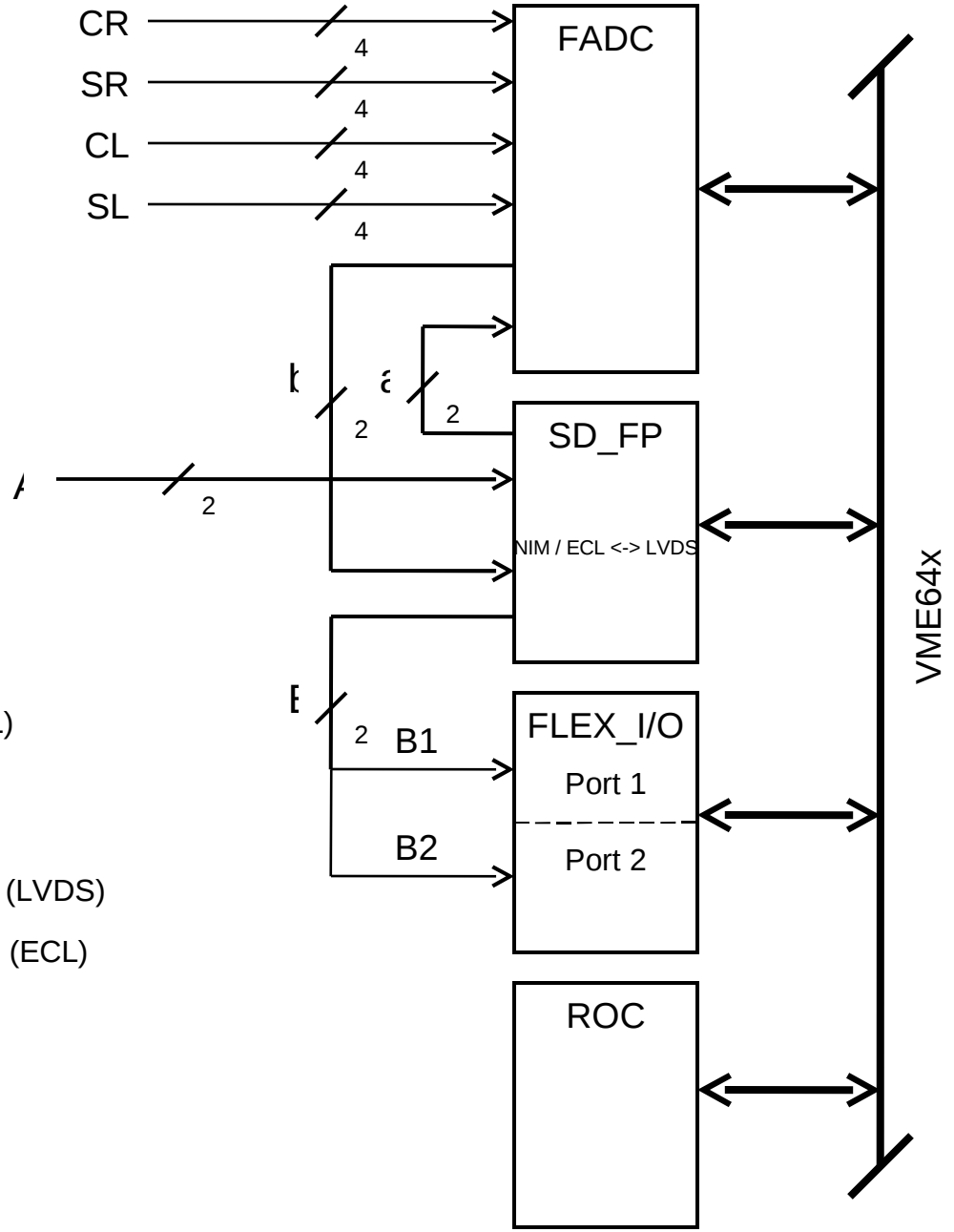
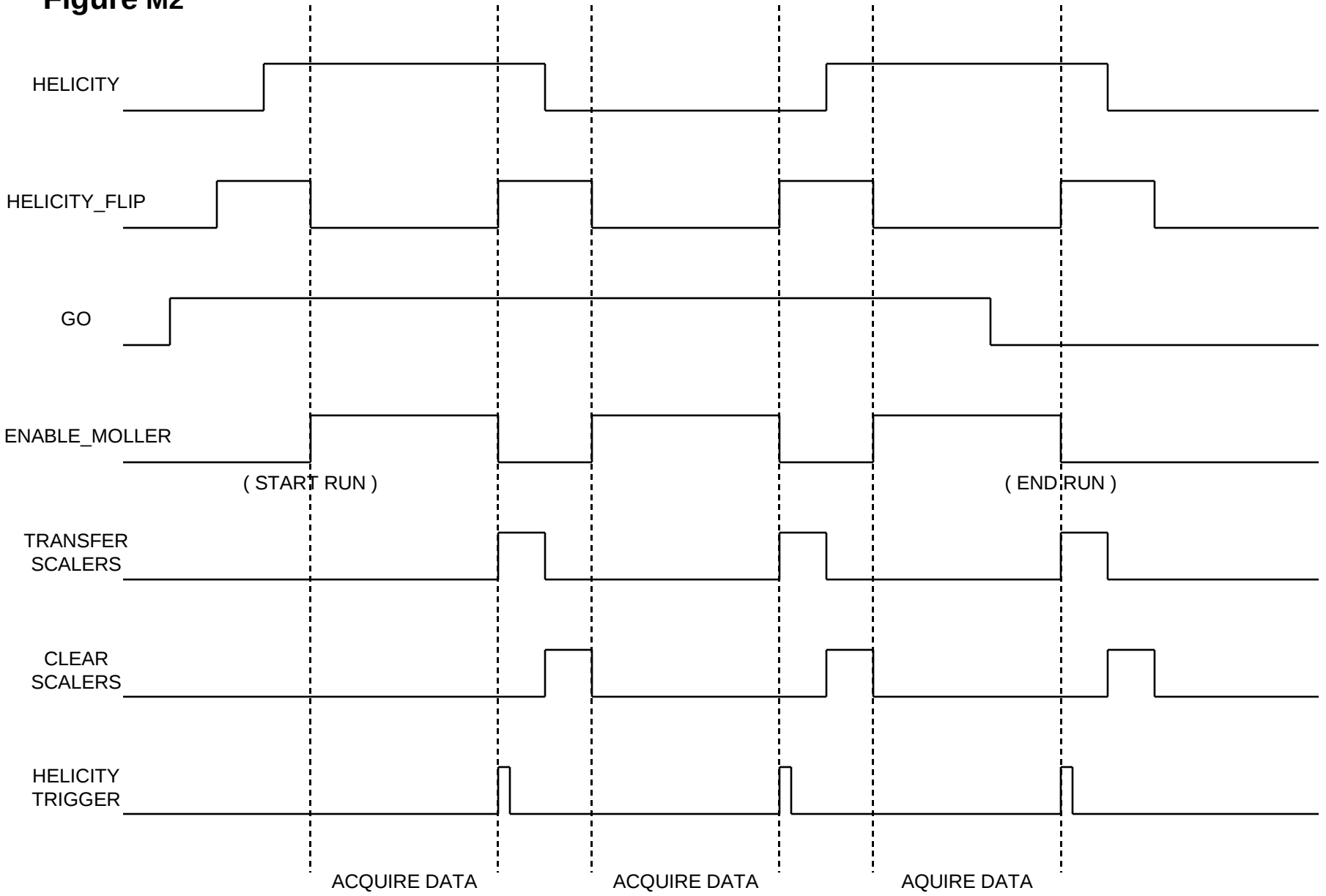


Figure M1

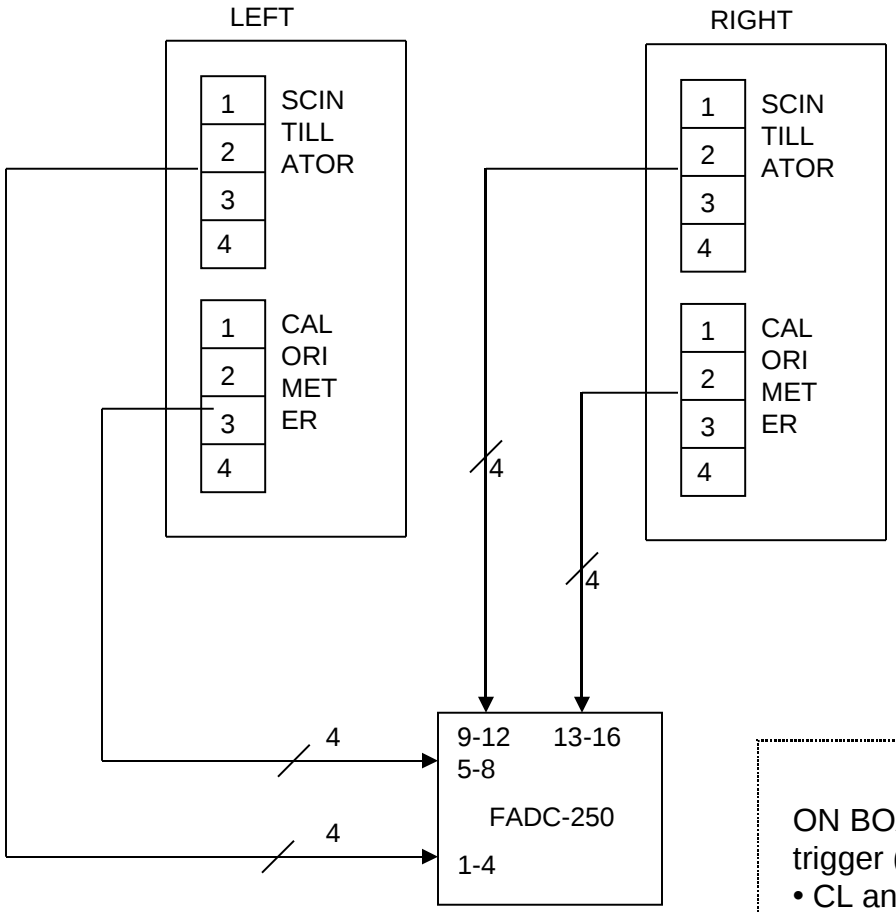
Overview

- Scintillator and calorimeter signals from the left and right halves of a Moller polarimeter are input into the FADC. Using the flexibility and speed of the FPGA, various logical quantities based on digital sums and hit patterns of the inputs is computed (see detailed description later). Some of these quantities (5) are scaled, while others (3) are used to trigger the capture of the input pulses that produced them. The comparison of the scaler values for the beam in its two helicity states is the object of the study.
- Figure M2 shows the free-running accelerator signals HELICITY and HELICITY_FLIP. These are input as control signals into the FADC front panel (after level conversion by the SD_FP module). The assertion of HELICITY_FLIP indicates that the helicity state is in transition, so scalers and triggers are disabled during this time.
- When the user issues GO to start a data run, enabling of scalers and triggers (ENABLE_MOLLER) will not begin until the trailing edge of the *next* HELICITY_FLIP pulse. Similarly, when GO is negated, acquisition will continue until the leading edge of the *next* HELICITY_FLIP pulse. In this way, data will always be acquired for an integral number of valid helicity periods (ENABLE_MOLLER).
- At the end of each ENABLE_MOLLER period, scaler data (ten 16-bit words) is transferred from the Moller FPGA to the Control FPGA over the 16-bit control bus. It is stored in an internal FIFO as six 32-bit words (1 header + 5 scalers). The header identifies the helicity state (bit 31) and the helicity interval number (bits 30-0). When the transfer is complete, the scalers are cleared. They are enabled to count again when ENABLE_MOLLER is asserted.
- At the end of each ENABLE_MOLLER period, the pulse HELICITY_TRIGGER is output from the FADC front panel. This is used to interrupt the Read Out Controller (ROC) so that the scaler data can be read out. This is done by routing the signal to port 1 of the FLEX I/O module (after level conversion by the SD_FP).
- For each internally generated trigger, the helicity state and trigger pattern are stored as a single word in the MOLLER FIFO. As the ADC data is being collected, the trigger word is transferred to the Control FPGA over the control bus, and appears as a type 10 (user defined) data word in the event.
- Data from internally generated triggers is stored on the FADC until a programmed number (block, 255 maximum) of events is acquired. When this happens, a pulse (DATA_TRIGGER) is issued from the FADC front panel. This signal is routed to port 2 of the FLEX I/O module (after level translation by the SD_FP module). The FLEX I/O interrupts the ROC so that the block of events may be read out. When the read out is complete, the ROC acknowledges the transfer and re-enables DATA_TRIGGER generation.

Figure M2


HELICITY
HELICITY_FLIP
GO
ENABLE_MOLLER
(START RUN)
(END RUN)
TRANSFER SCALERS
CLEAR SCALERS
HELICITY TRIGGER
ACQUIRE DATA
ACQUIRE DATA
AQUIRE DATA

HALL A Moller Polarimeter Requirement



When TRIGGER condition is met, send data that cause TRIGGER.

TRIGGER condition (or):
CL.AND.CR prescaled from 1 to at least 1000
CL prescaled from 1 to at least 1000
CR prescaled from 1 to at least 1000

$CR = \Sigma_{I=1,4}\sum_{j=1,2} P^J_I >$ threshold

$CL = \Sigma_{I=1,4}\sum_{j=1,2} P^J_I >$ threshold

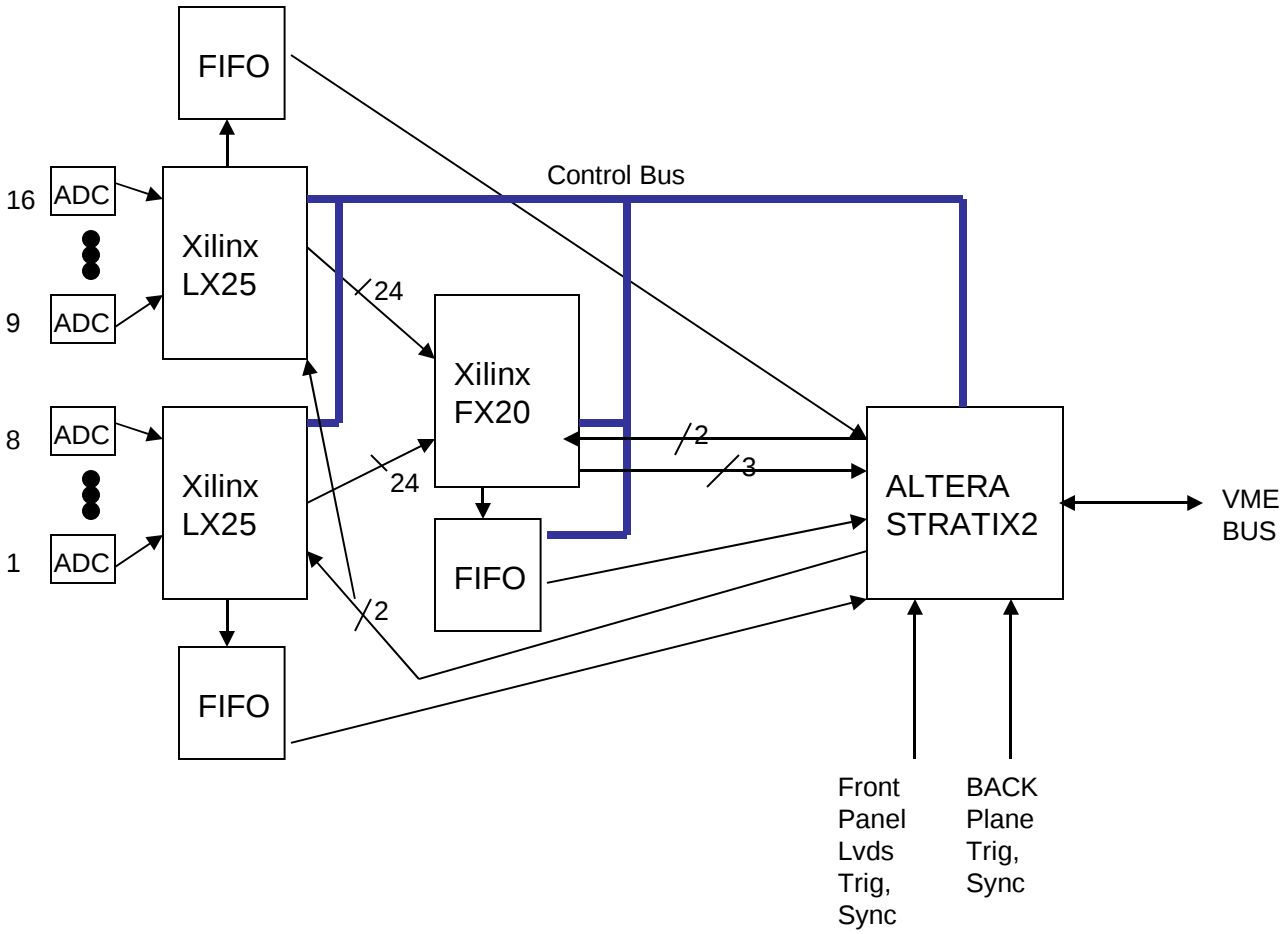
$SL = (\Sigma_{J=1,2} S1^J >$ threshold) or $(\Sigma J=1,2\ S2^J >$ threshold) or $(\Sigma J=1,2\ S3^J >$ threshold) or $(\Sigma J=1,2\ S4^J >$ threshold)

$SR = (\Sigma_{J=1,2} S5^J >$ threshold) or $(\Sigma J=1,2\ S6^J >$ threshold) or $(\Sigma J=1,2\ S7^J >$ threshold) or $(\Sigma J=1,2\ S8^J >$ threshold)

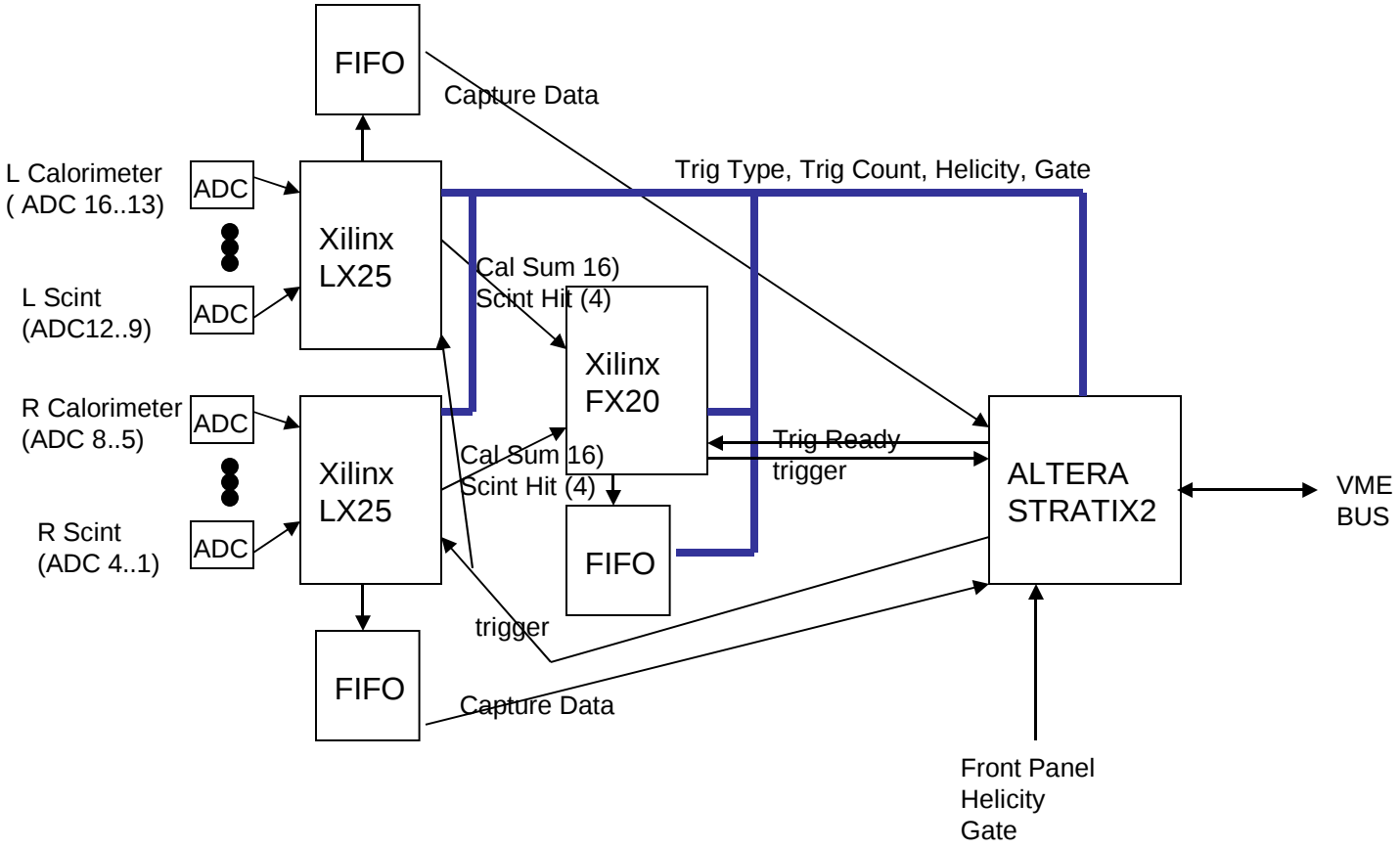
ON BOARD SCALER (COUNTER) to be read out by a separate trigger (helicity and gate bits) at the helicity cycle of 30 to 2kHz.

- CL and CR
- CL and SL
- CR and SR
- CL and CR and SL and SR
- CL and CR and (SL and SR delayed > 100 ns)

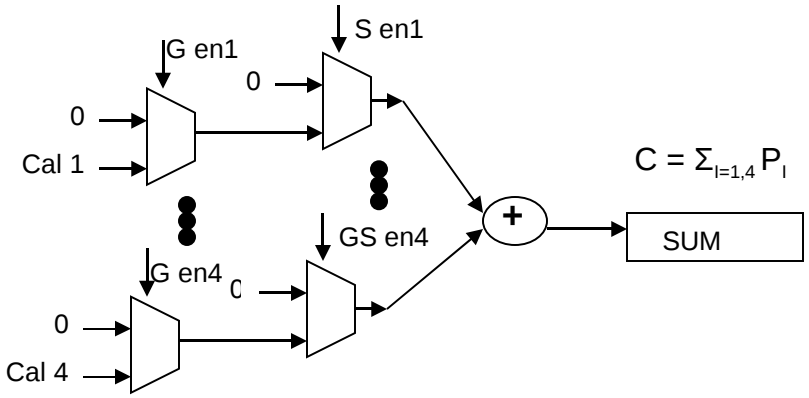
FADC HARDWARE ARCHITECTURE

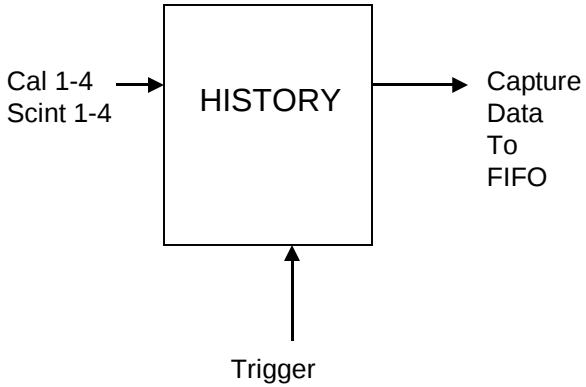


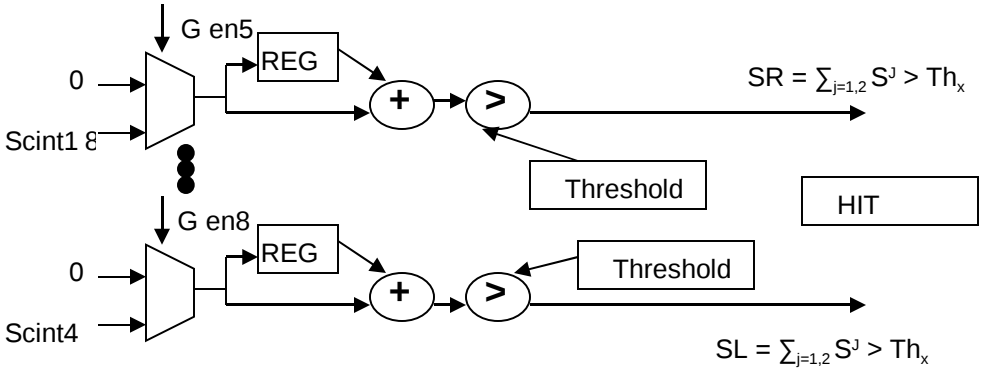
MOLLER DAQ FIRMWARE ARCHITECTURE
TOP LEVEL



MOLLER DAQ FIRMWARE ARCHITECTURE
Xilinx LX25 TRIGGER



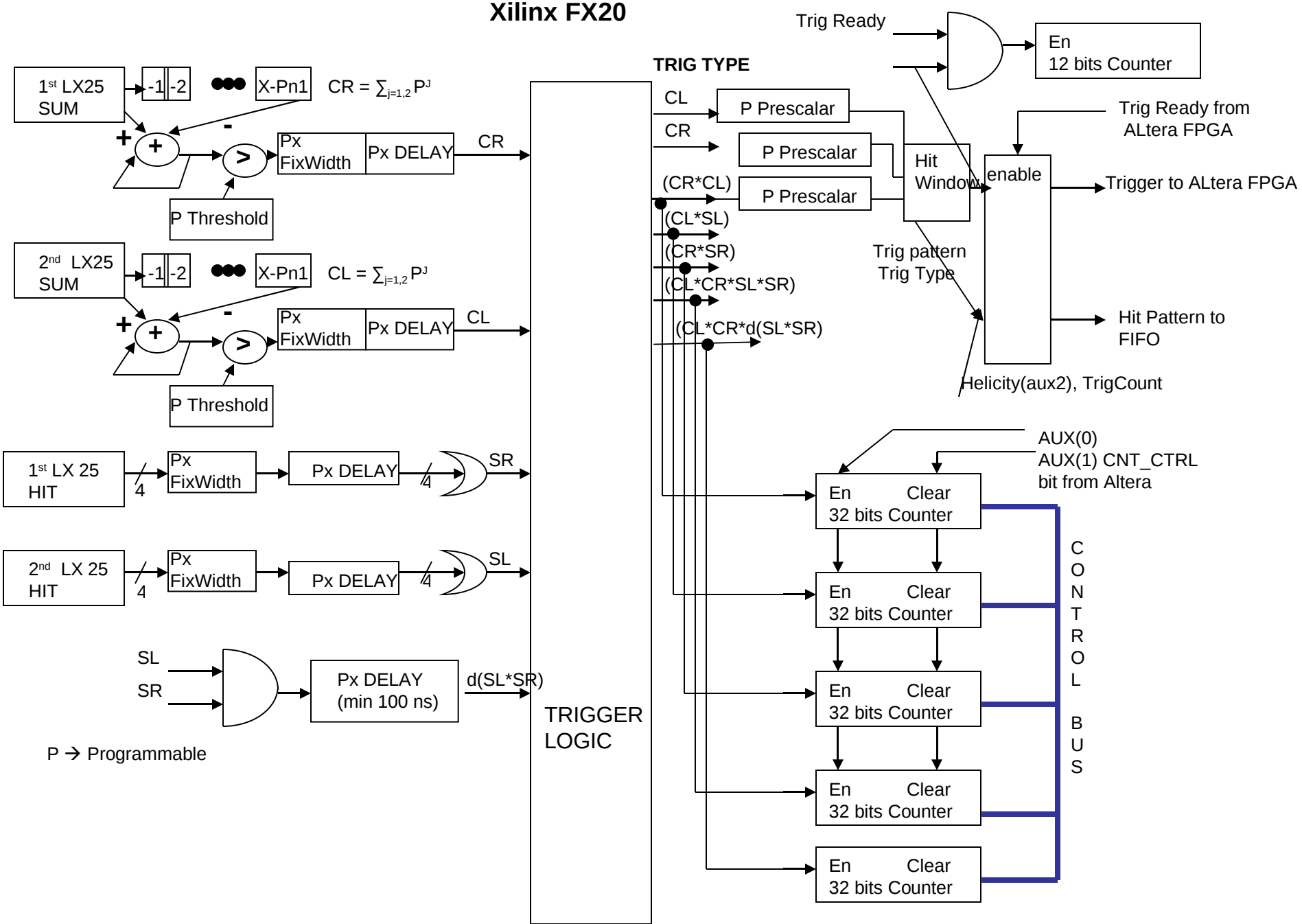




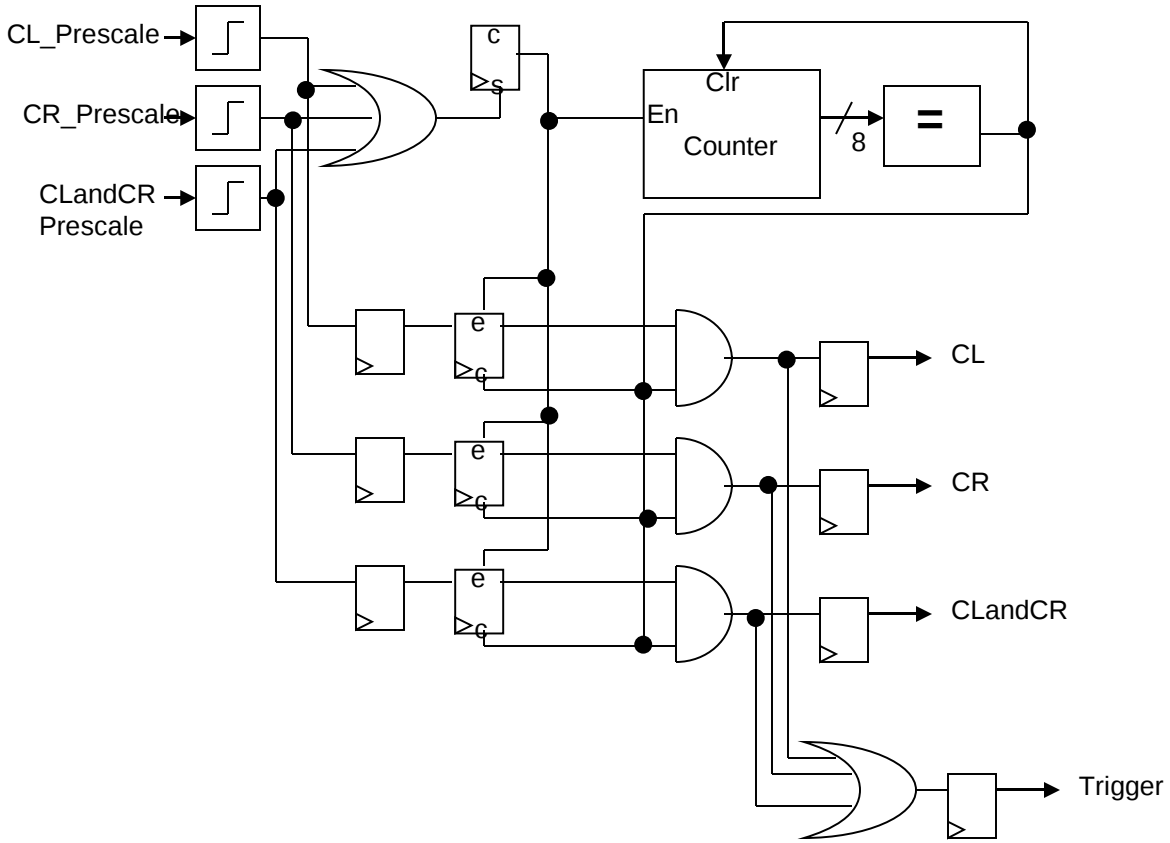
No change to Look Back Algorithm

G → Global

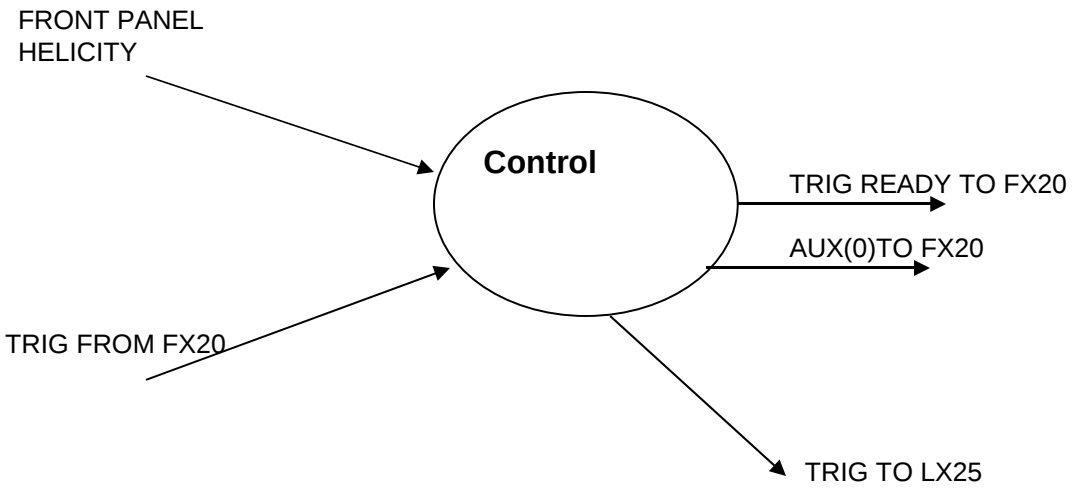
MOLLER DAQ FIRMWARE ARCHITECTURE
Xilinx FX20



MOLLER DAQ FIRMWARE ARCHITECTURE
Xilinx FX20 (Hit Window)



MOLLER DAQ FIRMWARE ARCHITECTURE
Altera FPGA



MOLLER DAQ FIRMWARE ARCHITECTURE
Altera FPGA