Wire Ch1 + Ch2 Test

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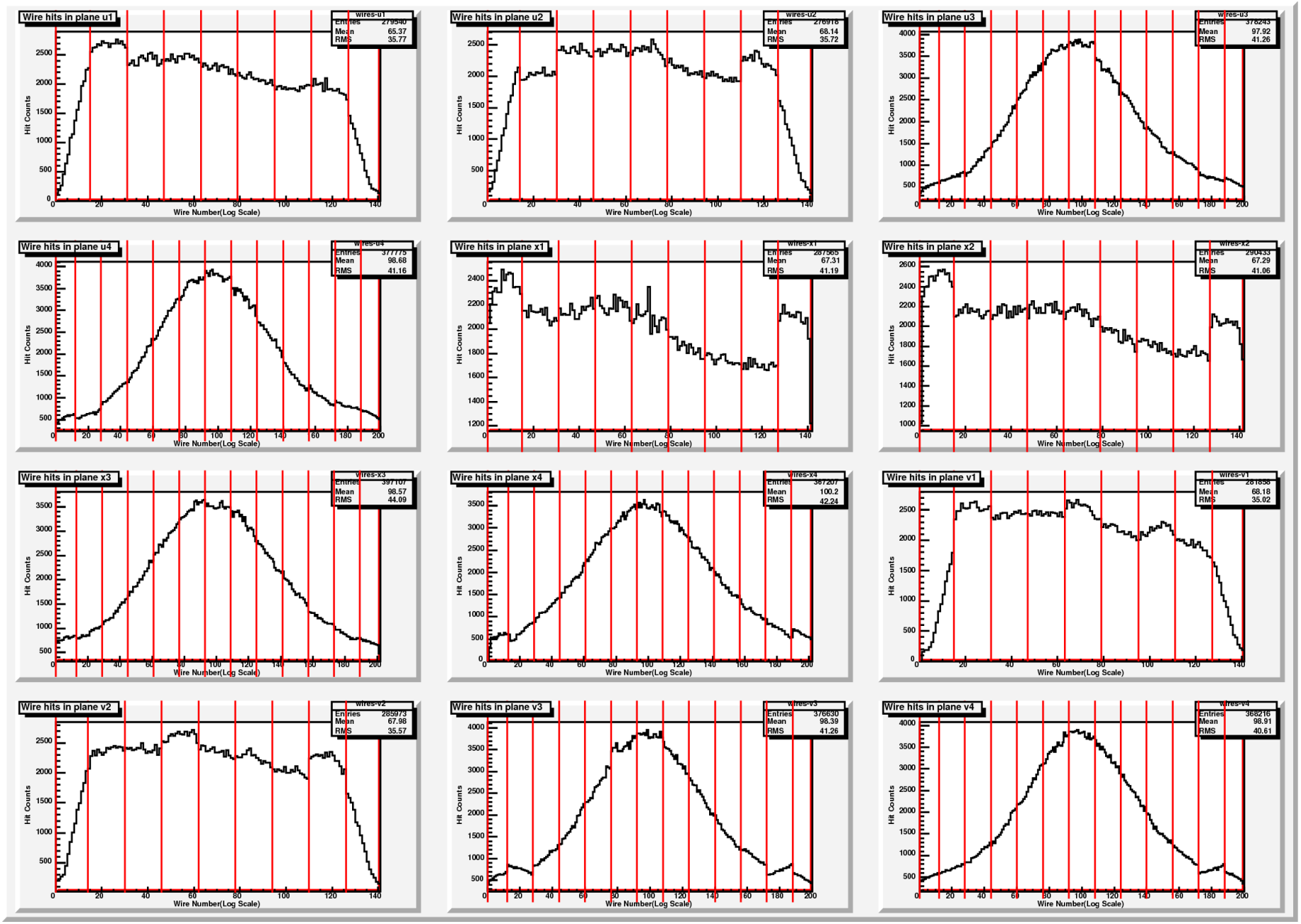
Wire Chamber Work

- Reconnect all cables according to the final mapping which handles FASTBUS and VME readout at the same time (efforts from all students).
- Test/fix all the long/short cables, test all the patch panels.
- Modify electron package HV lines according to the final version.
- Still need:
  - 4 VME TDC for 3 chamber test.
  - ~50 A/D cards on chamber.
  - Some 1877 FASTBUS TDC? (Kalyan)

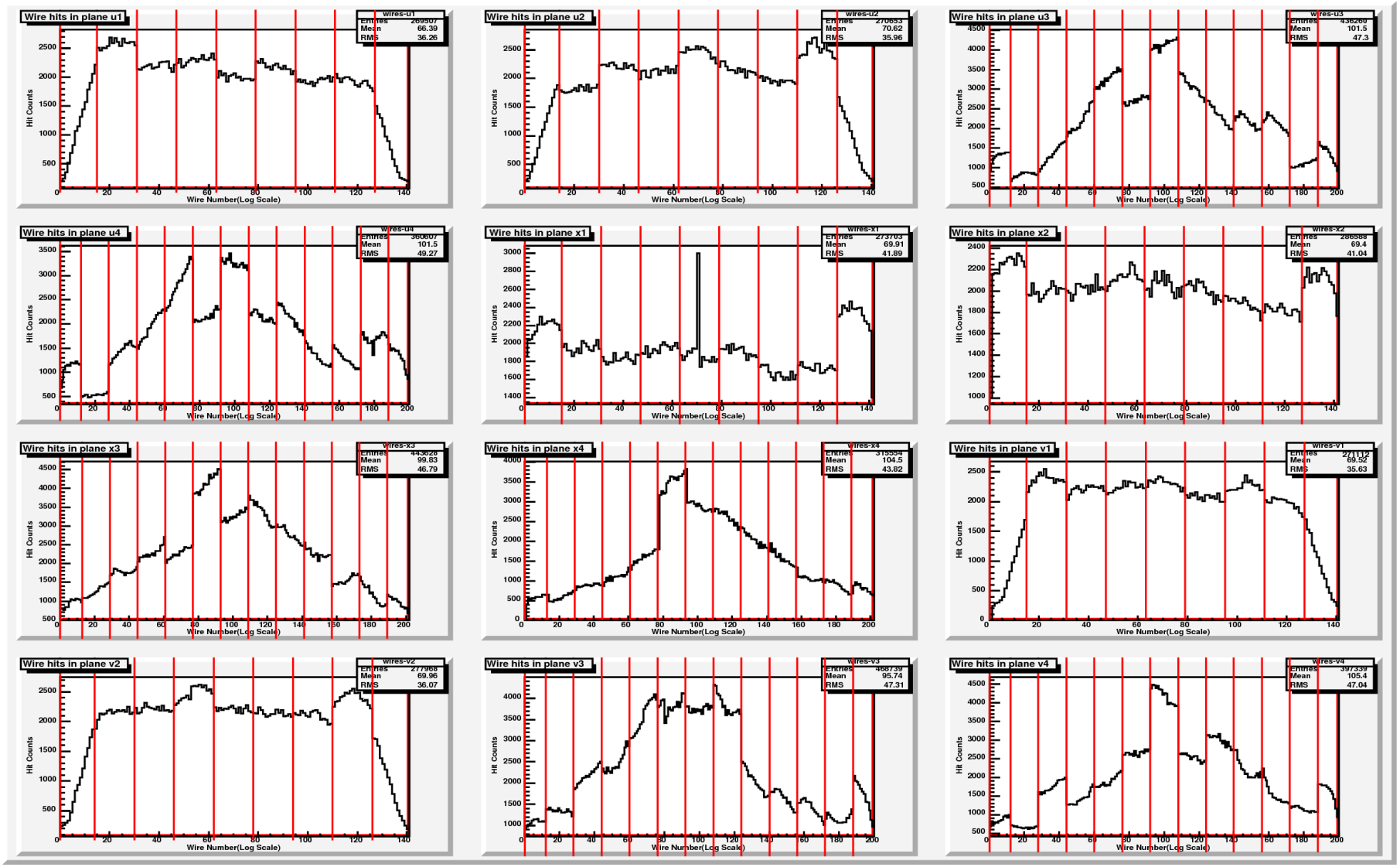
Wire Chamber Hit Pattern



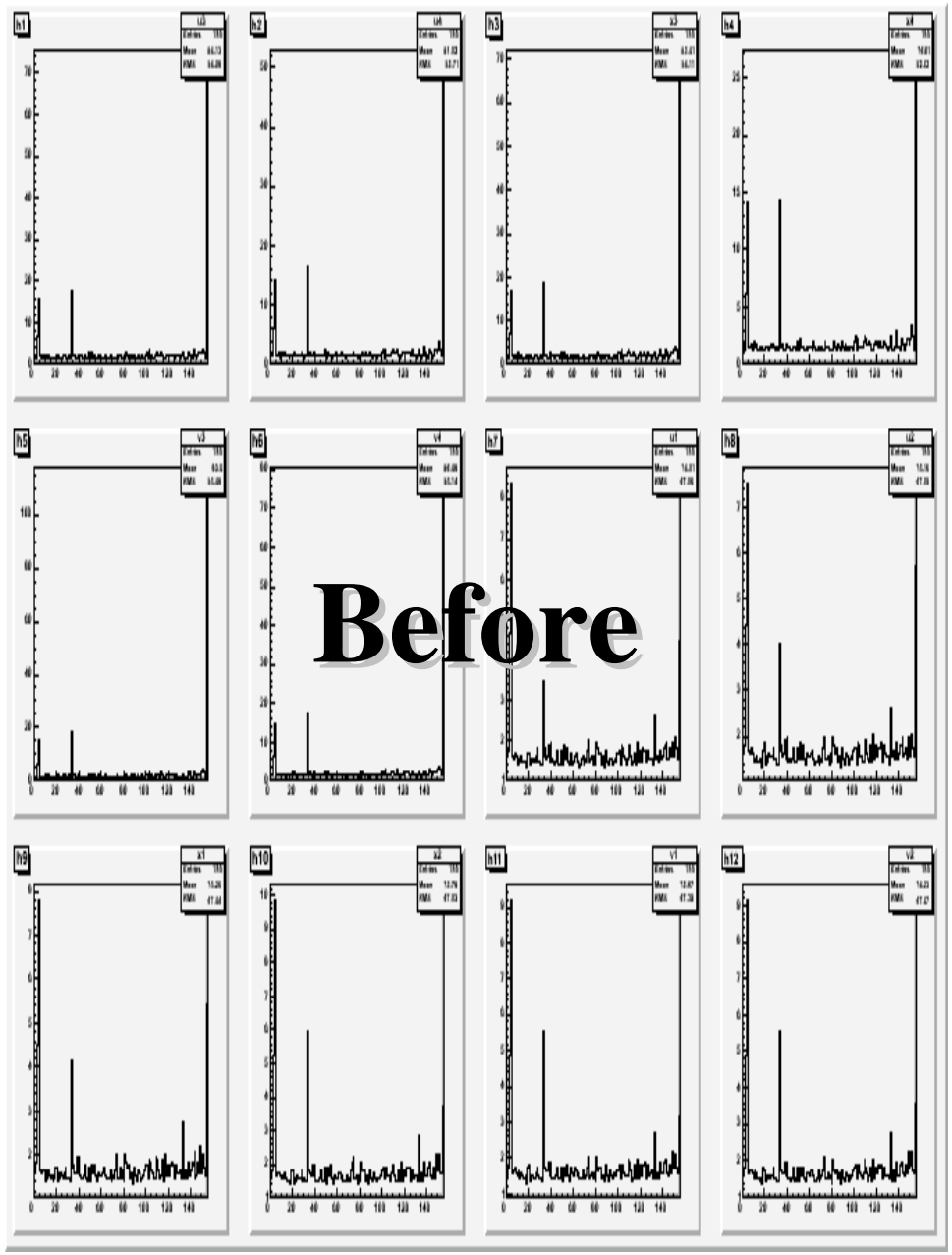
Wire Chamber Hit Pattern

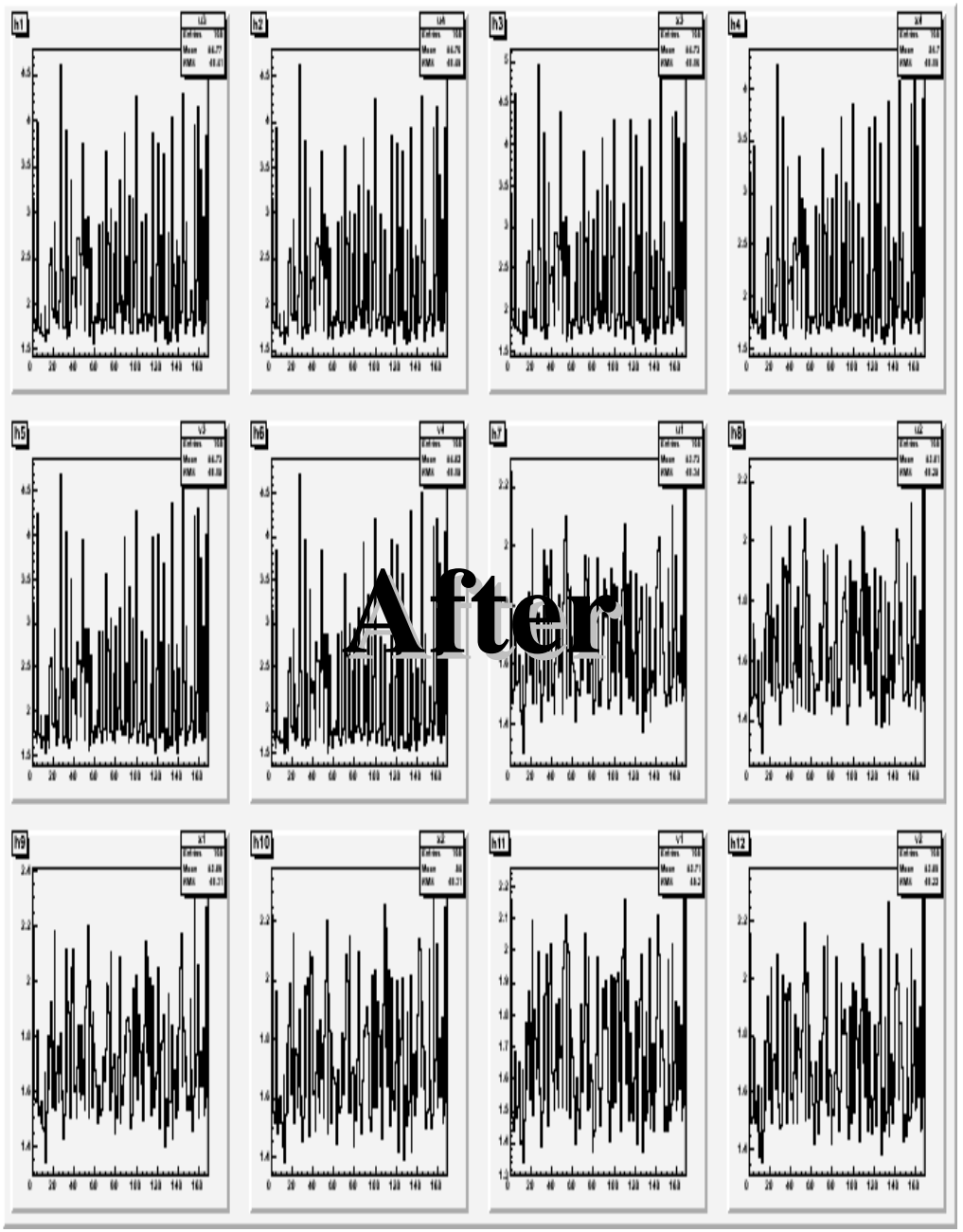
- In general good.
- Several mapping problems exist?
- Noise problem for several cards on both chambers
  - Cables can introduce noise to system when they are close to the power line.
  - Need to reduce threshold.
- The low voltage for level translator was too low (fixed now, Brad, Bill, et al.)

Before Fixing Power Supply

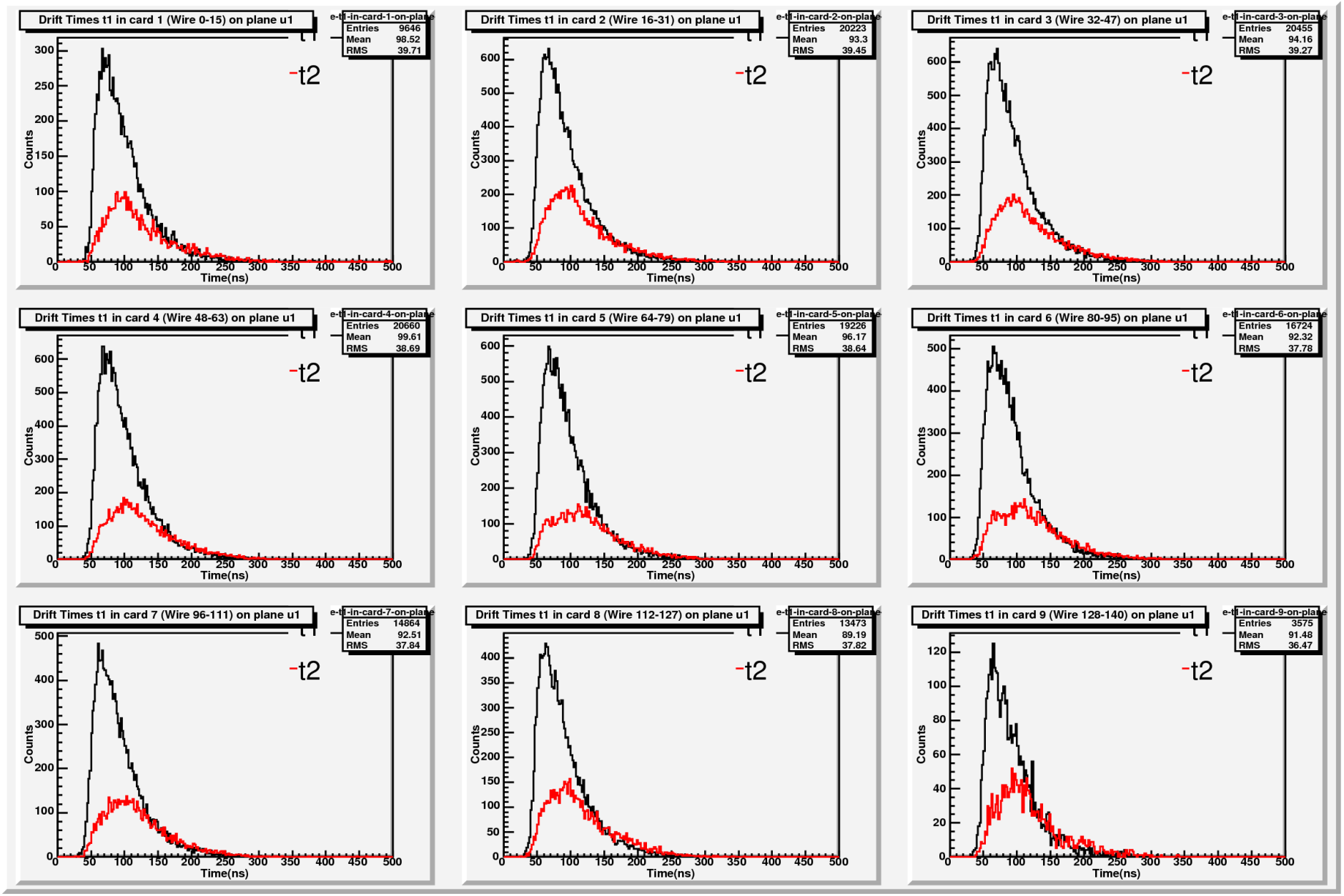


Time Dependent Noise

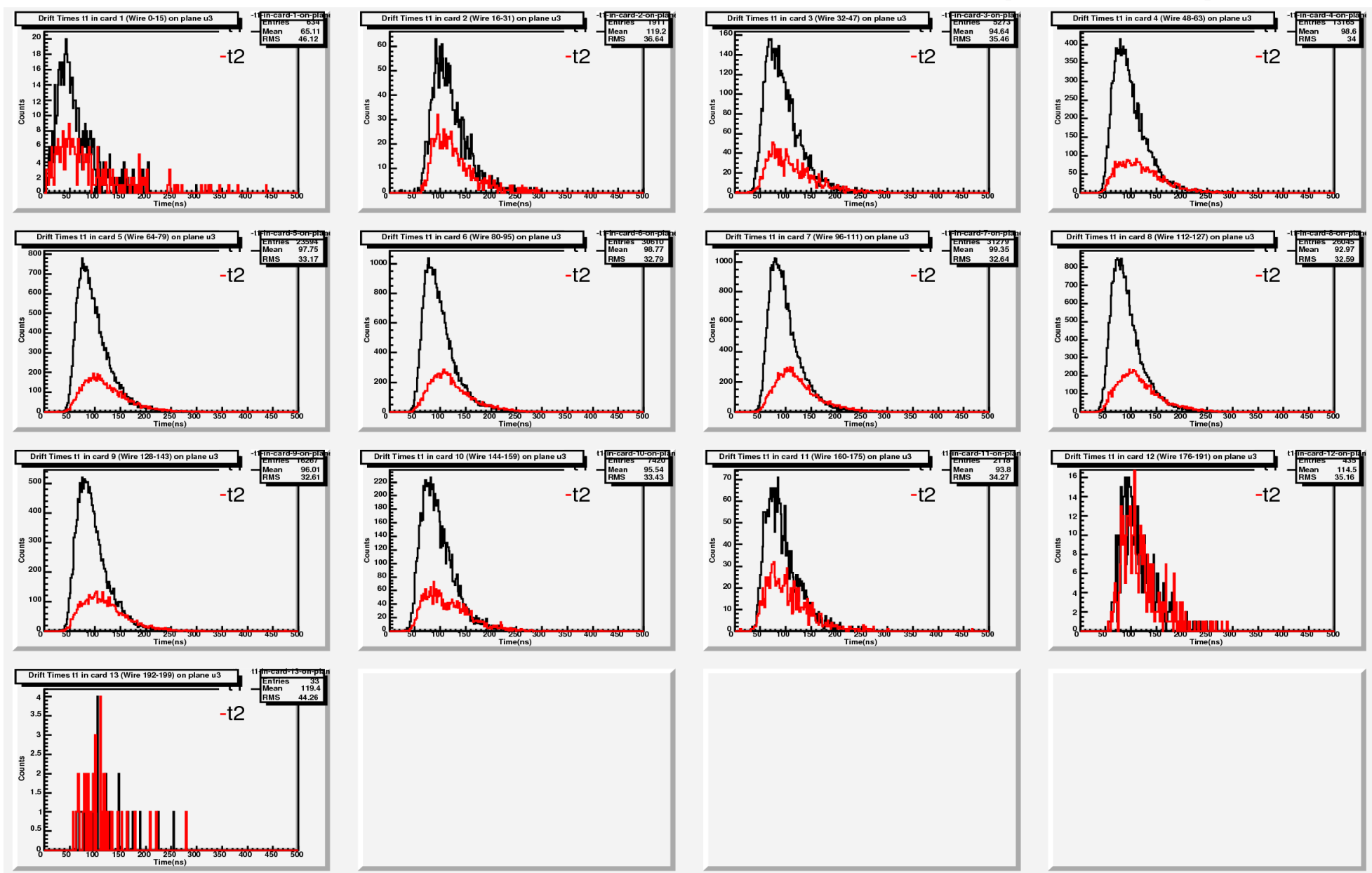




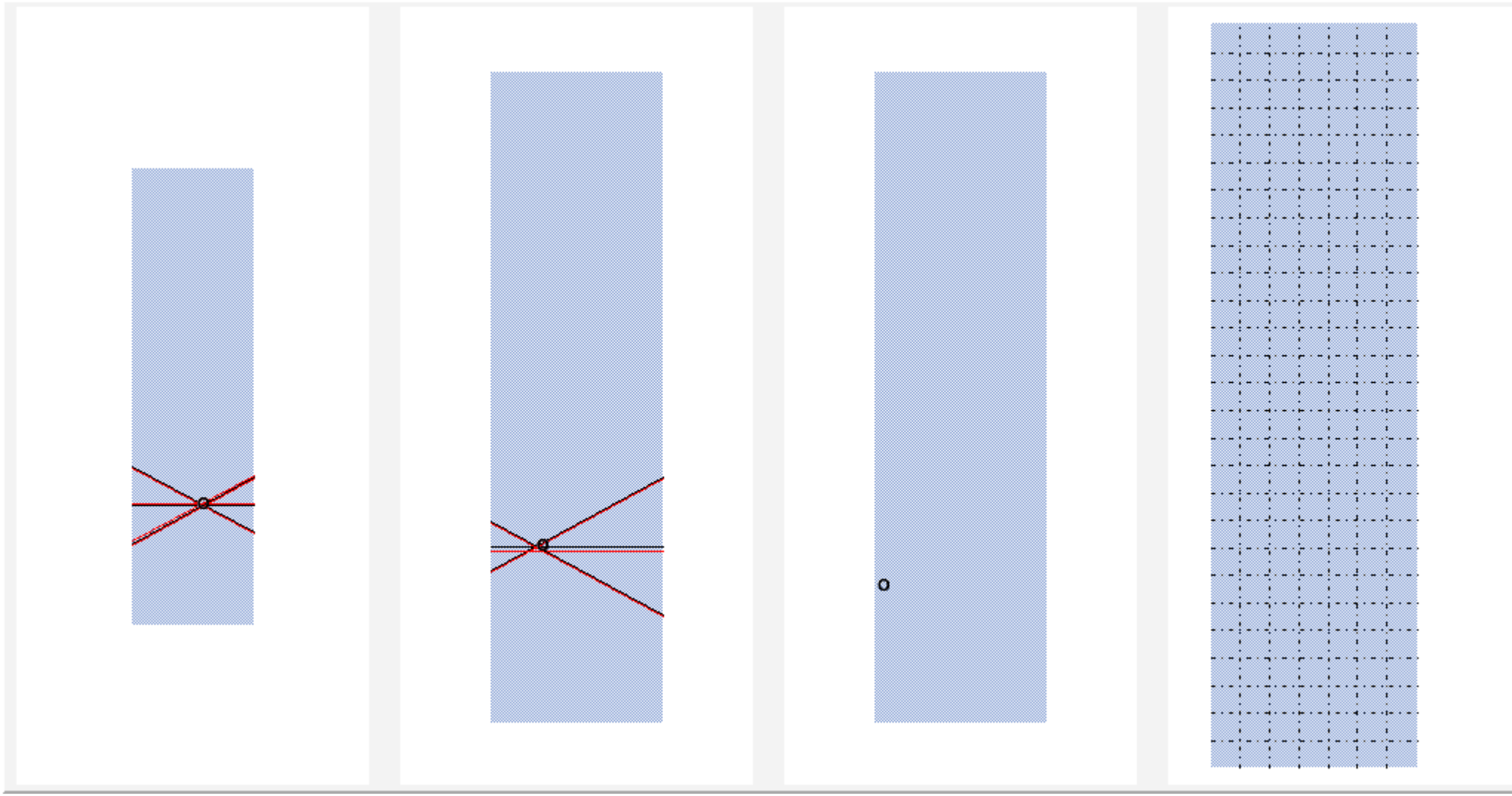
Drift Time is Fine (Ch1)



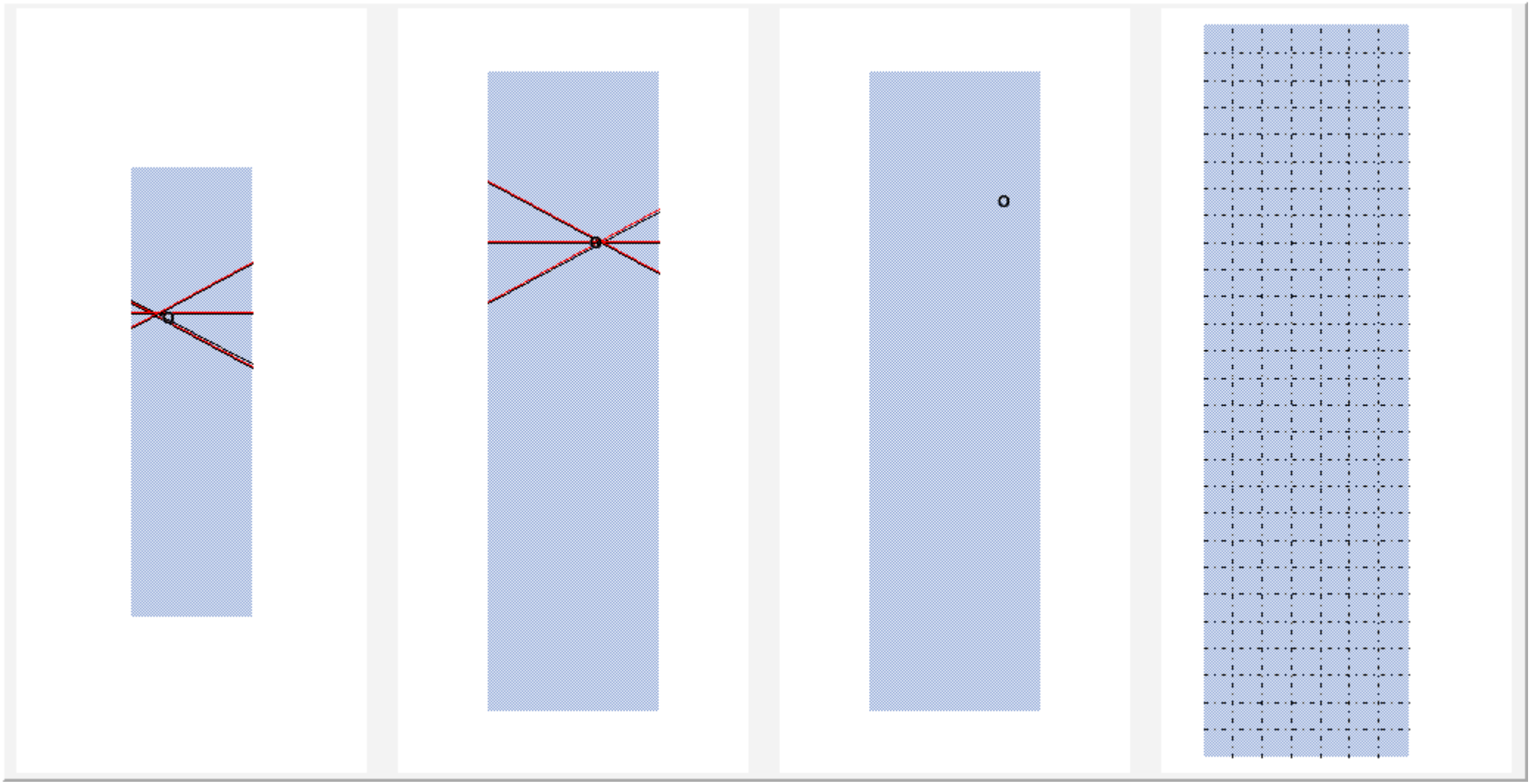
Drift Time is Fine (Ch2)



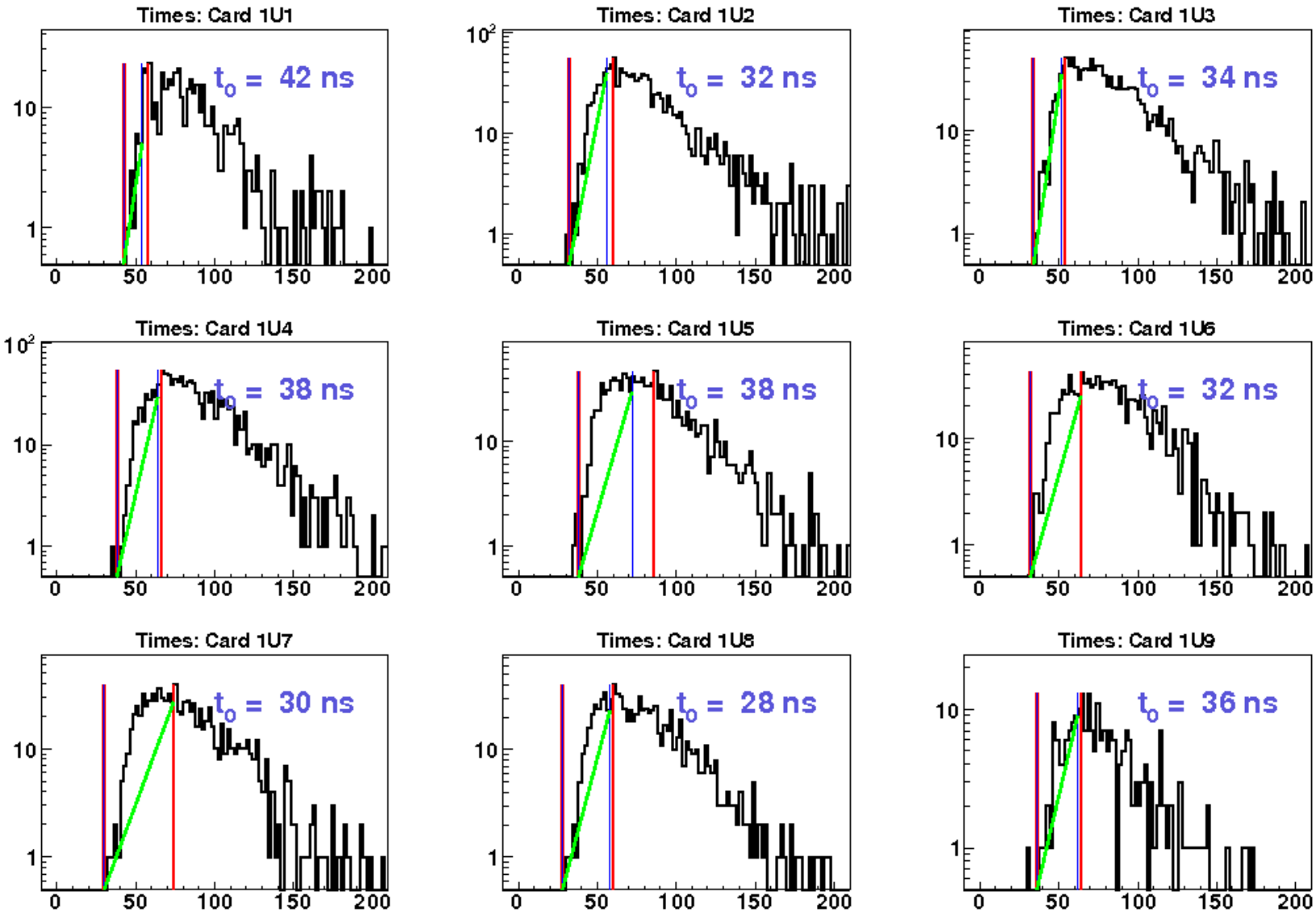
Can Find Track!



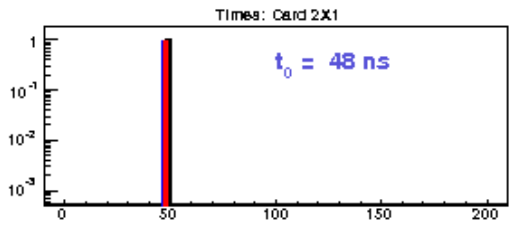
Can find Track!

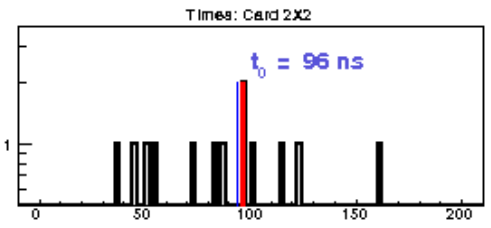


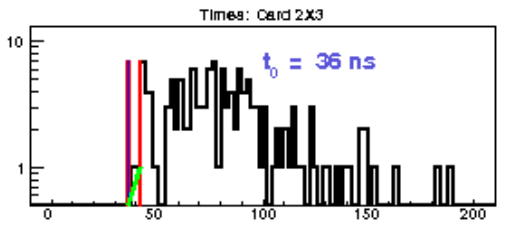
Timing offsets (Ch1)

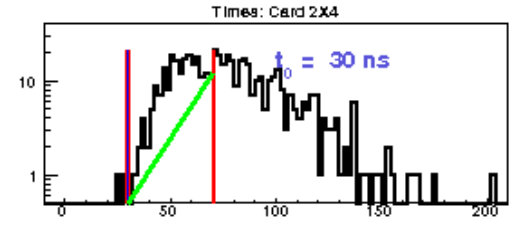


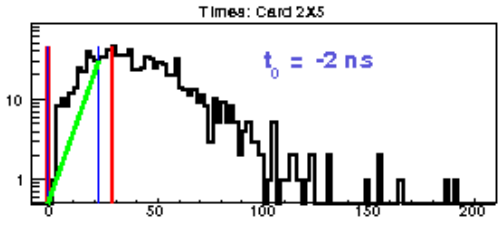
Timing offsets (Ch2)

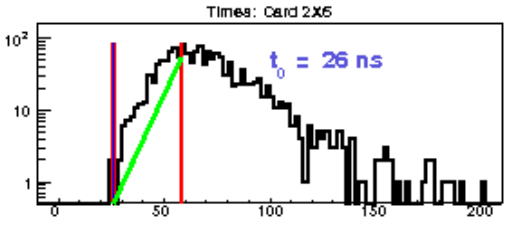


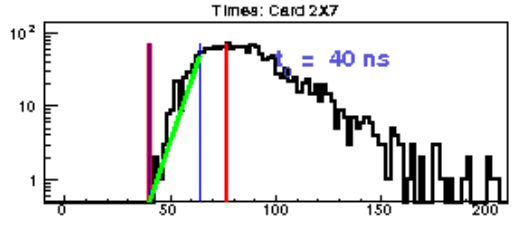


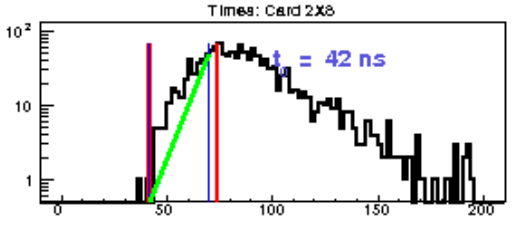


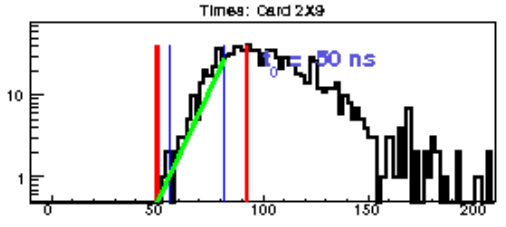


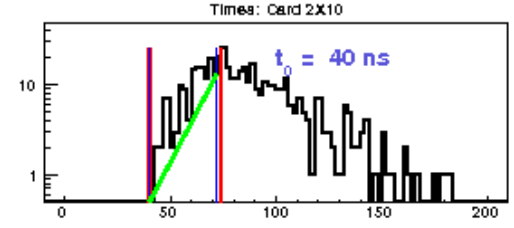


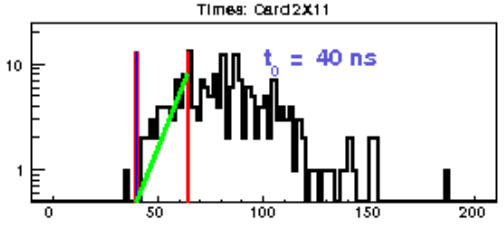


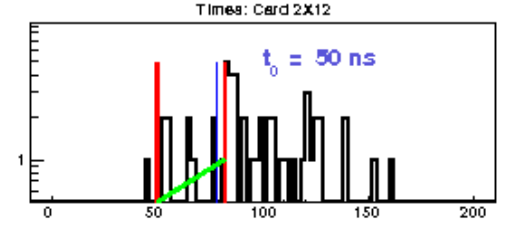


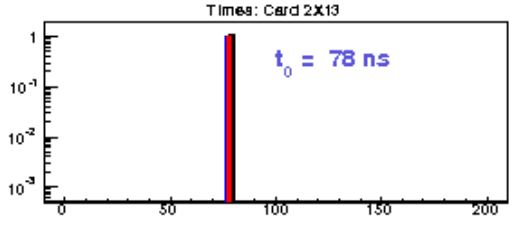






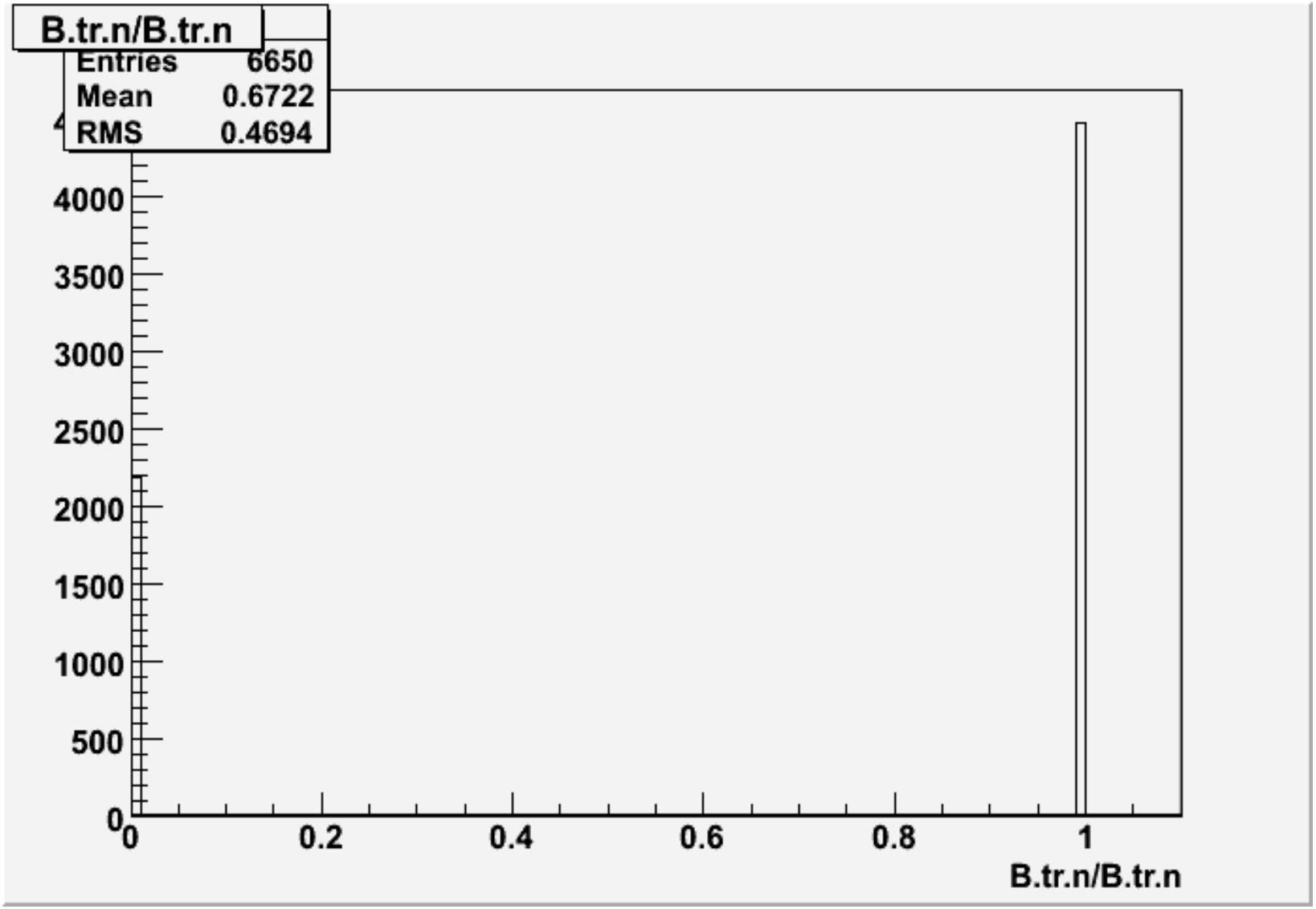






of Tracks Found!

- ~0.7 tracking efficiency



Problems

- Hardware:
  - Some mapping problem (cable connection)
  - Noise problem on electronics
- Software:
  - Geometry of two chambers
    - Position of chambers
    - Position of wires for different planes inside chamber
  - Mapping?

Summary & Future Plan

- We figured out the final mapping.
- Ch1+Ch2 are good on FASTBUS
  - Ch1+Ch3 worked before on VME
- Observe noise.
- Observe mapping problems.
- Figure out mapping problems
- Reduce noise further.
  - Lower threshold
- Need to figure out chamber position precisely.

Acknowledgment

- Kalyan and Brad
- All students who helped with cables.