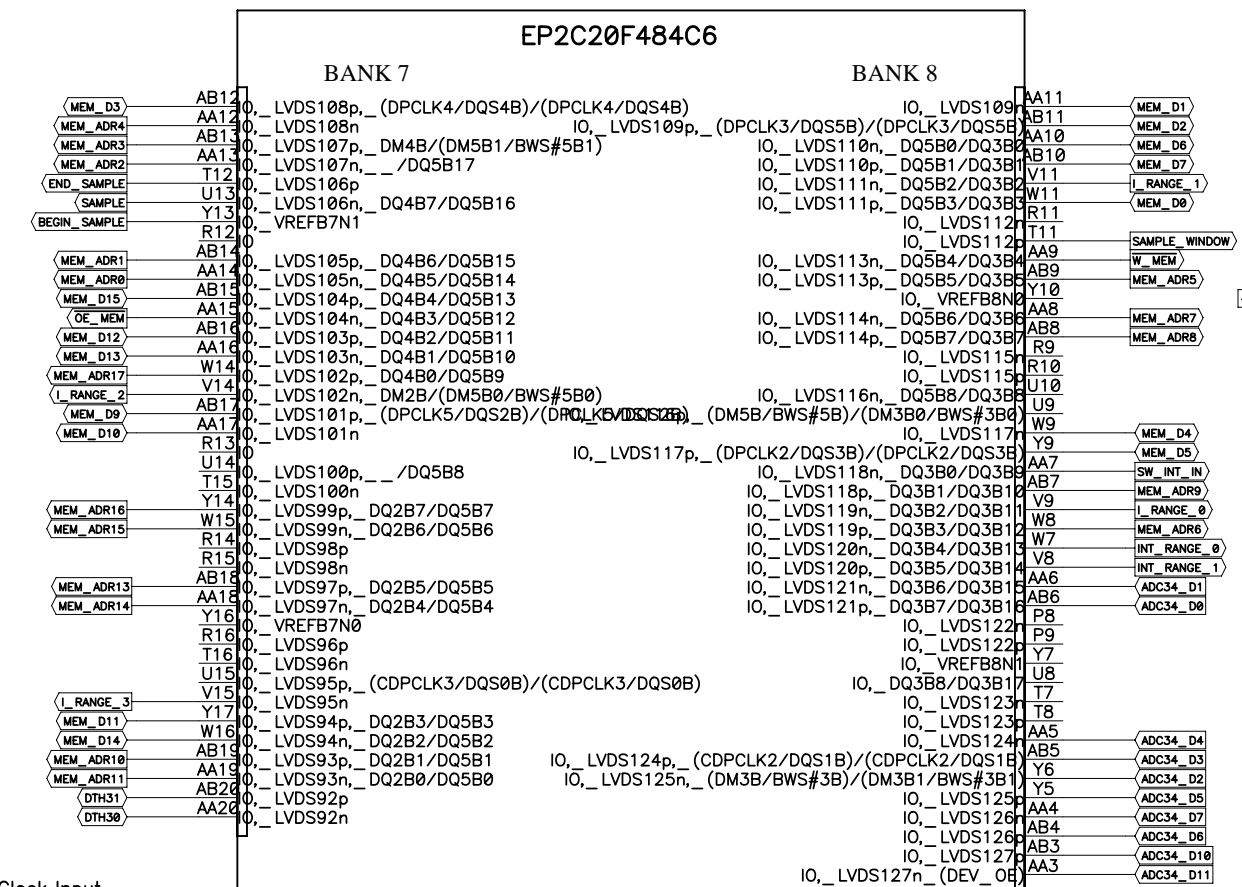
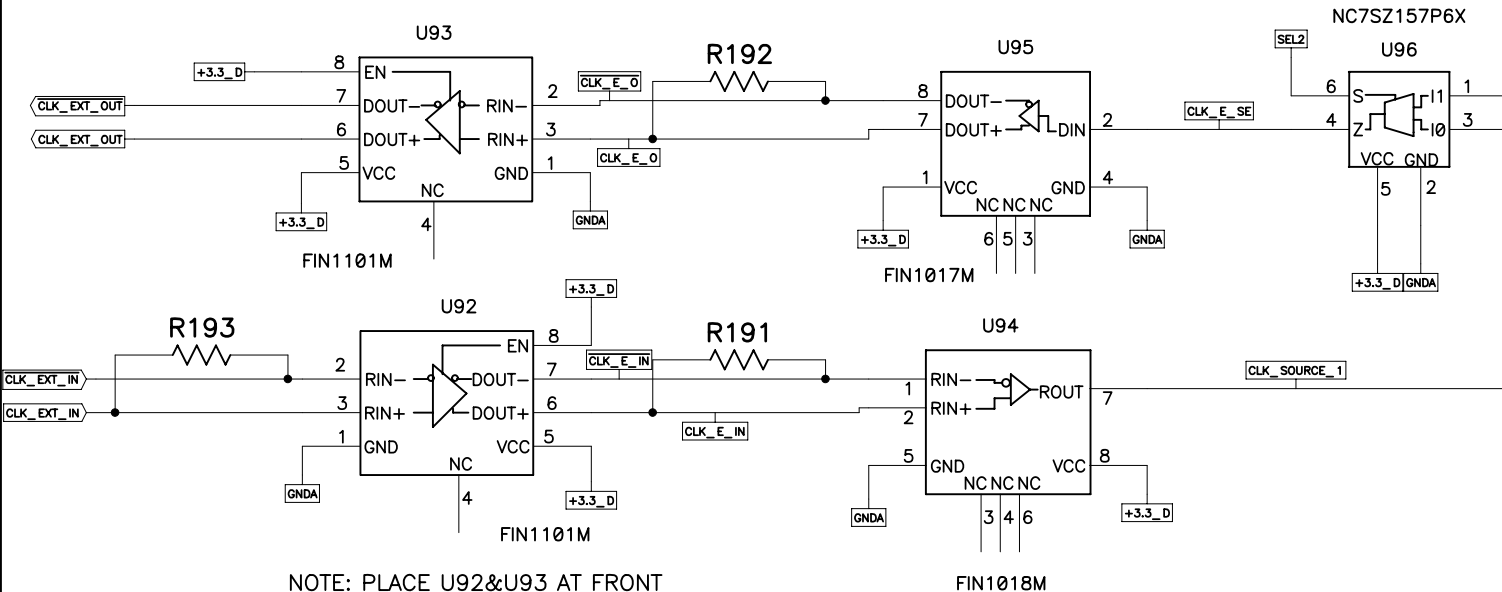
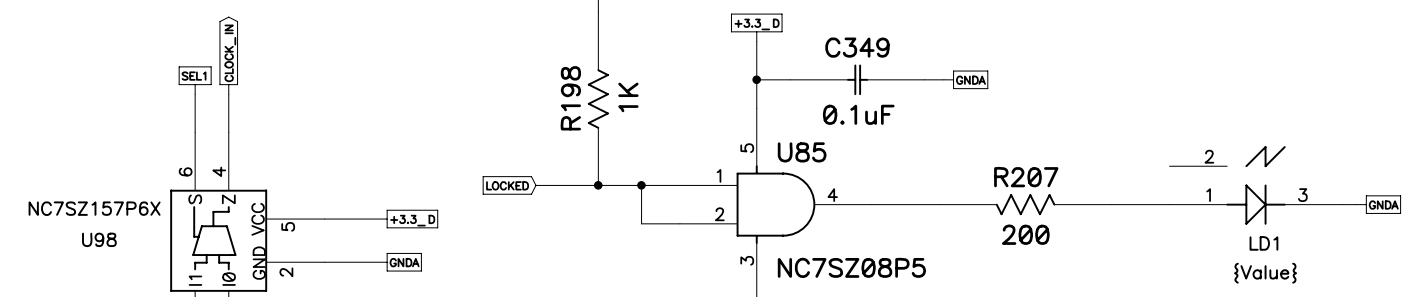
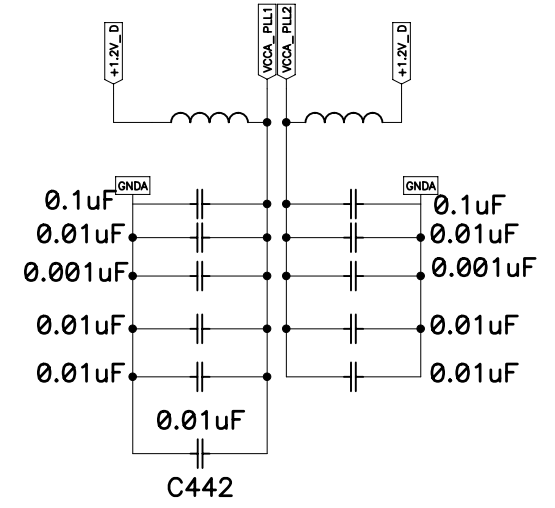
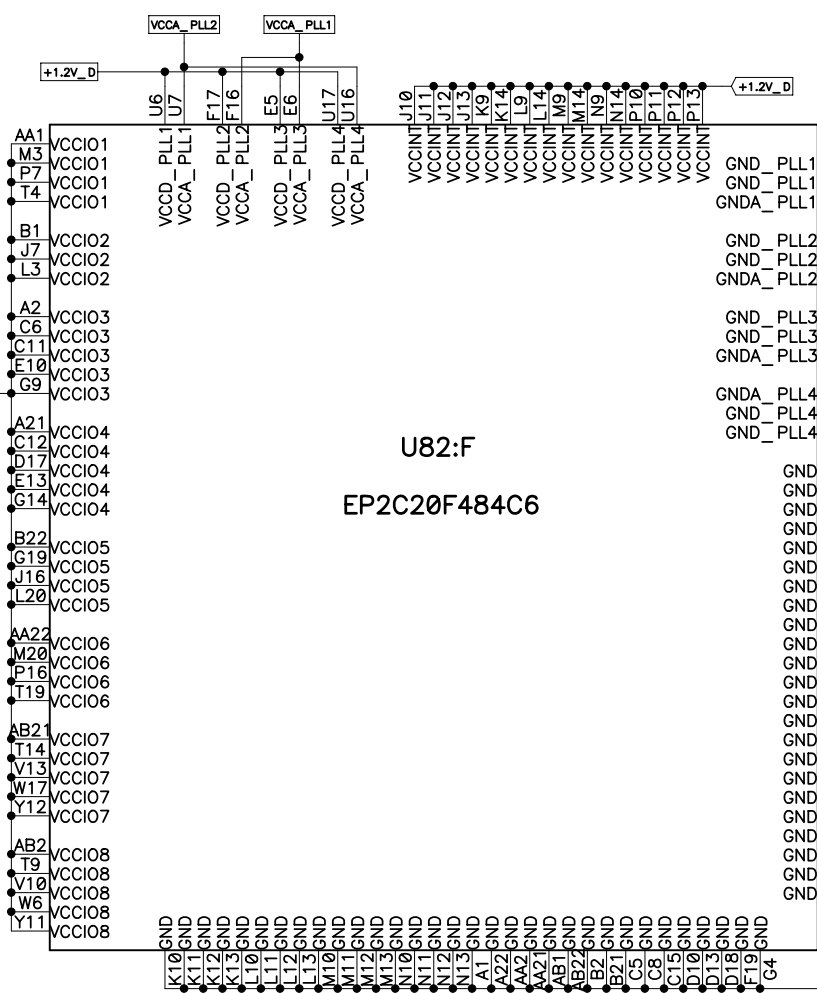
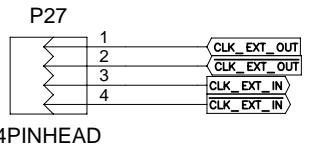


U82:D



Clock Input (Front Panel)
Clock Output (Front Panel)



NOTE: PLACE U92&U93 AT FRONT OF BOARD

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TITLE HIGH RESOLUTION 18-BIT ADC			
Hall A HAPPEX			
FJ Barbosa, E. Jastrzebski, J. Wilson			
FPGA			
SIZE	CAD I.D. NO.	DRAWING NO.	REV.
B		18-BIT_ADC_V2_1.SCH	
SCALE	SHOWN ON	SHEET OF	
		15	16



DWG. NO.

SH.

REV.