Tests of the PREX 18-bit ADCs

Brian Hahn
College of William and Mary

Robert Michaels, Fernando Barbosa, Edward Jastrzembski
Thomas Jefferson National Accelerator Facility

Krishna Kumar, Luis Mercado
University of Massachusetts

Richard Wilson
Harvard University

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I. INTRODUCTION AND SUMMARY

This report summarizes the tests of the PREX 18-bit ADC. See appendix A for a brief description of the ADC. The setup used for most of the tests is shown in fig 1. For some voltage-mode tests we used a pulser input or a function generator input.

At present we have a voltage-mode which accepts a voltage from 0 to +5V, and two current modes: a high-current mode and a low-current mode. The high-current mode is tuned to work at about 20 μA with minimum on-board gain settings, and the the low-current mode works at 1 μA. The higher current is where the Lumi detector PMTs work with optimal linearity, and the lower current is where we expect the PREX detector to operate.

In the following we use the notation of the first channel, see the circuit diagram (appendix A). The input goes across a resistor R159. Making R159 "big" is what gives us so-called voltage mode. The voltage then goes to a first stage amplifier. The gain of the first stage is controlled by two resistors R14 and R18. Converting between V-mode, low-I mode, and high-I mode is simply a matter of swapping these three resistors.

After the first stage amplifier the signal is converted to a current and subsequently this current is integrated. The conversion gain ("cg") is modified by on-board switches that selects how many resistors to put in parallel, and the integration gain ("ig") is controlled by a switch that selects capacitors in parallel.

It's important to know the source of noise, i.e. whether it comes from the board itself or from external sources. If the noise is minimized by increasing R159 while minimizing the cg and ig, then it is likely the noise comes from the board itself and probably from the switches that control cg and ig. (Note, we may easily remove these switches, perhaps ig would be a first candidate.) Indeed, in the first prototype board, these switches were observed to cause significant noise, and swapping these switches to newer, better rated switches has helped.

On the other hand, if the configuration has a maximum R159 and minimum cg and ig, *and* if small variations in cg and ig lead to no noticeable change in the "pedestal noise in ppm" (defined below), then the noise is presumably due to an external source. This seems to be the case at present, to a good approximation. There appears to be a 45 ppm noise from outside the ADC board, in the PMT test circuit (fig 1).

This latter conclusion is corroborated by the fact that the Qweak ADC sees a 45 ppm noise in the same setup, as explained below.

II. PEDESTAL NOISE

The term "pedestal noise" has been used loosely to mean different things, so we start with some definitions. Each definition is a quantity based on a pair of events.

TABLE I: **Open-Circuit Pedestal Difference (HAPLOG 1464,5)**

Gains (Int, Conv)	Voltage Mode (chan)	High-Current (chan)	Low-Current (chan)
3, 0	3.2	3.5	4.2
3, 1	3.7	4.4	6.9
3, 2	4.4	5.4	9.7
2, 0	3.6	4.2	6.2

TABLE II: **Pedestal Differences in Voltage Mode (HAPLOG 1464,5)**

Gains (Int, Conv)	Avg ADC (10^3 chan)	Pair Diff (chan)	Ped Diff (ppm)
3, 0	61.3	5.7	46
3, 1	123	10.3	43
3, 2	177	15.3	43
2, 0	97	8.4	43

- *Open-Circuit Pedestal Difference* = the pair-difference in ADC values when nothing is plugged in. Units are in channels.
- *Pedestal Difference in channels* = the pair-difference in ADC values when a signal is plugged in. Units are in channels.
- *Pedestal Difference in ppm* = The pair difference in channels divided by the sum of *observed* ADC values, this fraction expressed in ppm.
- *Extrapolated Pedestal Difference in ppm* = The pedestal difference in channels divided by 1.5× the maximum ADC value.

The idea of the extrapolated pedestal difference is to divide by $2 \times ADC$ where $ADC \sim \frac{3}{4}$ of the maximum ADC value. Since $\frac{3}{4} \times 2^{18} \sim 200$K, we normally use 200K as the ADC value. The extrapolated pedestal difference is one way to explain the implication of the open-circuit pedestal difference. For example, a 3 channel open-circuit pedestal difference implies an 8 ppm noise floor. Note, however, that the "extrapolated pedestal difference" can lead to misleading conclusions when discussing the noise of a system involving components outside the ADC.

The ADCs have 64 settings of gain using two knobs called "integrate gain" and "conversion gain". This gives us a factor of ∼20 in range. The integrate gain ranges from 3 to 0, with 3 being the lowest gain. The conversion gain ranges from 0 to 15 with 0 being lowest. It was found that the lower gain settings minimize the "pedestal difference in channels" but they don't change very much the "pedestal difference in ppm". The pedestals themselves depend on these gains but can be adjusted with an onboard DAC; the pedestals are positive and $\sim 0.5\%$ of the full-range. In most of these results I haven't subtracted the pedestal properly (sorry) but it won't change the answers much (typ. ∼2 ppm shift when you don't subtract pedestal). Table I shows the open-circuit pedestal differences for various gain settings. Table II shows the pedestal differences in ppm for voltage-mode, and tables III and IV are the same for low-current and high-current mode. All these results use the test setup in fig 1. A plot of typical results is shown in fig 2, while fig 3 shows how the noise scales with averaging. The voltage-mode used the Qweak ItoV which has a conversion of $V = 10^6 \times I$, so that a 1μA PMT current becomes a 1 Volt signal. There was some concern that the

TABLE III: **Pedestal Differences in Low-Current Mode with 1μA (HAPLOG 1464,5)**

Gains (Int, Conv)	Avg ADC (10^3 chan)	Pair Diff (chan)	Ped Diff (ppm)
3, 0	41	5.4	
But if we	increase to 2.85 μA	by increasing PMT HV:	
3, 0	95	7.5	39
Back to	1 μA		
3, 1	81.7	9.0	55
3, 2	118	12.7	54
2, 0	65	7.9	61

TABLE IV: **Pedestal Differences in High-Current Mode with 20μA (HAPLOG 1464,5)**

Gains (Int, Conv)	Avg ADC (10^3 chan)	Pair Diff (chan)	Ped Diff (ppm)
3, 0	106	7.6	35
3, 1	211	14.8	35

TABLE V: **Pedestal Differences : Qweak vs HAPPEX ADC**

	QWeak ADC		—	HAPPEX ADC		—
Voltage	Avg ADC (10^6 chan)	Pair Diff (10^3 chan)	Ped Diff (ppm)	Avg ADC (10^3 chan)	Pair Diff (chan)	Ped Diff (ppm)
No input	-4.6	3.96	2.2	1.52	3.3	8
1.55 V	256	22.1	43	62.7	5.8	46
2.69 V	542	45.8	42	130	11	42
4.8 V	945	76.8	41	245	19.7	40

ADC itself produces noise in this circuit, so we repeated the measurements using the Qweak ADC, see table V. The same setup (fig 1) is used with ItoV.

The conclusion of this study is that there is a noise of approximately 30 to 50 ppm in the PMT circuit in fig 1 which is seen by both Qweak and HAPPEX 18-bit ADCs, and by all modes of the HAPPEX ADCs. (We haven't tried the 16-bit ADCs in this setup recently. I'm too tired ... does somebody want to ?) To remind you, PREX expects a counting statistics noise of 125 ppm, so adding a 50 ppm noise in quadrature increases this to 135 ppm. If we run with oversampling by 10, each sample has a counting statistics noise of 400 ppm, so an extra 50 ppm noise would be negligible.

As discussed in the Introduction, the noise appears to be mostly external to the board at this time and with this test setup. However, it would probably be a good idea to remove the integrate gain but leave some conversion gain (factor of $\sim$5). Further gain adjustment can be achieved by swapping the resistors R159, R14, and R18.

III. PERFORMANCE TESTS

In addition to the pedestal noise studies in the previous section, the following performance tests were done.

1. *Linearity:* In V-mode or I-mode the input signal can be measured with 1% accuracy and the ADC response is within 1% of expectation.
2. *Differential Linearity:* The 18-bit ADC is expected to have some differential nonlinearity manifested by a reduced probability of a hit in some bit locations, however no missing bits – i.e. the probability is never zero. We have observed this, and the DAC noise alleviates it as expected, see fig 4. Using DAC noise with a sine wave input, a smooth secant curve distribution is observed, see fig 5. Likewise a square wave input with variable duty cycle gives the expected result, see fig 6.
3. *Crosstalk:* With a large signal on one input, no variation is seen on an adjacent input, see fig 7. Another way to observe this, in either I-mode or V-mode, is to turn on the HV in the test setup (fig 1) and note that as the signal changes from pedestal to 200K, an adjacent channel does not change.

IV. RECOMMENDATION

We recommend to purchase 15 units of the 18-bit ADC to be ready by Christmas 2008. The I-mode and V-mode can be easily converted, but we'll start off with 9 V-mode, 3 low-I mode and 3 high-I mode boards.

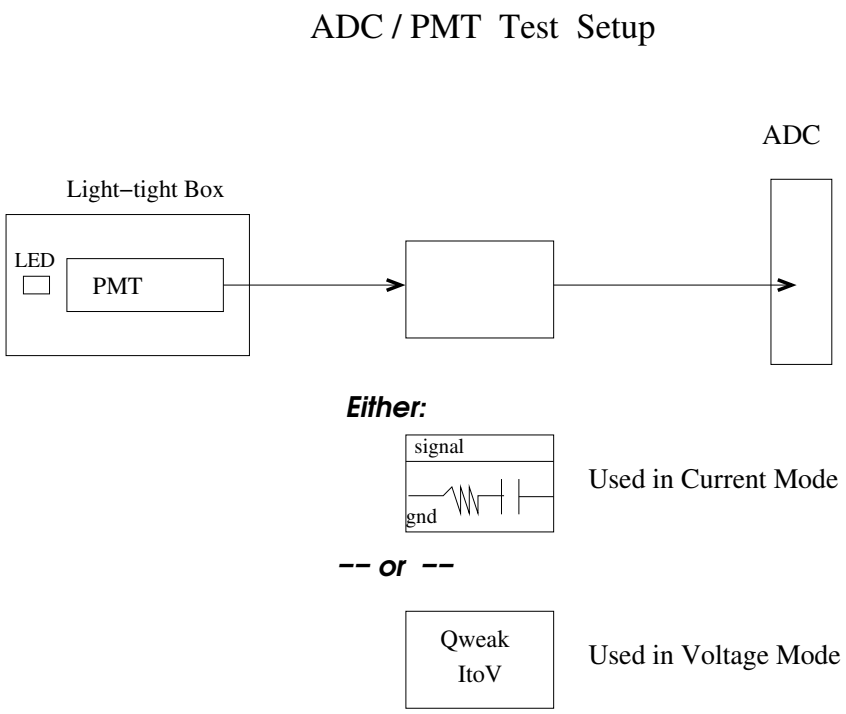

FIG. 1: Test setup using the PMT and light source (LED).

APPENDIX A: Purpose and Design of ADC

Parity experiments require high precision measurements of signals integrated over a helicity pulse (33 msec), or over a fraction as small as 1/20 of a helicity pulse, this latter case is called "oversampling". The signals consist of PMTs from detectors (current sources) or voltage levels (voltage sources) from various devices such as beam position monitors (BPM) or beam current monitors (BCM). The reason we integrate is that in order to see the tiny parity violating signal in a reasonable amount of beam time the event rate must be far too high (e.g. gigaherz range) to count individual events, so we must integrate the signals. The ADCs are designed to achieve high resolution (18 bits) with small nonlinearity, see specifications listed in table VI as well as the detailed specification document available online:

http://hallaweb.jlab.org/parity/prex/adc18/prex_adc18_spec.ps

The circuit diagrams are available online at

http://hallaweb.jlab.org/parity/prex/adc18

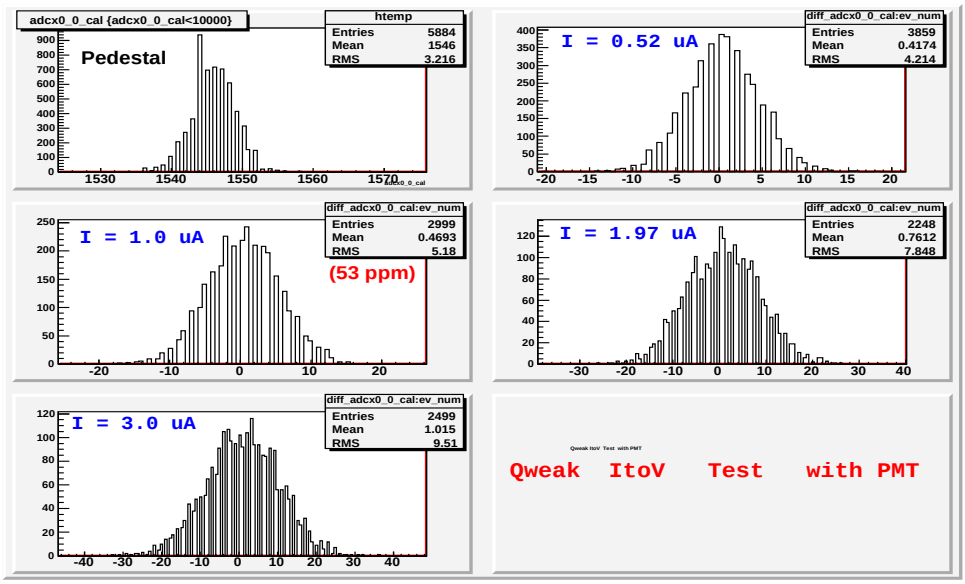

FIG. 2: The pedestal differences with various amounts of current from the PMT in the setup in fig 1, the ItoV box and the voltage-mode ADC. The upper left case is with nothing plugged into the ADC. The 53 ppm noise at 1 μA is with proper pedestal subtraction. (HAPLOG 1457)

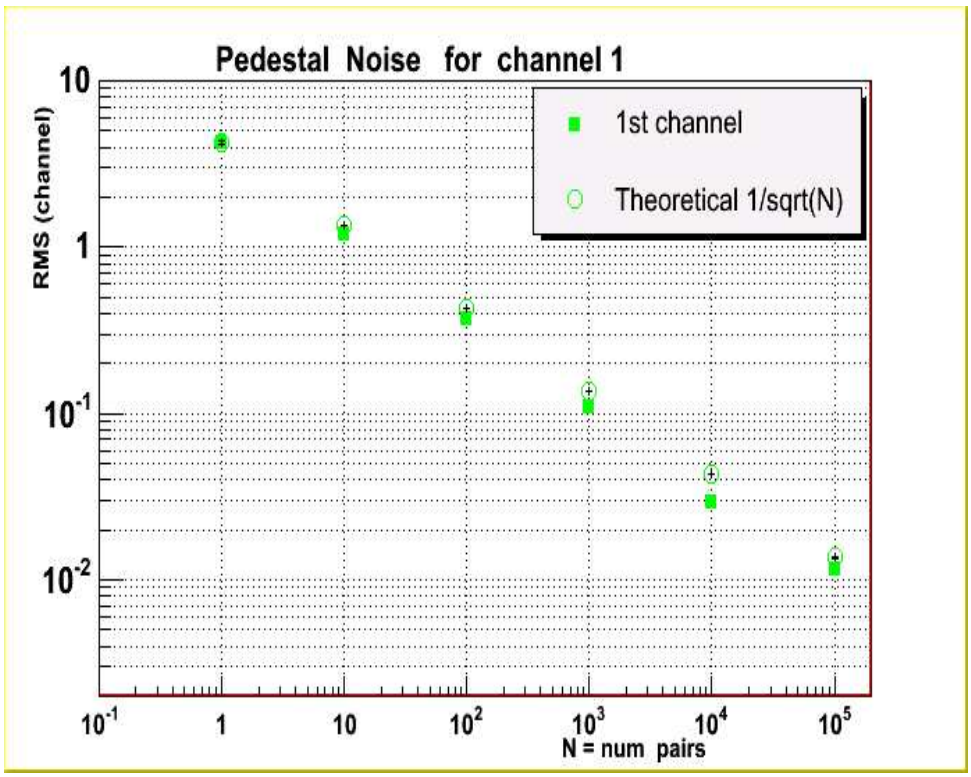

FIG. 3: The pedestal noise is averaged over different periods time (number of samples) as compared to $1/\sqrt{(}N)$ scaling.

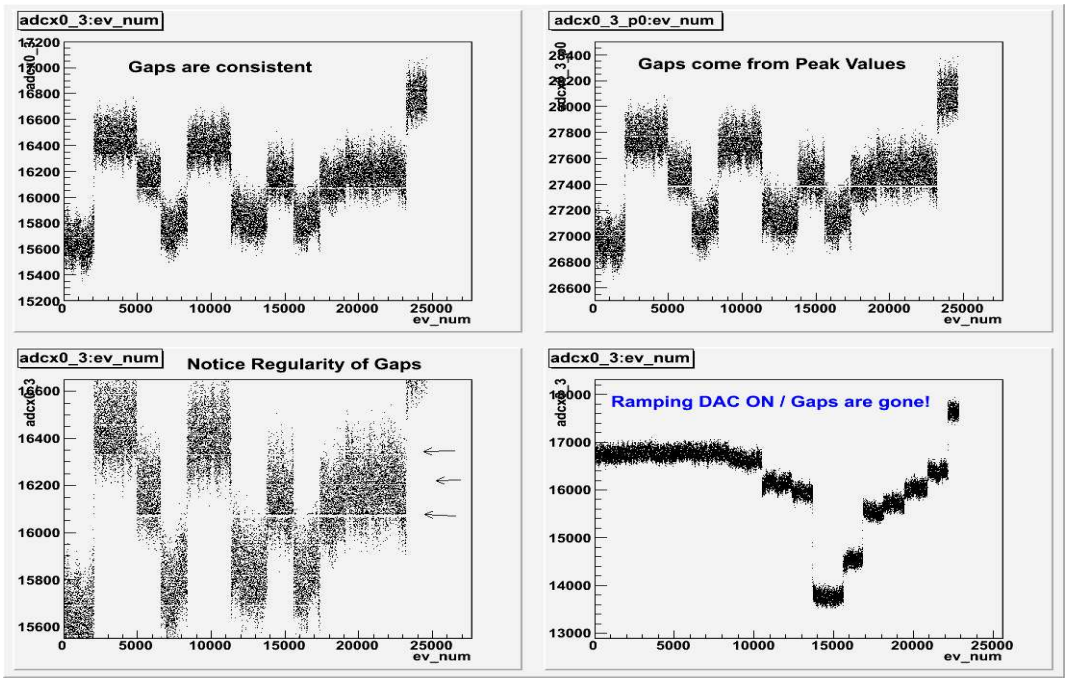

FIG. 4: Effect of DAC noise on eliminating differential nonlinearity (the gaps). (HAPLOG 1177, see also 1176)

TABLE VI: **ADC Specification**

Quantity	Specification
Bit Resolution	18 bits
Rate Capability	10 kHz
Input Signals	PMT signals (I) or Voltages
Input Polarity	One sign, but reversible
Gain Adjustment	64 Steps, factor of 20
Max Input (V-mode)	5 V
Min Input (I-mode)	0.2 μA
Differential Nonlinearity	$\leq 2 \times 10^{-5}$
Integral Nonlinearity	$\leq 5 \times 10^{-5}$
Pedestal Noise	$\leq 100\mu$Volt or $\leq$2.5 ADC chan FWHM
VME Form Factor	9U with J1-J2 in lower 2/3

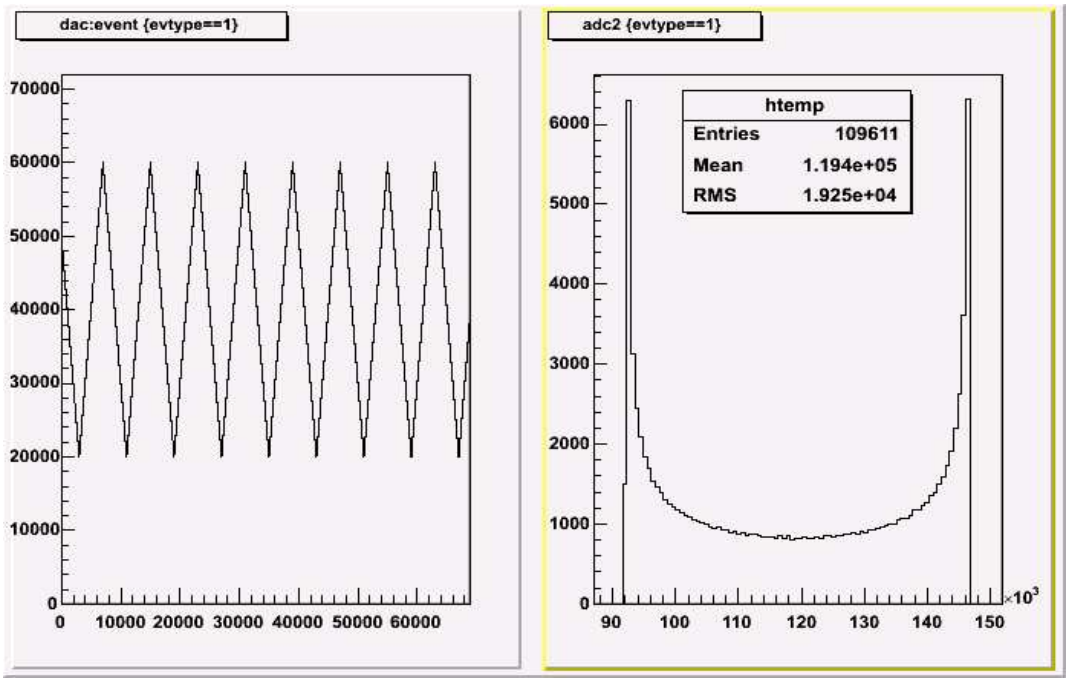

FIG. 5: A sine wave input to a Voltage-mode ADC is smoothed out by DAC noise (left) resulting in a smooth ADC distribution (right). (HAPLOG 1043)

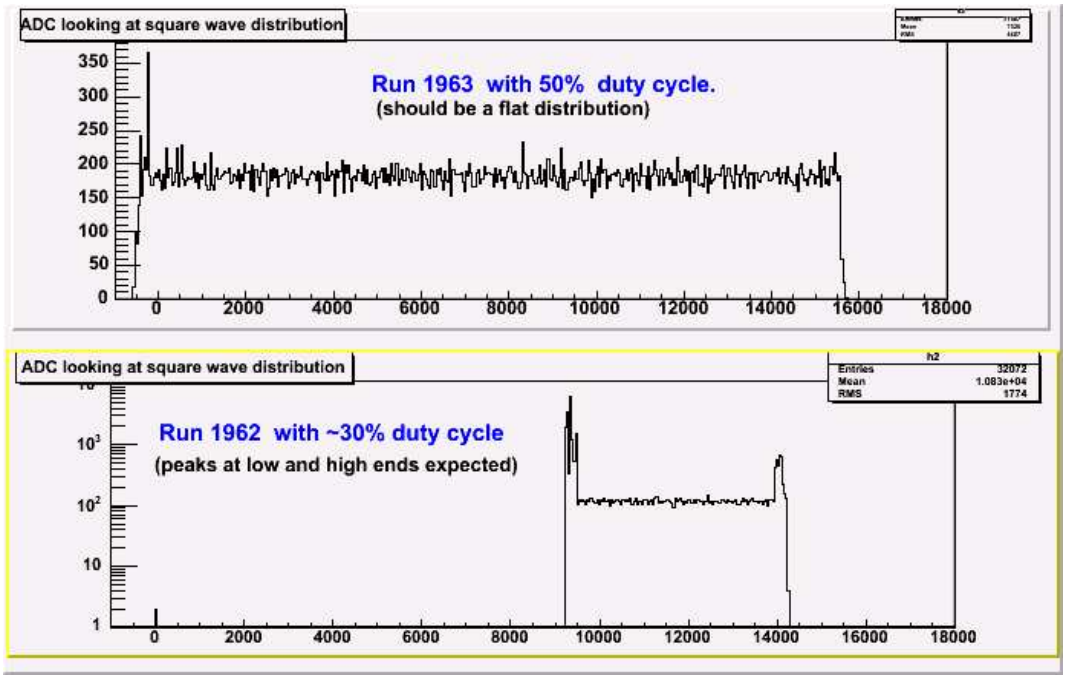

FIG. 6: A square wave signal input to a Voltage-mode ADC produces a flat distribution and produce the expected ADC spectrum depending on duty cycle. (HAPLOG 1030)

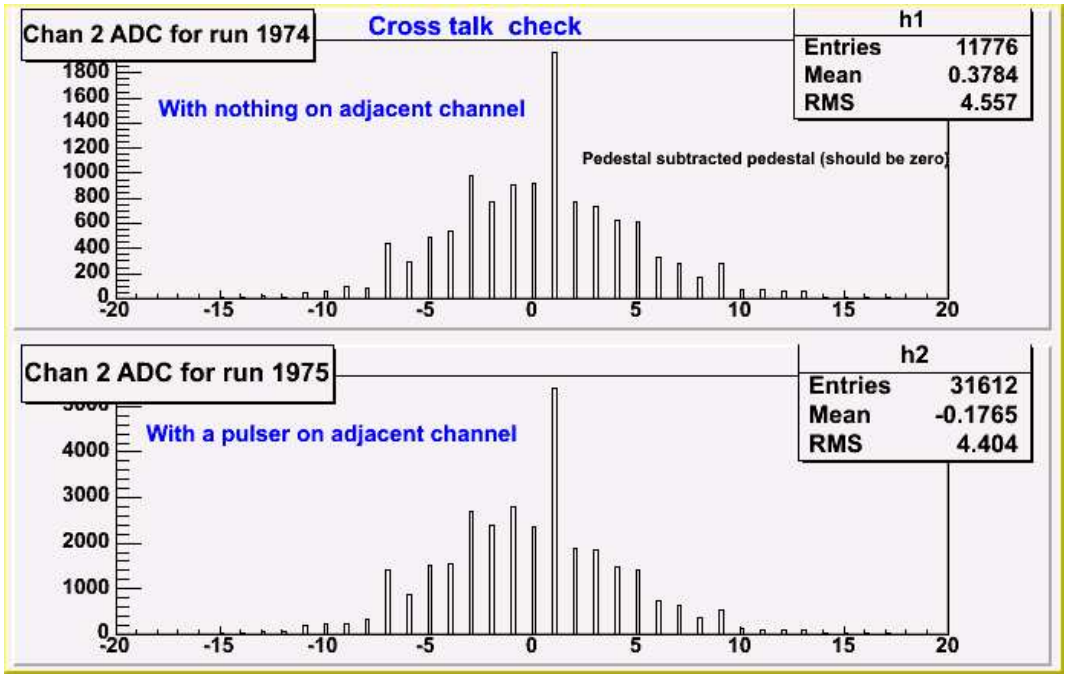

FIG. 7: Study of crosstalk between adjacent channels. A pulser on one channels has no effect on the pedestal of another. (HAPLOG 1037, see also 1031.)