FADC for Hall A Moller

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I INTRODUCTION

This is a specification for a FADC for the upgraded Møller DAQ in Hall A. We think we can use the existing JLab design with some modifications to the FPGA to produce a trigger. The DAQ will run a standard CODA VME one-crate setup.

We will need 1 FADC units of 16 channels plus a spare in about 4 months from now.

II APPLICATION

The Hall A Møller polarimeter detects electrons scattered from a polarized iron foil. Since there are two electrons in the final state, the detector consists of two arms. Each arm contains 4 calorimeter blocks and 4 scintillator counters[1]. In one arm, the calorimeter blocks are arranged in a column. The electrons are swept along the column by a dipole magnet and their energies depend on the position. However, the HV on the PMTs are tuned to equalize the calorimeter outputs from all 4 blocks. The electron signal can be shared between two adjacent blocks. Typically, only one scintillator counter in the column is hit.

The maximum expected rates above the thresholds used are[2]:

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1) At the moment only one scintillator counter is installed in each arm.
2) This is a factor of 3 increase with respect to the present polarimeter running.

- Calorimeter: 1 MHz per arm;
- Scintillators: 4 MHz per arm;
- Coincidence of both arms: 400 kHz.

With the present setup, the calorimeter signals arrive at an analog fan-out unit, the analog sums from the columns as well as the signals from the scintillation counters pass through discriminators, and various coincidence signals are formed with a PLU. The coincidence rates are recorded with scalers, read out every helicity cycle at 30 Hz. Additionally, the raw signals are measured with an ADC and a TDC units, triggered by a selected combination of the pulses from the PLU. The first 3-10 of such events per helicity cycle were recordered, in order to make sure that the data are good, but without overloading the DAQ system. The Møller asymmetry can be measured only with the scalers, since the statistics of the ADC/TDC events is 100-1000 times shorter than needed for that. The "helicity triggers" contain additional information: scalers for a beam current monitor (BCM, VtoF), a 100 kHz pulser in order to measure the helicity window, encoders for the target positions etc. All the triggers contain the trigger info, the helicity state and the QRT state, recorded via the TIR input registers.

One 16-channel FADC unit might be able to replace nearly all the electronics we are using now. In addition, it would allow to reduce the systematic errors by:

- measuring the asymmetries using the full events;
- analyze the pile-up effects and compensate for them.

The implementation must include:

- making logical signals when combination of the input signals exceed certain thesholds;
- writing out the FADC "event" data using a logical signal for the trigger with a certain prescaler, at a rate up to the maximum rate allowed by the existing FADC systems (160 kHz);
- making internal scalers in the FADC unit counting the coincidence signal; the scalers must be read out at every helicity cycle;
- the readout should include the "event triggers" (< 160 kHz) and the "helicity triggers" (30-2000 Hz), both should additionally contain the helicity bit and the QRT bit;
- the "helicity trigger" readout should include additional scalers/ADC for the BCM, pulser, BPM, encoders etc.

III LOGICAL SIGNALS

The input signals are typically > -2 Volts and 40 nsec wide with a fall time of 5 nsec.

Let P_i^j be the calorimeter PMT data for samples j and ADC input channel i, and let S_i^j be the scintillator data. The data would be summed over 2 samples $j = 1, 2$ because the signals will be aligned in time sufficiently well that they should peak within adjacent 4 nsec windows. It's conceivable we may pick 4 samples to sum over, but we'll assume 2 here. Note, it isn't necessary to use 2 for the scintillator; we can use one sample for that.

We will need to set two programmable parameters: threshold_1 and threshold_2 in order to build logical combinations:

- **CL** $= \sum_{i=1,4} \sum_{j=1,2} P_i^j \geq \text{threshold}_1$
- **CR** $= \sum_{i=5,8} \sum_{j=1,2} P_i^j \geq \text{threshold}_1$
- **SL** $= (\sum_{j=1,2} S_1 \geq \text{threshold}_2)$ .OR. $(\sum_{j=1,2} S_2 \geq \text{threshold}_2)$ .OR. $(\sum_{j=1,2} S_3 \geq \text{threshold}_2)$ .OR. $(\sum_{j=1,2} S_4 \geq \text{threshold}_2)$
- **SR** $= (\sum_{j=1,2} S_5 \geq \text{threshold}_2)$ .OR. $(\sum_{j=1,2} S_6 \geq \text{threshold}_2)$ .OR. $(\sum_{j=1,2} S_7 \geq \text{threshold}_2)$ .OR. $(\sum_{j=1,2} S_8 \geq \text{threshold}_2)$

The trigger to read out the FADC raw data should be a mixture of the coincidence and singles:

- CL.AND.CR prescaled from 1 to at least 1000
- CL prescaled from 1 to at least 1000
- CR prescaled from 1 to at least 1000

The prescaling factors as well as the thresholds should be easily programmable.

The triggers will initiate a readout of the FADC. Our understanding is that the FADC can interrupt the cpu, so it acts like a TIR. It is desirable to have the above three triggers be separate trigger types.

A On-Board Scalers

Additionally, it would be useful if the FPGA runs a kind of a scaler, counting

- CL.AND.CR
- CL.AND.SL
- CR.AND.SR
- CL.AND.CR.AND.SL.AND.SR
- CL.AND.CR.AND.(SL.AND.SR delayed>100ns)

These scalers are to be read out by a separate trigger at the helicity cycle - 30Hz to 2kHz. In essence, the scalers are a deadtime-free integration of the data, integrated over the helicity period. The helicity gate defines the integration time. It may be an externally supplied gate and will include a period between helicities when the scalers will not count. In this period (typically 200μsec) there will be plenty of time to read out other modules in the VME crate. This interrupt should take priority over other interrupts because we should not miss any helicity periods.

It is highly desirable to be able to "flag" these integration periods by the helicity itself. Although the helicity information should be available elsewhere in the VME crate, redundancy is important for asymmetry measurements.

The "scaler triggers" should contain additional information read from different units, as described above.

B Rate Estimates

The FADC sampling rate is 250 MHz. We will typically read out 10 samples at the timeframe of the trigger. For 1 FADC of 16 channels, the maximum data rate with zero deadtime is expected to be 160 kHz. Hence the data rate is $160\,\mathrm{kHz} \times 12\,\mathrm{bits} \times 10\,\mathrm{samples} \times 16\,\mathrm{chan} = 307\,\mathrm{Mbits/sec} = 38\,\mathrm{Mbytes/sec}$. For this DAQ we will use the fast 6100 VME cpus and Gigabit ethernet. The readout will be augmented by an I/O register and a separate scaler unit. For running in Fall 2009, the Møller signals will be split and sent to both this new DAQ and the old DAQ.