The PREX collaboration requires the option of running at higher helicity reversal frequency in order to suppress various sources of random noise. Practical considerations in the present data acquisition systems limit the maximum frequency to around 300 Hz. It is expected that modulations associated with 60 Hz line frequency will be an important source of noise, both from beam modulations and electronics noise. For this reason, particular attention is given to reducing the total contribution from 60 Hz frequence components.

PREX proposes that the helicity be changed with the period associated with 30 Hz, 120 Hz, or 240 Hz (33.3 ms, 8.33 ms, or 4.17 ms helicity state windows). At Jefferson Lab, the present helicity reversal frequency is 30 Hz. This flip rate is insensitive to 60 Hz line noise, as each window integrates over two full 60 Hz cycles. For the higher frequency reversal periods, a multiplet of helicity windows will be required to cancel line noise.

# 1 Overview of the Helicity Reversal Scheme

The proposed helicity reversal scheme is similar to what is presently used, except for the use of multiplets used to cancel 60 H noise. Helicity states, chosen in multiplets (described below) in a pseudo-random pattern, are held for a fixed time. The helicity state transition is followed by a settling time $T_{Settle}$, after which a signal is asserted to mark a period of valid data, for a time $T_{Gate}$.

The required control signals are

1. **PS** (pair-sync): Toggles at 1/2 the reversal frequency, used to mark complementary windows in a helicity pair.

2. **MS** (multiplet sync): Held true for the first window of each helicity multiplet, this allows easy syncronization in the data stream with the multiplet helicity pattern.

3. **GATE**: Held true for a fixed time $T_{Gate}$, this marks the entire valid integration period. Specific data acquisition systems will use the leading edge to set a locally-timed gate for data collection, others DAQs will use this signal directly to gate readout electronics.

4. **HELICITY**: This signal carried the helicity information to trigger the voltage change on the Pockels cell and on helicity-correlated feedback systems. It will be distributed only to the hut in the electron source and to the isolated "helicity magnet" system.

5. **DH** (delayed helicity): This signal is changed synchronously with **HELICITY**, but carries the helicity information delayed by not-less-then 1 multiplet. PREX specifcally requests delay settings of 8 windows (for 30 and 120 Hz running) and 16 windows (for 240 Hz running), as well as the availability of a "real-time" mode in which **DH** matches **HELICITY** without delay.

The settle time $T_{Settle}$ should be selectable. The most likely values to be used during PREX will be around 100 $\mu$sec at 240 Hz reversal and 250 $\mu$sec at

30 Hz reversal. A reasonable set of starting values might be (50, 75, 100, 150, 250, 500) microseconds.

At 30 Hz, the helicity states should occur in pairs, with the first window state selected randomly and the second window complementary to the first. For higher frequencies, line noise will be cancelled through the use of multiplet helicity patterns:

- Some set of flipping frequencies which are multiples of 60 Hz should be available. Specifically requested, in addition to 30 Hz, are 120 Hz (T=8.33 ms per state), and 240 Hz (T=4.17 ms).
- At 120 Hz, the helicity state sequence should occur in quadruplets, selected at random from the patterns $(+--+)$ or $(-++-)$.
- At 240 Hz, the helicity state sequence should occur in octoplets, selected at random from the patterns $(+--+-++-)$ or $(-++-+--+)$.
- For other frequencies which are harmonics of 60 Hz ($f = N \times 60$), helicity patterns should be generated in multiplets of $2N$ windows. The first $N$ windows of the multiplet should occur as randomly-ordered helicity pairs, with the subsequent $N$ windows being complementary.
- The flip pattern must be locked to the 60 Hz line power phase.
- Any variation in helicity window period (necessary to hold the line-phase lock) should occur during the $T_{Settle}$. The time $T_{Gate}$ must always be fixed.

It is further requested that a complementary signal to **HELICITY** should be generated, or a current shunt used, to balance the current draw on the board between the two helicity state selections. Although this sounds minor, in the past the selection of a helicity state by a non-isolated board was seen to correlate to actual deviations of the electron beam. Balancing the current draw between helicity state selections will provide further suppression of any potential problems with electrical pickup, and provide additional safety factor in case the board in imperfectly isolated. This feature will also be a convenient safeguard for the the applications of the board in test setups, where elaborate electrical isolation would be inconvenient.

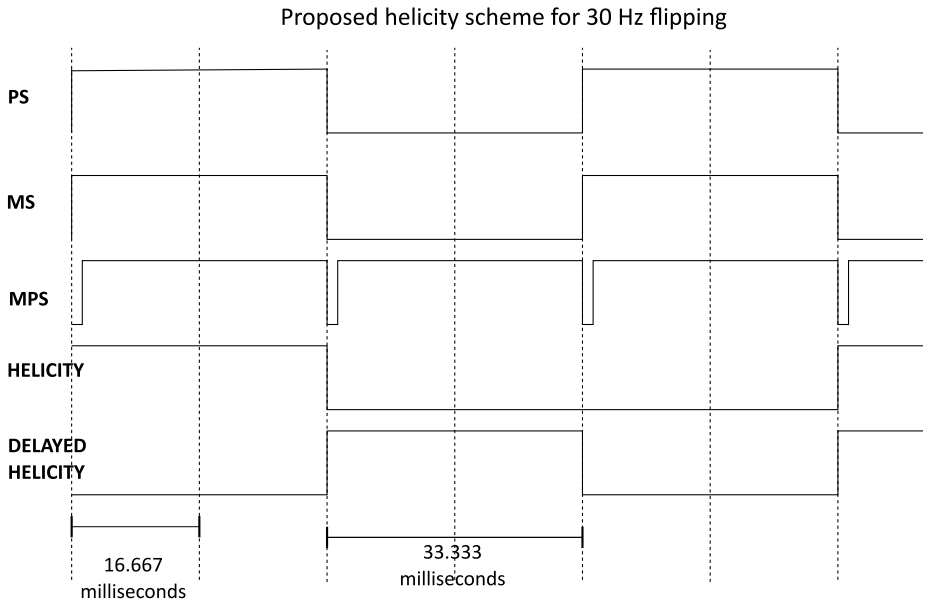


Figure 1: Proposed helicity scheme for 30 Hz flipping. Each helicity window averages over two cycles of 60Hz noise, providing cancellation of line noise. Pairs of complementary helicity are used, with the order selected at random. A 8-window delay on **DH** is used to avoid correlations between real and reported helicity.

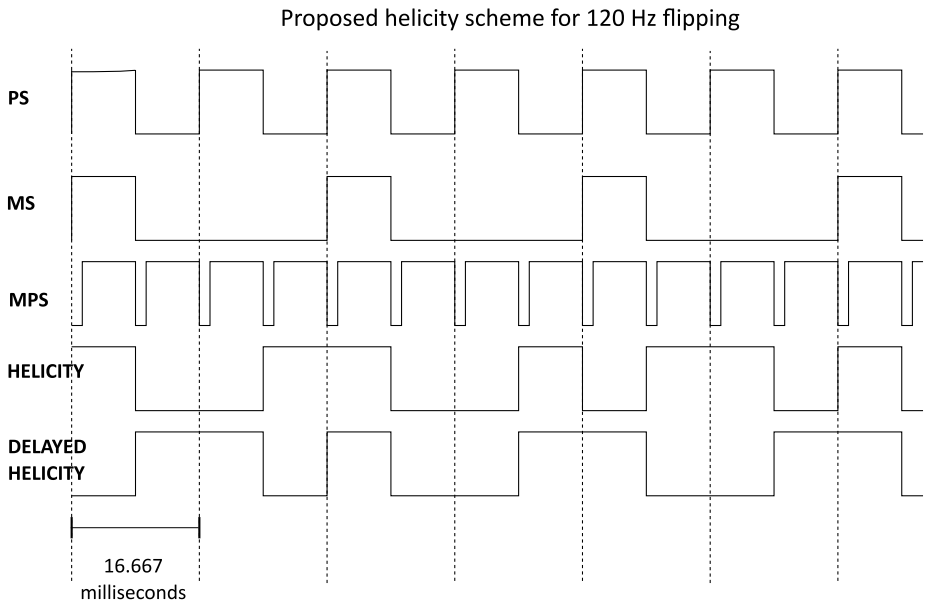


Figure 2: Proposed helicity scheme for 120 Hz flipping. Line-locked quadruplets, composed of two complementary pairs, are used to cancel 60 Hz line noise. A 8-window delay on **DH** is used to avoid correlations between real and reported helicity.

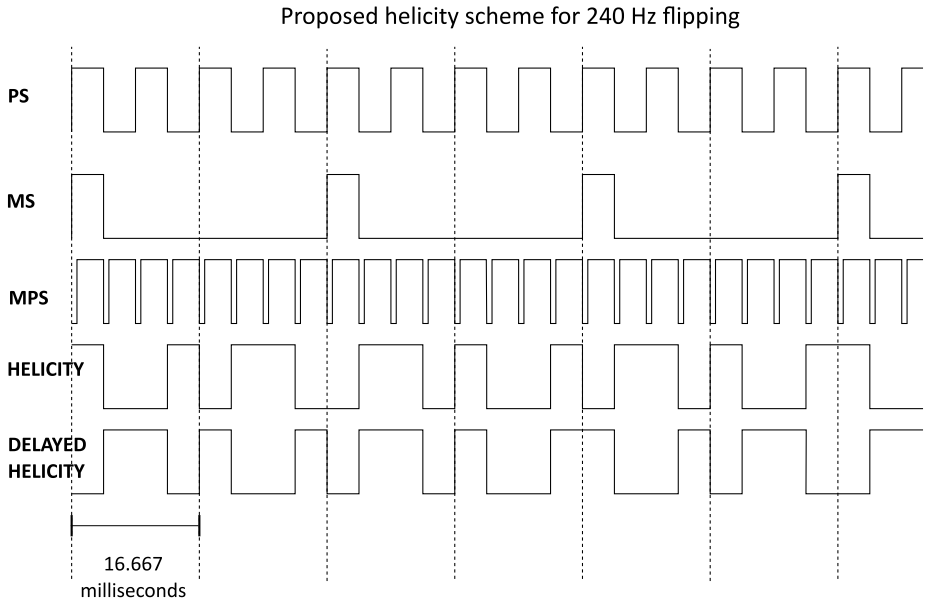


Figure 3: Proposed helicity scheme for 240 Hz flipping. Line-locked octoplets composed of two complementary quadruplets are used to cancel 60 Hz line noise. A 16-window delay on **DH** is used to avoid correlation between helicity and reported helicity.