SoLID DAQ

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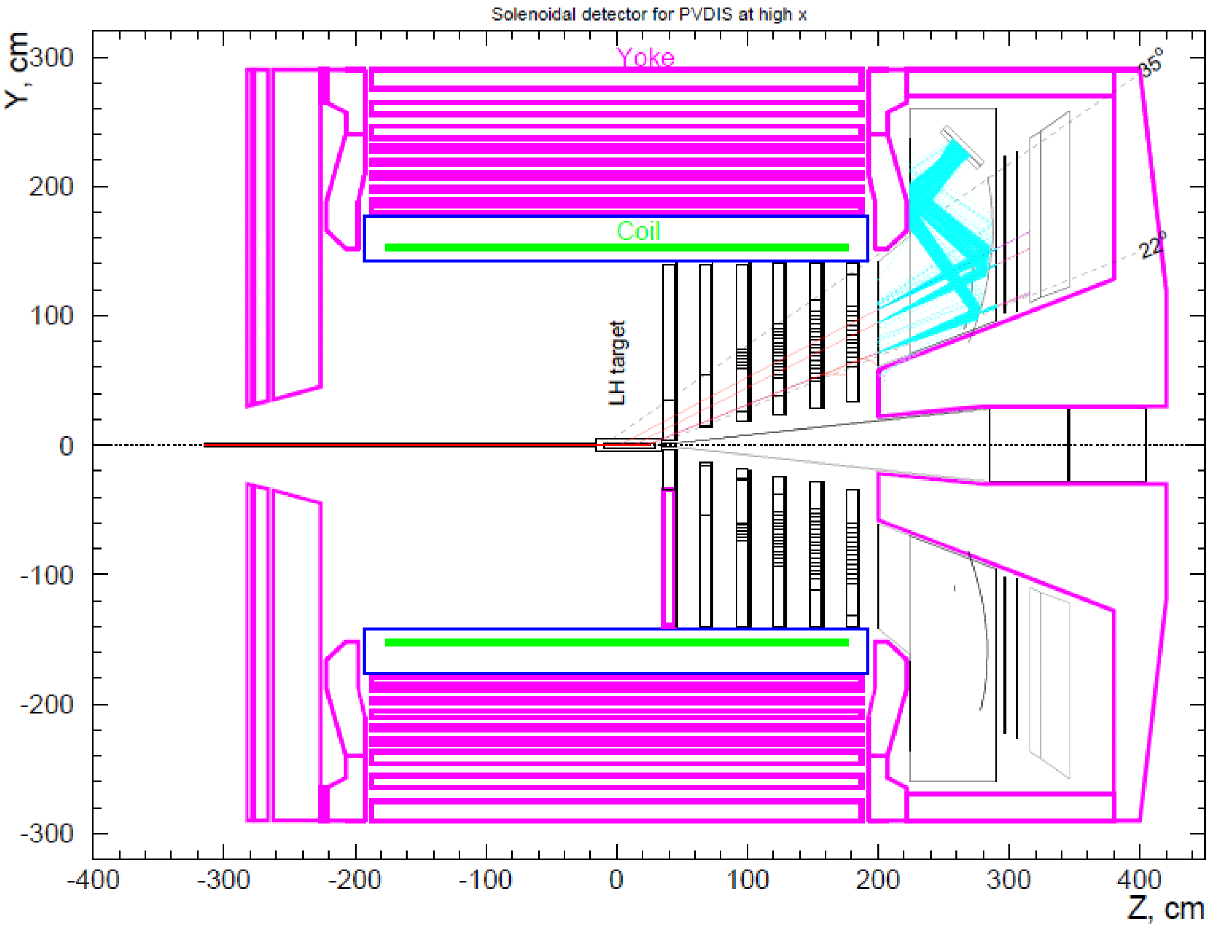
Overview

- Requirements overview
- GEM
- Electronics layout
- Budget
- Parasitic tests
- Test stand
- Conclusion

Detector layout and trigger for PVDIS



Trigger

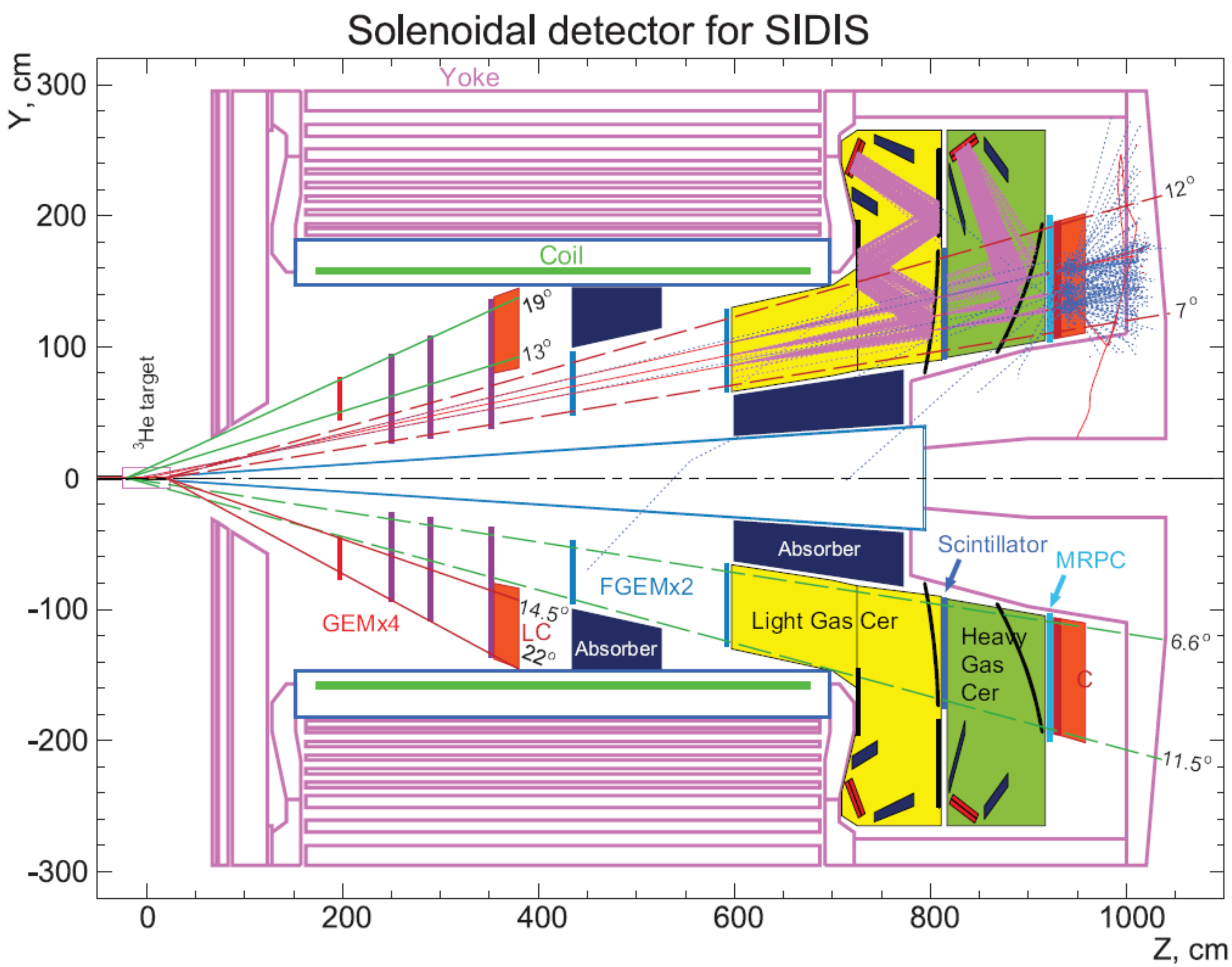
Calorimeter
+
Cerenkov

200 to 500 KHz of electrons

30 individual sectors

Max 17 KHz/sector

Detector layout and trigger for SIDIS



Trigger

Calorimeter
+
Cerenkov
+
MRPC

Max rate 300 KHz

SIDIS: Single Electron Trigger

- Large Angle: 65 kHz @ 11 GeV
  - Calorimeter only
  - Electron: 11 kHz
  - High energy photon: 51.5 kHz
    - (possible to be rejected by including GEM in trigger, need study)
  - Hadron: <3 kHz (energy cut)
- Small angle: 120 kHz @ 11 GeV
  - Calorimeter + Gas Cherenkov
  - Electron: 90 kHz
  - High energy photon: 16 kHz (after Gas Cherenkov)
  - Hadron: 15 kHz (after Gas Cherenkov and Calorimeter)
- 8.8 GeV gives about 240 kHz

SIDIS: Hadron trigger

- Calorimeter + MRPC + Scintillator
- Hadron rate : 7.7 MHz
  - Charged hadron: 6.1 MHz (dominated)
  - Electron: 0.1 MHz
  - Photon: 1.5 MHz (after MRPC and Scintillator)
- Dominated by inclusive hadrons

SIDIS: Coincidence @ 35 ns window

- Coincidence rate: 50 kHz
- Given the safety margin, expected to handle about 100 kHz.
  - Include some single trigger to study detector performance etc.
- 4kB * 100 kHz ~ 400 MB/s to disk
  - Goal to reduce things to 50 MB/s by L3 farm

SIDIS channel count

Detector	Module type	Number of channels	Number of FADC
Forward Calorimeter	FADC	1896	119
Large angle calorimeter	FADC(+TDC)	920	58
Light Gas Cerenkov	FADC	120	8
Heavy Gas Cerenkov	FADC	270	17
Scintillator	FADC	120	8

The FADC of LC can be programmed to produce timing signals with ~400ps resolution (already demonstrated by simulation) to remove the needs of TDC.

APV25 readout

- Buffer length 192 samples : 4.8 us Look back 160 samples : 4 us

- Estimated occupancy : 220 hits per trigger, X Y data, 440 strips

GEM : 6 Layers 164 000 channels total, 28 000 channels per planes

Occupancy : 1.6 %

- APV readout time :

t_APV = 141 x number_of_sample / 40 MHz

t_APV(1 sample) = 3.7 us.

Max rate APV front end :
270 KHz in 1 sample mode
90 KHz in 3 samples mode
Will be triggered by coincidence trigger around 50 KHz

APV25 VME readout

- 220 hits x 2 x 2 bytes / 200 Mb

Average readout time for GEM
4.4 us / 11 crates

Readout time negligible and no dead time with buffering

More detailed simulation of APV25 and background being implemented will give confirmation in about 1 month

Other GEM readout chips

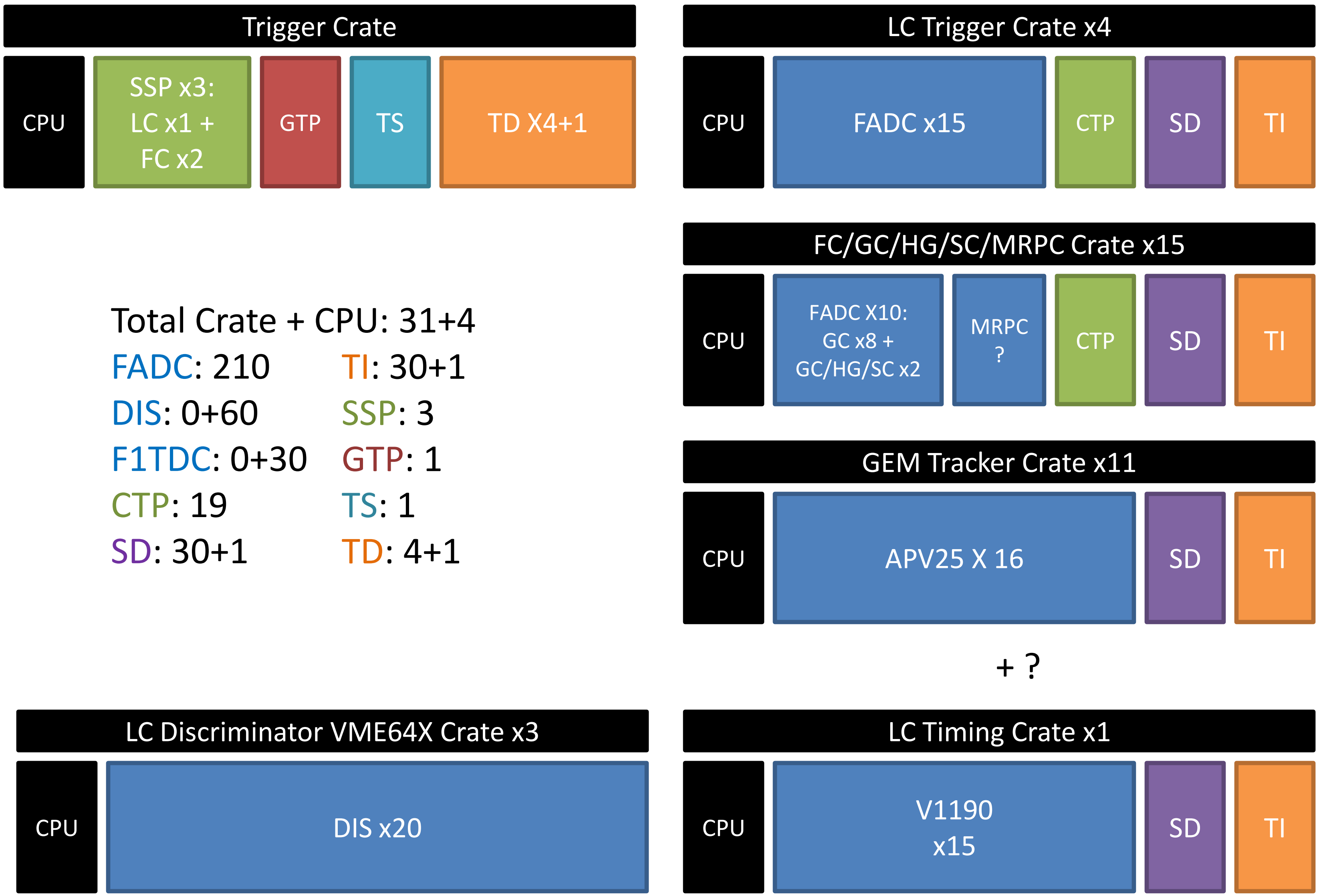
Name	Exp	Det	#ch	Shaper (ns)	Noise	Range (fC)	Pol.	ADC	f (MHz)	P/ch. (mW)	Feat.	Tech	Rad hard
APV25	CMS	Si strip	128	50	270+38e/pF	20	both	A	40	2.7	PD, PR	0.25 CMOS	10
AFTER	T2K	TPC	72	100-2000 s-gauss	(350-1800) + (22-1.8)e/pF	19	both	A	1-50 (100)	7.5	VG,VS	0.35 CMOS	no
MSGCROC	DETNI	Gas strip	32	T: 25 E: 85	2000e @ 40pF	800	both	A,1	2ns TDC		VG, ZS	0.35 CMOS	no
Beetle	LHCb		128	25	500+50e/pF	17.5	both	A/1	40	5.2	F-OR	0.25 CMOS	40
VFAT	TOTEM		128	22	650+50e/pF	18.5 (cal)	both	1	40	4.47	F-OR	0.25 CMOS	50
NINO	ALICE	TPC	8	1	1900+165/pF	2000 th<100	both	1	async	30	BR	0.25 CMOS	no
CARIOCA	LHCb	MWPC	8	<15 @ 220pF	2000+40e/pF	250	both	1	async	46	BR	0.25 CMOS	20
PASA+ ALTRO	ALICE TPC	TPC	16	190_{fwhm} s-gauss	570e @20 pF	160	both	10	20	< 40	BC, TC, ZS	0.35,0.25 CMOS	
SVX4	CDF, D0	Si strip	128	100-360	410+45e/pF	60fC	neg	8	106 (212)	2	ZS	0.25 CMOS	20
SPIROC	ILC, T2K	SiPM	36	A:25-175 T: 10	A: 1/11pe; T:1/24pe	2000 pe	neg	8-12	100ps TDC	0.025 *pulse*	dual-gain	0.35 SiGe	no

Legend: PD = peak detection, PR = pile-up rejection, VG = variable gain, VS = variable shaping, F-OR = fast-OR, BR = baseline restorer, BC = baseline correction, TC = tail correction, DC = data compression, ZS = zero suppression

GEM in trigger

- Use signal of 5th GEM plane for fast trigger
- Quality of signal to be tested
- Could reduce rate in Large Angle from photon calorimeter by 50 KHz
- Additional FADC channels to put in trigger

DAQ/Trigger for SoLID SIDIS



SIDIS electronics

Module	Unite price	Quantity	
FADC 250	4500	210	$945,000
CTP	5000	19	$95,000
SSP	5000	3	$15,000
GTP	5000	1	$5,000
VXS crate	11500	1	$11,500
TS	3500	1	$3,500
TI	3000	30	$90,000
TD	3000	4	$12,000
SD	2500	30	$75,000
VXS crate	11500	30	$345,000
VME CPU	3400	31	$105,400
L3 farm node	5000	12	$60,000
		Total detectors	$1,762,400
VXS crate	11500	1	$11,500
Discriminators	2500	60	$150,000
VME64X crate	8100	3	$24,300
V1190	11010	15	$165,150
VME CPU	3400	4	$13,600
TID	3000	1	$3,000
SD	2500	1	$2,500
			$370,050
		Grand Total	$2,132,450

Other projects

- SuperBigBite
  - 242 hadron calorimeter
    - 16 FADC
- Hall 12 GeV upgrade
  - VDC 2944 channels
    - 24 V1190 TDC
  - 50 FADC
  - CTP, TS, TD,SD, 2 VXS crates

- Other experiments : Primex ? Up to about 130 JLAB FADC available

SIDIS electronics

Modules	Unit price	Quantity	Price	Borrow
FADC 250	4500	144	$648,000	HRS + SBS
CTP	5000	15	$75,000	HRS
SSP	5000	2	$10,000	HRS
GTP	5000	0	$0	HRS
VXS crate	11500	0	$0	SBS
TS	3500	0	$0	HRS
TI	3000	24	$72,000	HRS
TD	3000	2	$6,000	HRS
SD	2500	24	$60,000	HRS
VXS crate	11500	24	$276,000	HRS
VME CPU	3400	19	$64,600	HRS
L3 farm node	5000	12	$60,000	
		Total	$1,271,600	
VXS crate	11500	0	$0	HRS
Discriminators	2500	50	$125,000	HRS
VME64X crate	8100	0	$0	HRS
V1190	11010	0	$0	HRS
VME CPU	3400	0	$0	HRS
TID	3000	0	$0	HRS
SD	2500	0	$0	HRS
		Total timing	$125,000	
				With 20 % spare
		Total detectors	$1,396,600	$1,675,920

Test run setup

- MRPC
  - V1290
  - JLAB or SIS FADC
- GEM / Hadron Blind Detector
  - APV25 (UVA)
    - SRS readout
    - MPD

DAQ electronics projects at UMass: spring and summer 2012
R.Miskimen

- UMass is responsible for the final assembly and testing of all *380 FADC modules* for Hall D. This activity will take place at UMass summer 2012, probably stretching into the fall.
- An undergraduate, Fabien Ahmed, spent the summer of 2011 at JLab working with the electronics group on FADC tests. A graduate student, Bill Barnes, and team of undergraduates will work on the electronics tests at UMass.
- Operations at UMass will include mechanical assembly of the VME boards, programming the FPGA's, verifying board operation, measuring and recording noise levels.
- Readout through a Wiener USB board in the VXS crate, connected to PC

DAQ electronics projects at UMass: connection to SOLID

- This activity helps Hall D, only helps SOLID by building expertise in the collaboration for working with and debugging DAQ electronics

- With support from Hall A, we would develop a CODA based DAQ test station at UMass: replicate the one VXS crate/sector readout for PVDIS/SOLID

Need CODA, and to borrow CTP, SSP, and CPU

Test DAQ rates, triggers, software for FADC

Hall A HRS DAQ Test stand

- Injector Compton
  - 2 FADC and SD boards
- Ordered parts
  - 2 VXS crates
  - 4 FADC
  - 2 TI, SD, TD

  - CODA3 still in the work (maybe out at end of February) : test L3 Farm

  - Application for Compton Counting DAQ for PREX ?

Simulation

- Simulation of background up to digitization level
  - Occupancies and event size
  - Trigger simulation
  - Data reduction

Conclusions

- Coincidence trigger to reduce rate to about 50 KHz
- APV25 limiting DAQ rate
- Timing needed for Large Angle Only for TOF
- Overlap of electronics with other experiment
- Around 1.7 M $ including spares for PVDIS and SIDIS
- Test of electronics for test run (APV25)
- Test stand at Jlab and Umass

Going for Hall D type electronics

Backup

SoLID SIDIS Detector Rates

- In 50 ns windows, 11 GeV

Detector	Rate	Hits	Type	Data Size per hit
GEM	4.4 GHz	220	Hits (time)	4 Byte x 2 (X/Y)
LC	120 kHz	1	Energy, Hits	8 Byte x 2 (PS/SH)
FC	200 MHz	10	Energy, Hits	8 Byte x 2 (PS/SH)
LGC	40 MHz	3	Energy, Hits	8 Byte x 2 (split)
HGC	60 MHz	4	Energy, Hits	8 Byte x 2 (split)
MRPC	850 MHz	45	Hits	4 Byte
SC	300 MHz	15	Energy, Hits	8 Byte
Total				2.5 kB

With header and other over head
event size is ~ **4 kB**

L1 Trigger

- Electron Singles Trigger:
  - LC > 400 MeV || (FC > 400 MeV && LGC)

$$T_L^e|_{11(8.8)GeV} = Y_L^e + Y_L^\gamma + \frac{Y_L^h}{R_{LC}} = 11 + 52 + \frac{56}{20} = 66(55)kHz$$

$$T_F^e|_{11(8.8)GeV} = Y_F^e + \frac{Y_F^\gamma}{R_{LGC}} + \frac{Y_F^h}{R_{LGC} \cdot R_{FC}} = 89 + \frac{620}{40} + \frac{6100}{40 \cdot 10} = 120(180)kHz$$

  - Total event rate: 190 - 240 kHz
  - Frontend data rate: 800 – 1000 MB/s
  - ROCs can barely handle this rate
    - Assuming 10 VME crates, 100 MB/s per ROC
    - add more crates since PVDIS uses > 30
  - Maybe a little bit too much to write to the tape
  - Not much room for improvement, already very close to electron yield.

Reduce L1 Trigger: Two Options

- Make coincidence with another charged particle in Forward detector
  - FC > 200 MeV && MRPC && Scintillator

$$T_F^h|_{11(8.8)GeV} = Y_F^h + Y_F^e + \frac{Y_F^{\gamma all}}{R_{MRPC} \cdot R_S} = 6 + 0.1 + \frac{200}{20 \cdot 6.5} = 7.7(6.9)MHz$$

  - Coincidence rate with 35 ns window ~ 50 kHz
- Use L3 farm
  - With powerful parallelism computing, we can easily reduce the rate by a factor of 5
  - Reduce the difficulty to put MRPC (customized VME board) into the trigger logic
- Both options give 200 MB/s data rate to the tape