SoLID GEM Detectors in US

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Outline

- Overview of SoLID GEM Trackers
- Large area GEM R&D @ UVa
- Update on APV25 Electronics
- SoLID GEM-US Pre-R&D
Overview of SoLID GEM Trackers

Tracking requirements for PVDIS

- Luminosity ~ $10^{39}$/cm$^2$/s
- Rate: from 100 kHz/cm$^2$ to 600 kHz/cm$^2$ (with baffles) from GEANT4 estimation
- Spatial Resolution: ~ 100 µm (σ) in azimuthal direction
- Total area: ~37 m$^2$ total area (30 sectors × 5 planes, each sector covering 12 degree)
- Need radiation and magnetic field tolerant

Idea

- Use the same set of GEM modules for all 3 configurations (PVDIS, SIDIS and J/ψ)
- All electronics channels from PVDIS would be more than enough for SIDIS and J/ψ
Overview of SoLID GEM Trackers: Large area GEM challenges

- SoLID needs GEM modules as large as 113 cm × 44 cm for the larger disk of PVDIS

- The biggest challenge used to be the non-availability of large area GEM foils.
  - Previously limited by double mask technique for etching: hard to the two masks accurately: Max area was limited to ~ 45 cm × 45 cm
  - New Single Mask technique allows to make GEM foils as large as 200 cm × 55 cm

- The remaining challenge is large production capacity:
  - If all LHC related large GEM project (CMS, ALICE, TOTEM) gets underway, this will require almost 100 % of CERN production capacity
  - Currently work going on for large GEM production capabilities in China and in the US.
Characteristics of PRad GEM trackers

- 2 large triple-GEM chambers (~122 cm × 55 cm)
- Largest GEM ever built, bigger than the largest SoLID GEM module
- COMPASS style 2D Cartesian strip readout: long narrow strip (> 130 cm) → but still low capacitance noise
EIC-FT-GEM (SoLID) Prototype I

- Trapezoidal shape 1-m long triple-GEM (3-2-2-2): widths at the inner radius and outer radius equal to 23 cm and 44 cm respectively.
- Readout board: flexible 2D U-V strip readouts (COMPASS style) with a pitch of 550 μm, top layer (140 μm, wide U-strips) run parallel to one radial side of the detector and bottom layer (490 μm, V-strips) run parallel to the other side.
- Test beam results published in NIM A 808 (2016) 83-92
Common GEM foil for EIC Forward Tracker R&D:

- Common GEM foil design developed by three groups at UVa, Florida Tech (M. Hohlmann), and Temple University (B. Surrow).
- Active area: A trapezoid foil with a length of 903.57 mm, widths at both ends equal to 43 mm and 529 mm and an opening angle of 30.1°.
- Opening angle of the trapezoid is 30.1 deg., allows some overlap when making a disk from 12 detectors.
- All HV sectors connections and gas flow structure are made on the large radius end.
- Honeycomb support are removed for a low mass detector
- Share a lot of features with SoLID Trackers GEMs

New assembly method:

- Ongoing work on the design of proto II of Forward Tracker Detector R&D of EIC
- Similar assembly technique for the pRad GEM chambers
- Foils are glued to frames but frames **not glued together** but sealed with O-rings and bolts
- could be re-opened.
**Upgrade of the U-V strip 2D readout board**

- The readout strip pitch is equal to 400 μm to improve spatial resolution, reduce pedestal noise and strip occupancy.
- but **cluster size will increase** → however provide an easier way to separate photon background from MIPs.
- Larger U-V strip stereo-angle of 30.1° provide significant improvement of the spatial resolution in the radial direction.
- Electrical contacts between the strips and the FE electronics done with **zebra connectors** on the outer radius side of the detector.
- With zebra connectors, **no mounted connectors and metallized holes (vias)** on the readout board.
  - Lower production cost and eliminated risk associated with vias short and connector soldering on flexible readout foil.

**Zebra-Panasonic adapter board**

- Needed to read out the chamber with he existing APV25-SRS Front End Cards, design almost ongoing.
- In the final version, for EIC/SoLID GEM trackers, the zebra strips will be directly on the FE cards.

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**Design of EIC-Proto II 2D U-V strips readout board**

- 2d U-V strips (5 μm Cu) readout on board, 50 μm Kapton; Pitch: 400 μm.
- Top layer: 80 μm U-strips parallel to one radial side.
- Bottom layer: 350 μm V-strips parallel to other radial side.

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**Drawings of the Zebra-Panasonic adapter board**

- Zebra-Panasonic adapter
- 2 APV25 FE cards per adapters
- adapters are held together with bolts and screws
- Design borrowed from ATLAS Mezzanine adapter board.
Low-Mass GEM R&D: Chromium GEM foil (Cr-GEM)

Standard GEM

5 μm Cu

100 nm Cr

50 μm Kapton

Cr-GEM

100 nm Cr

50 μm Kapton

Cr-GEM foil:

- Copper (Cu) clad raw material comes with 100 nm Chromium (Cr) layer between Cu and Kapton, 5μm Cu layers removed, leave only 100 nm residual Cr layers as electrodes, Cr-GEM foils provided CERN PCB workshop

- Using Cr-GEM foil lead to almost 50% reduction of the material of an SoLID-like light weight triple-GEM detector: this is because the material in a lightweight triple-GEM is dominated by the GEM foils & readout board
Multi Purposed Digitizer (MPD) is a VME64x module

- MPD data transferred may either on the VME bus or via optical fiber
- INFN & JLab currently working on the implementation of the communication between MPD and SSP over optical fiber
- First tested prototype expected by end of Nov/2015
- DAQ: Porting of MPD acquisition code to CODA framework close to be completed

Integration into CODA DAQ (in good progress, test currently ongoing)
- Test of the full MPD + CODA DAQ with SBS chamber in coming weeks
The Scalable Readout System (SRS)

- APV25-based system developed by the international RD51 Coll. based @ CERN
- Front End cards on the chamber host the APV25 chip ➔ data to ADC via HDMI cables
- ADC cards interfaced with the FPGA board (FEC card) ➔ FEC data fragment to the SRU
- SRU send the data fragment from many FECs to the DAQ PC through Gb Ethernet

The Need for PRad GEMs readout:

- Peak trigger rate 5 kHz
- 72 APV25-FE cards (9216 channels), 6 (8*) ADC/FECs ➔ 2 SRU boards
- Implementation of the 10 Gb Optical link for the SRU (done)
- Integration of SRS into CODA DAQ (in good progress, test currently ongoing)
GEM in Experiment at JLab in 2016

- The PRad in Hall B: (April – May 2016)
  - Two PRad GEMs 120 cm × 55 cm provide 100 μm position accuracy
  - Readout electronics: APV25 + SRS

- Tritium Experiment in Hall A (Fall 2016)
  - 4 Experiments with Tritium target with Bigbite Spectrometer @ 11 GeV
  - Two chambers (150 cm × 60 cm) made of 3 SBS GEM modules each
  - Readout electronic: APV25 + MPD
SoLID GEM-US Pre-R&D program: Plan for the next 2 years

First year 2016:

- **Study of the performance of GEM in high background rate environment**
  - Data with x-ray source combine with cosmic (and/or $^{90}$Sr) to provide the input on the GEM efficiency in high rate environment needed for the evaluation of the tracking efficiency by the tracking reconstruction software group
  - Optimization of the design of different GEM modules size needed to equipped all layers in all PVDIS / SIDIS / J/$\psi$ configuration
- **Acquire a few Chinese GEM foils for test and characterization**
  - Electrical test, Performance comparison with standard CERN foils
- **Readout electronics for SoLID GEMs**
  - Identify the need for SoLID GEM tracking and specification for the ideal chip
  - Survey of the candidate chips available on the market other than APV25, DREAM and VMM

Second year 2017:

- **SoLID GEM chambers design & prototyping**
  - Assembly of a prototype for the most challenging geometry (can even use Chinese GEM foils)
  - Applied experience learned from the EIC-FT-GEM R&D prototype II
- **Readout electronics for SoLID GEMs**
  - Acquire a few VMM electronics from RD51 for tests with the SRS DAQ
SoLID GEM-US Pre-R&D program: High rate studies for SBS

X-ray box setup @ UVa:
- Photon energy range: up to 50 keV
- Angular distribution: uniform within 60°
- Output flux: 24 MHz/cm² on the surface of GEM for 20 keV/ and current 5 μA

Charge deposition in GEM:
- Conversion rate about 0.5% to electrons for ionization
- up to 3.4*10¹¹ electrons/cm²/s equivalent to about 7 MHz / cm² MIP.
These data produced for this study could be used as input for the tracking efficiency for SoLID.
VMM developed at BNL for the ATLAS Muon Upgrade New Small Wheel

- export regulations (ITAR) compliance circuit

G. Iakovidis MPGD2015 @ Trieste

VMM2 - Second ASIC prototype in 2014

- adjustable discrimination threshold per channel
- trimming range: 15 mV in 1m increments
- sub-hysteresis mode: effective discrimination ~ 2 mV
- neighbour logic: sub-threshold neighbor channels
- polarity: adjustable positive or negative
- gain: adjustable 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/FC (max charge 2 to 0.06 pC)
- peaking time: adjustable 25, 50, 100, 200 ns

- clock frequency: up to 200 MHz to the 6bit ADC
- 12-bit timestamp: 12-b Gray-code counter on BC provides timing TAC stop (20-b, ~100 μs, sub-ns resolution)
- 4-deep FIFO
- 10-bit, 200 ns , 1.5 mW, for peak amplitude
- 8-bit, 100 ns , 1.5 mW for peak timing (relative to BC)
- 38-bit event data at digital outputs

Slides from G. Iakovidis (RD51/ & MPGD2105)
VMM2 - Frontend boards and readouts

- VMM2 FE card has an SRS version
- Supported by RD51 collaboration as replacement of APV25 chip within the community

- VMM3 expected to be release this year (2016)
- Will be very close to the final version
- Upgrade and bug fix of VMM2
- We plan to acquire a few chips to start test with our current SRS setup

Improvements in VMM3 and schedule

<table>
<thead>
<tr>
<th>Function</th>
<th>Circuit</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD handling logic</td>
<td>Readout</td>
<td>in progress</td>
</tr>
<tr>
<td>SLVS IOs</td>
<td>Digital interface</td>
<td>in progress</td>
</tr>
<tr>
<td>Latency reduction in analog and digital paths (incl. clk to data)</td>
<td>Shaping amplifier and passive filter</td>
<td>queued</td>
</tr>
<tr>
<td>Operation at 2nF input capacitance</td>
<td>Front-end charge amplifier</td>
<td>queued</td>
</tr>
<tr>
<td>Simultaneous high-resolution and direct-output operation</td>
<td>Channel and control logic</td>
<td>queued</td>
</tr>
<tr>
<td>SEU-tolerant logic</td>
<td>Register, control and reset</td>
<td>queued</td>
</tr>
<tr>
<td>Direct input for ADC characterization</td>
<td>ADC or peak detector input node</td>
<td>queued</td>
</tr>
<tr>
<td>Configuration</td>
<td>Slow interface</td>
<td>being discussed</td>
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</table>

<table>
<thead>
<tr>
<th>task</th>
<th>status</th>
</tr>
</thead>
<tbody>
<tr>
<td>VMM2 design / fabrication</td>
<td>complete</td>
</tr>
<tr>
<td>B0A package</td>
<td>complete</td>
</tr>
<tr>
<td>PCB (A2)</td>
<td>complete</td>
</tr>
<tr>
<td>VMM2 tests</td>
<td>in progress</td>
</tr>
<tr>
<td>VMM SEU &amp; L1H circuits</td>
<td>in progress</td>
</tr>
<tr>
<td>VMM3 design</td>
<td>in progress</td>
</tr>
</tbody>
</table>
SoLID GEM R&D activities requiring funding at UVa and TU

- Small investments in pre R&D pay big dividends at final R&D and production.
- While a significant progress towards SoLID GEMs accomplished within the EIC R&D program some SoLID specific funding needed.
- Following is a rough estimate for the first year of SoLID GEM pre-R&D
  - **UVa $ 20 k:**
    - Components and manpower for a Solid prototype design.
  - **TU $ 20 k:**
    - Design and fabrication costs for SoLID specific GEM foils and chamber components.
  - **UVa/TU $ 40 k:**
    - Funds to host Chinese collaborators for extended visits.
    - Purchase single mask foils from CIAE and build and characterize prototypes.

From Nilanga’s talk @ the previous SoLID Coll. Meeting
(Sept. 2015)
Summary / Outlook

Large GEM activities in US (UVa & Temple U)

- Production of Large Area GEM trackers for the SBS in Hall A and PRad in Hall B
- Ongoing intensive GEM R&D for the EIC forward tracking
- Multi-Institute collaboration for development of MPGD technologies
- Effort to promote domestic production of GEM with Tech Etch (B. Surrow, Temple U)
- Progress in the integration of the APV-25 readout electronics into Jlab CODA DAQ
  - Both APV-SRS and APV-MPD Electronics will be used in beam at JLab in 2016

SoLID GEM-US program for a two years pre-R&D

- Finalize the design of SoLID GEM modules for all configuration
- Setup a program to start testing and characterization of Chinese GEM foils
- Construction of full size prototypes of the
- Investigate needs and option for SoLID GEM readout electronics
- Study the currently available candidate such as BNL VMM or Saclay DREAM chip
Back Up
Overview of SoLID GEM Trackers: PVDIS Configuration

- Instrument five locations with GEMs:
- 30 GEM modules at each location: each module with a 12-degree angular width.

<table>
<thead>
<tr>
<th>Location</th>
<th>$Z$ (cm)</th>
<th>$R_{min}$ (cm)</th>
<th>$R_{max}$ (cm)</th>
<th>Surface (m²)</th>
<th># chan</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>157.5</td>
<td>51</td>
<td>118</td>
<td>3.6</td>
<td>24 k</td>
</tr>
<tr>
<td>2</td>
<td>185.5</td>
<td>62</td>
<td>136</td>
<td>4.6</td>
<td>30 k</td>
</tr>
<tr>
<td>3</td>
<td>190</td>
<td>65</td>
<td>140</td>
<td>4.8</td>
<td>36 k</td>
</tr>
<tr>
<td>4</td>
<td>306</td>
<td>111</td>
<td>221</td>
<td>11.5</td>
<td>35 k</td>
</tr>
<tr>
<td>5</td>
<td>315</td>
<td>115</td>
<td>228</td>
<td>12.2</td>
<td>38 k</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
<td></td>
<td>≈ 36.6</td>
<td>≈ 164 k</td>
</tr>
</tbody>
</table>

Largest GEM module size required: 113 cm x (21-44) cm
With ~5% spares, we will need about 170 k readout channels.

Large number of readout channels; but cost of electronics going down – cost per channel for the RD51 SRS APV-25 based readout is ~ $3.00 + R&D expenses to optimize electronics for SoLID needs.
Overview of SoLID GEM Trackers: SIDIS Configuration

- Six locations instrumented with GEM trackers:
- PVDIS GEMs can be re-arranged to make all layers for SIDIS by moving the modules closer to the axis so that they are overlapping with each other

<table>
<thead>
<tr>
<th>Plane</th>
<th>Z (cm)</th>
<th>R_I (cm)</th>
<th>R_O (cm)</th>
<th>Active area (m²)</th>
<th># of channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-175</td>
<td>36</td>
<td>87</td>
<td>2.0</td>
<td>24 k</td>
</tr>
<tr>
<td>2</td>
<td>-150</td>
<td>21</td>
<td>98</td>
<td>2.9</td>
<td>30 k</td>
</tr>
<tr>
<td>3</td>
<td>-119</td>
<td>25</td>
<td>112</td>
<td>3.7</td>
<td>33 k</td>
</tr>
<tr>
<td>4</td>
<td>-68</td>
<td>32</td>
<td>135</td>
<td>5.4</td>
<td>28 k</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>42</td>
<td>100</td>
<td>2.6</td>
<td>20 k</td>
</tr>
<tr>
<td>6</td>
<td>92</td>
<td>55</td>
<td>123</td>
<td>3.8</td>
<td>26 k</td>
</tr>
<tr>
<td>total:</td>
<td></td>
<td></td>
<td></td>
<td>~20.4</td>
<td>~ 161 k</td>
</tr>
</tbody>
</table>

- The idea of using the same modules for different configurations need to be evaluated
- Might not necessarily be optimal in term of cost production and best design for the experiment
Temple University GEM R&D program

Slides provided by Bernd Surrow

- Major effort on STAR Forward GEM Tracker completed with full installation in fall 2012 - 24 large triple-GEM detectors arranged on disks / 30720 channels (APV25-S1)

- Large group at TU with fully equipped micro-pattern detector laboratory (Detector lab and permanent clear room facility) at new Science Education and Research Center with outstanding resources

- Major funded EIC R&D effort on large triple-GEM detectors focusing on light-weight structures and commercial fabrication of various detector components