SBS/A1n DAQ status

Alexandre Camsonne

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Outline

- Overview
- Fastbus inventory
- Test stand
- Module flipping
- CODA 3 / Intel CPU
- MPD APV25
- Questions
- To do / timeline
- Conclusions

Overview

- Mixed DAQ using VME for GEM readout and Fastbus for other detectors

- Use multiple crates and modules to reduce deadtime

Fastbus

- A1n : Big Bite
  - Lead Glass
  - 4 Fastbus crates
- Gep :
  - BigBite 4 Fastbus crates
  - BigCal : 6 Fastbus crates
  - Cdet : 8 Fastbus crates

Fastbus

- SFI
  - Hall A : 6 + 2 (TEDF) + 1 (EEL)
  - Hall B : 5 (+ 11 available if DC upgrade)
  - DAQ group : 1
  - 6 CLEO FRITZ SFI but no driver / software

11 SFI + 4 spares

- Crate / Power supply
  - 3 BigBite
  - 2 TEDF
  - 5 + (11) Hall B
  - 2 RCS ?
  - 1 EEL
  - 2 HRS

10 powers supplies
+ 3 spares
Need 6 power supplies
and 18 Fastbus blowers

- New
  - power supplies : 10 K$
  - SFI : 9 K$
  - Intel VME CPU : 3.5 K$
- Need to check for Geographical and Arbitration controller board

Test stand

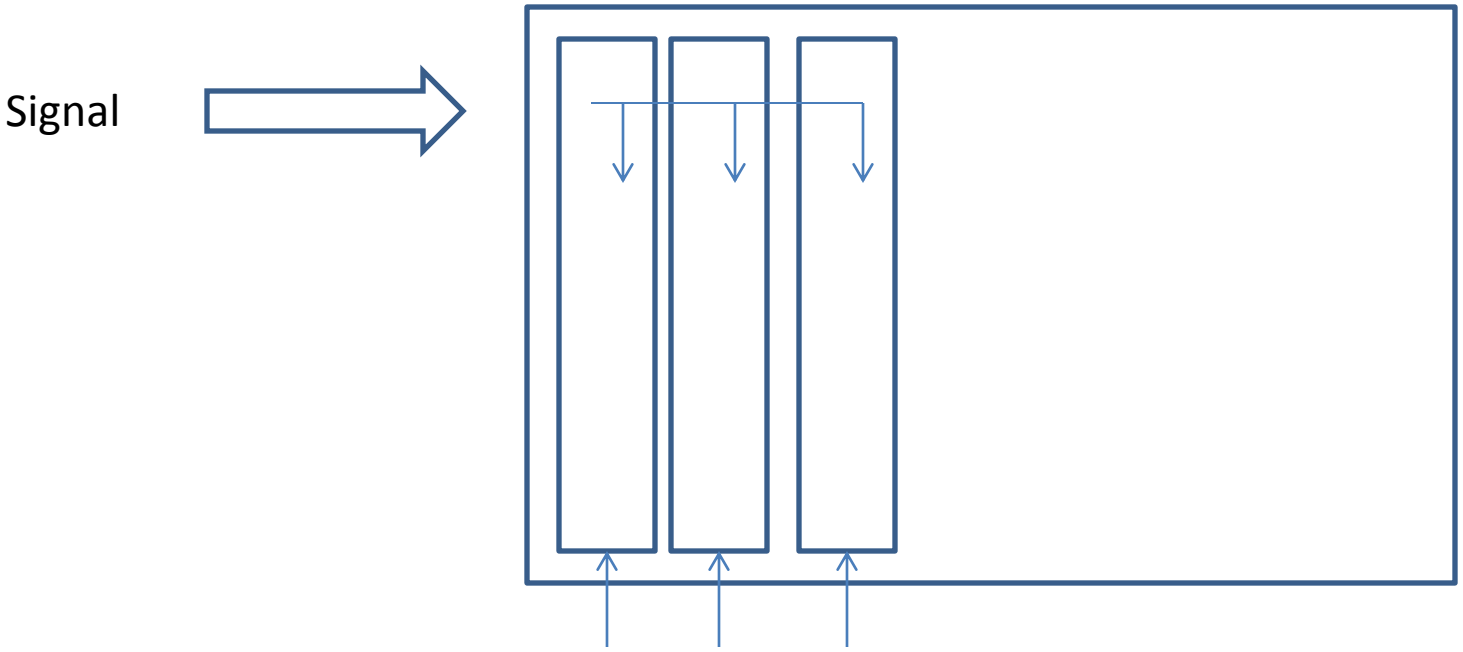
- 2 Fastbus Crate and PS from Hall B
- OSP done
- CODA running from
- 2 SFI with Intel VME CPU
- TS and VME64X crate to be installed

- Error on boards

- Testing modules :
  - Troubleshoot with old VME CPU and test components in EEL

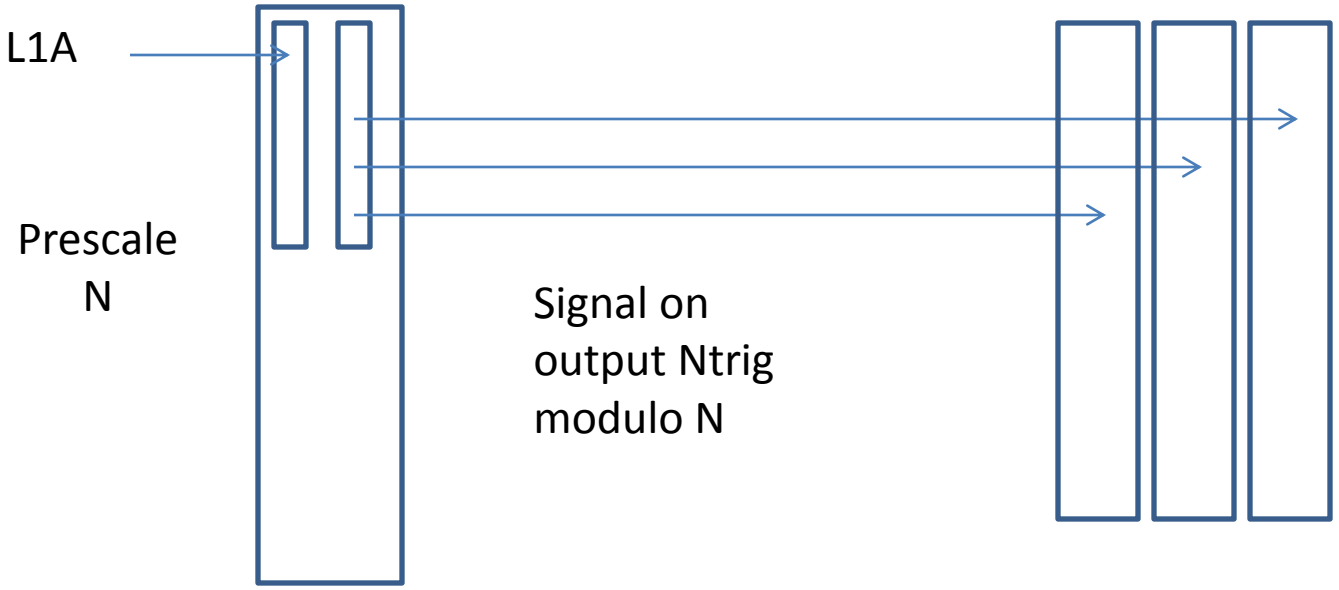
Module flipping

- Send signals to several modules to reduce encoding deadtime
- Use ribbon cable with daisy chaining



Module flipping

- V1495 programming
  - Use Compton prescaler as starting point



Module flipping

- V1495 programming
  - First version working should be good enough to evaluate dead time improvement
  - Want to implement FIFO to store state for readout and TDC output with board status for sync check
  - Need to check synch and timing resolution

Intel CPU

- Installed Linux operating system on Compact Flash so board can boot stand alone
- Readout of Fastbus working
- Trigger with old VME TI with SFI working trying new TI to test improvement with event blocking
- Develop code for module flipping readout

MPD / APV25

- MPD working with APV25 using CAEN controller
- MPD boards in UVA for GEM testing
- Move APV setup to JLAB after test
- Adapt Evaristo's library for use with CODA using Intel VME CPU

Questions

- New TI order
- HCAL trigger funding and development
- Additional cost of MQT power supplies
- Hall B Fastbus

To do / timeline

- Evaluate performance of module flipping using old VME CPU and EEL setup (1 week)
- Evaluate performance with Intel CPU (2 weeks) in TEDF
- Setup Trigger supervisor add Fastbus bin : test setup with multiple crates (1 week)
- Check data integrity and implement sync check (2 weeks)

To do / timeline

- Port MPD library to use with CODA (3 weeks)
- Test full A1n setup
- Add additional crates for SBS running
- Develop HCAL trigger
- Test coincidence trigger

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Conclusion

- Test stand in TEDF running but need to debug
- Basic readout of Fastbus done with Intel CPU
- Module flipping hardware ready : need to write software and study performance. First glance at performance in a few weeks. Major work to make sure of data synchronization

- Still lot of work left for MQT, Hadron Calorimeter, MPD

- Need complete Fastbus inventory (potential shortage of GAC and ATC)
- Full test of all electronics and spares