HCal Electronics
with First-level ECal trig

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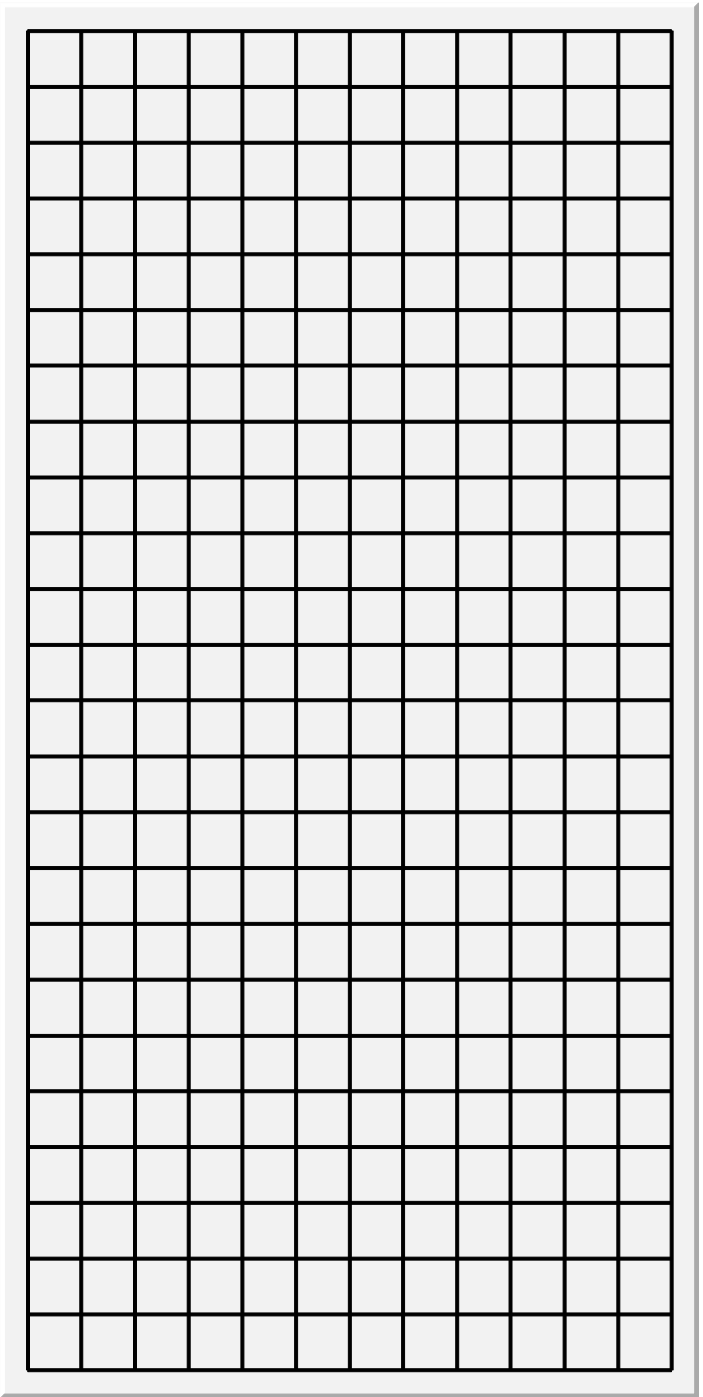
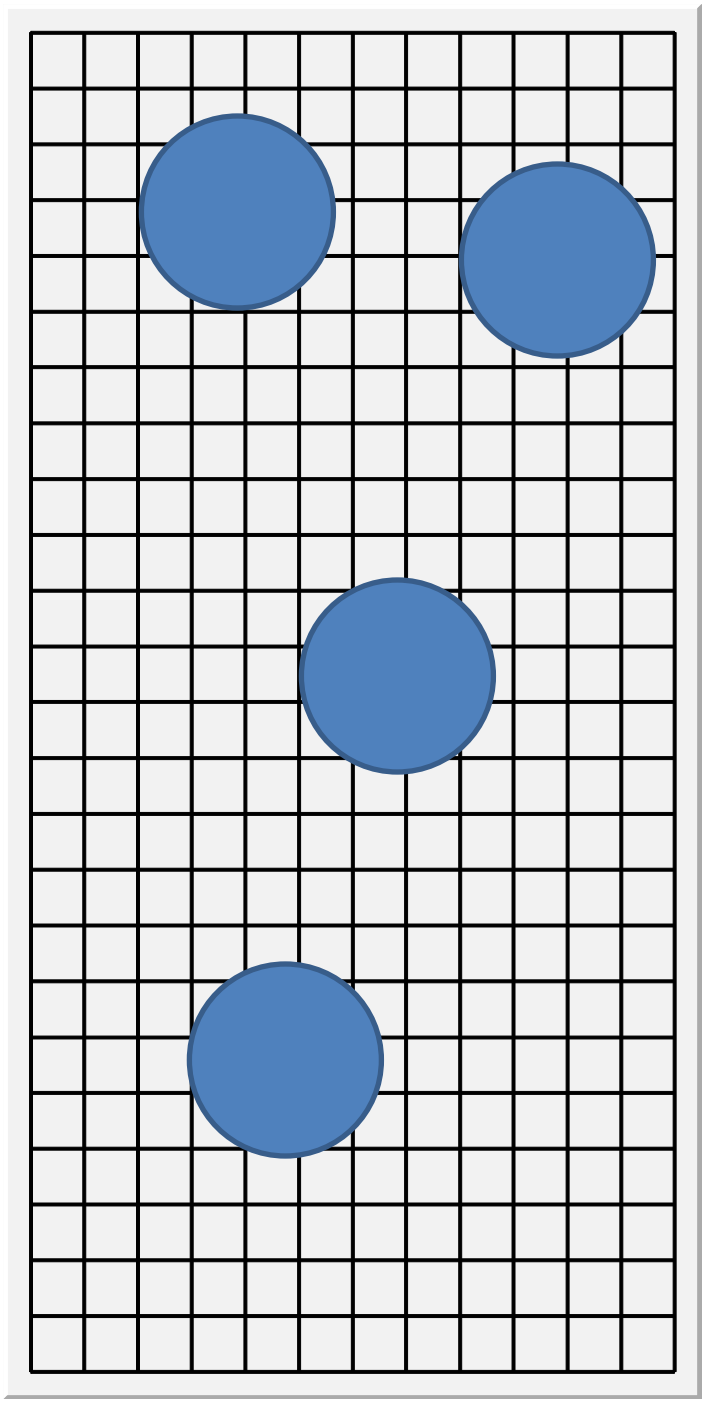


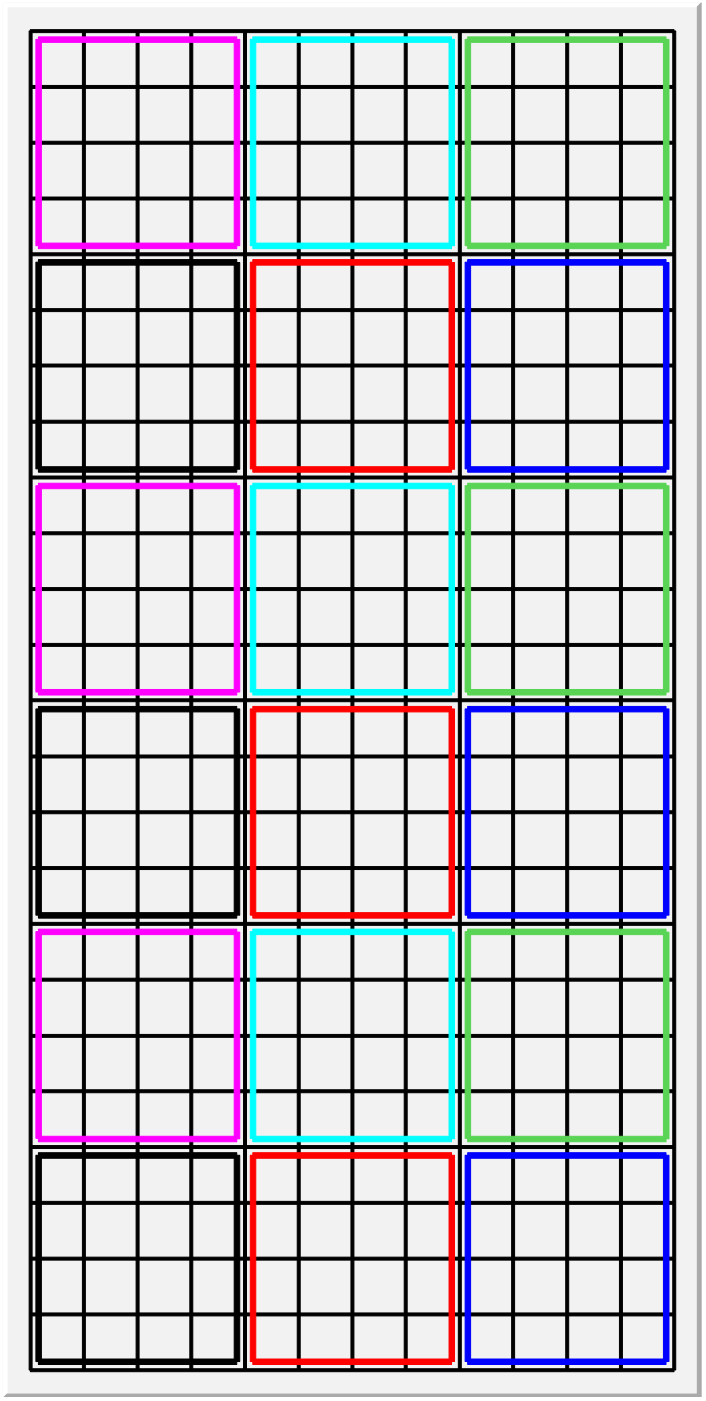
Hcal 288 modules (one PMT per module)

12 X 24 grid

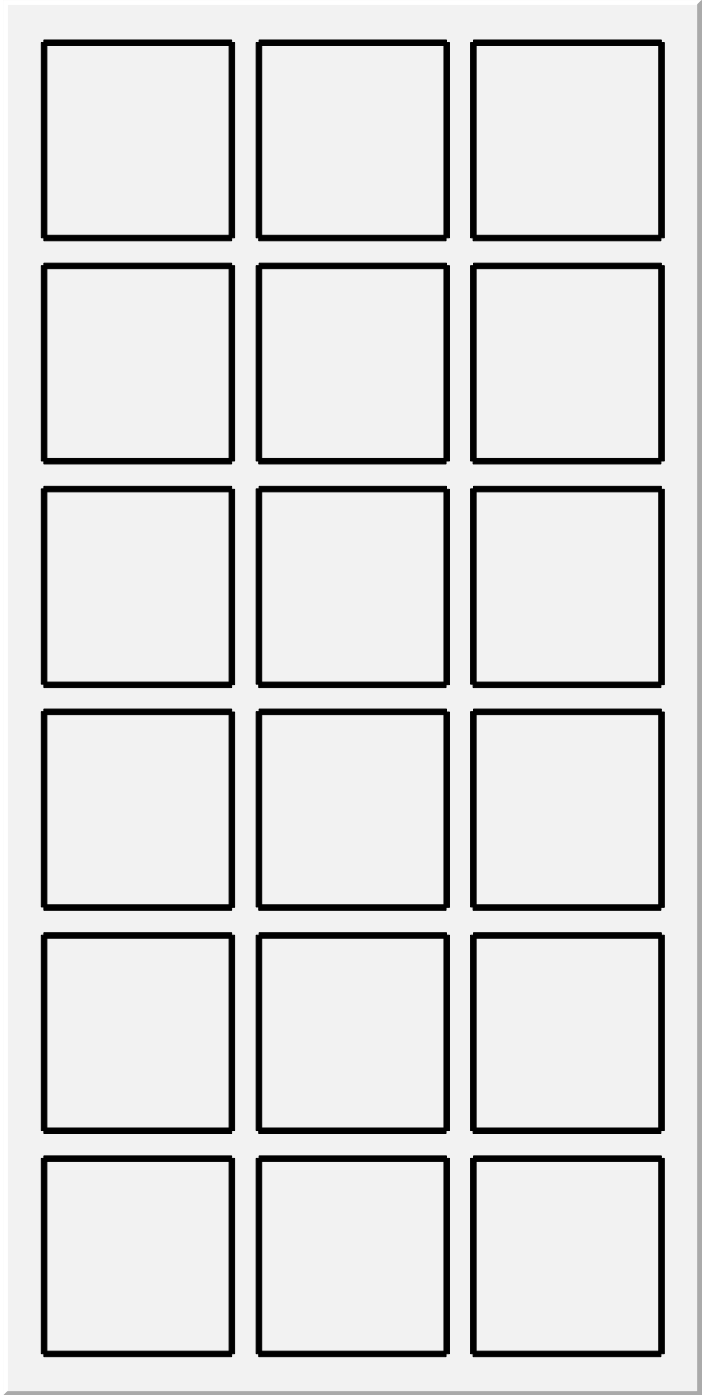


Shower size ~3X3 to 4X4

Want to (quickly) sum all energy in shower for ECal trigger, but select section of HCal expected for ECal hit.

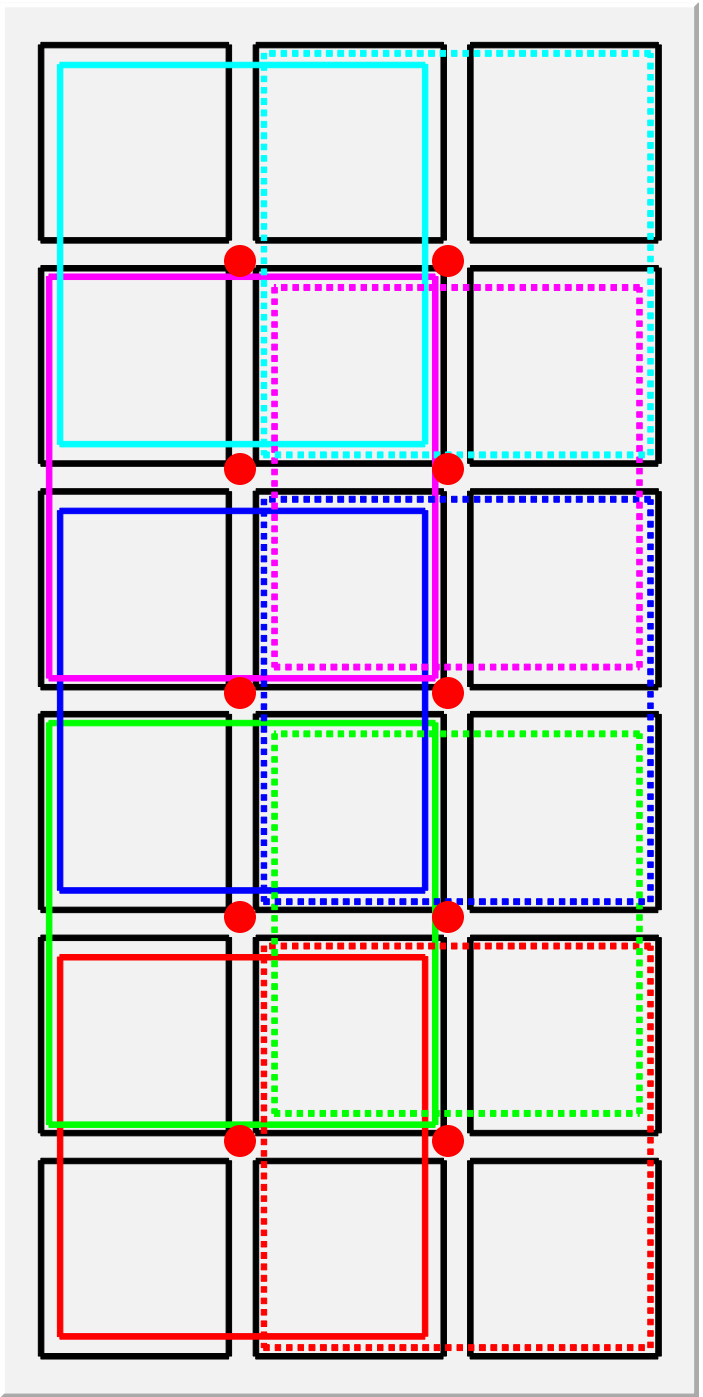


Triggering scheme being investigated by Monte Carlo based on dividing modules into groups of 4X4



Gives 18 groups in 3X6 array

Shower could be confined to a group
but more likely to extend into neighbouring groups



Form overlapping regions by taking all possible 2X2 sets of (4X4 module) groups. Each group is a member of four regions (or less).

Total of 10 regions to be summed to give total energy in region. Each sum can be compared to threshold.

Ten logic signals to send to ECal to look for energy in region of HCal expected to correspond to ECal hit.

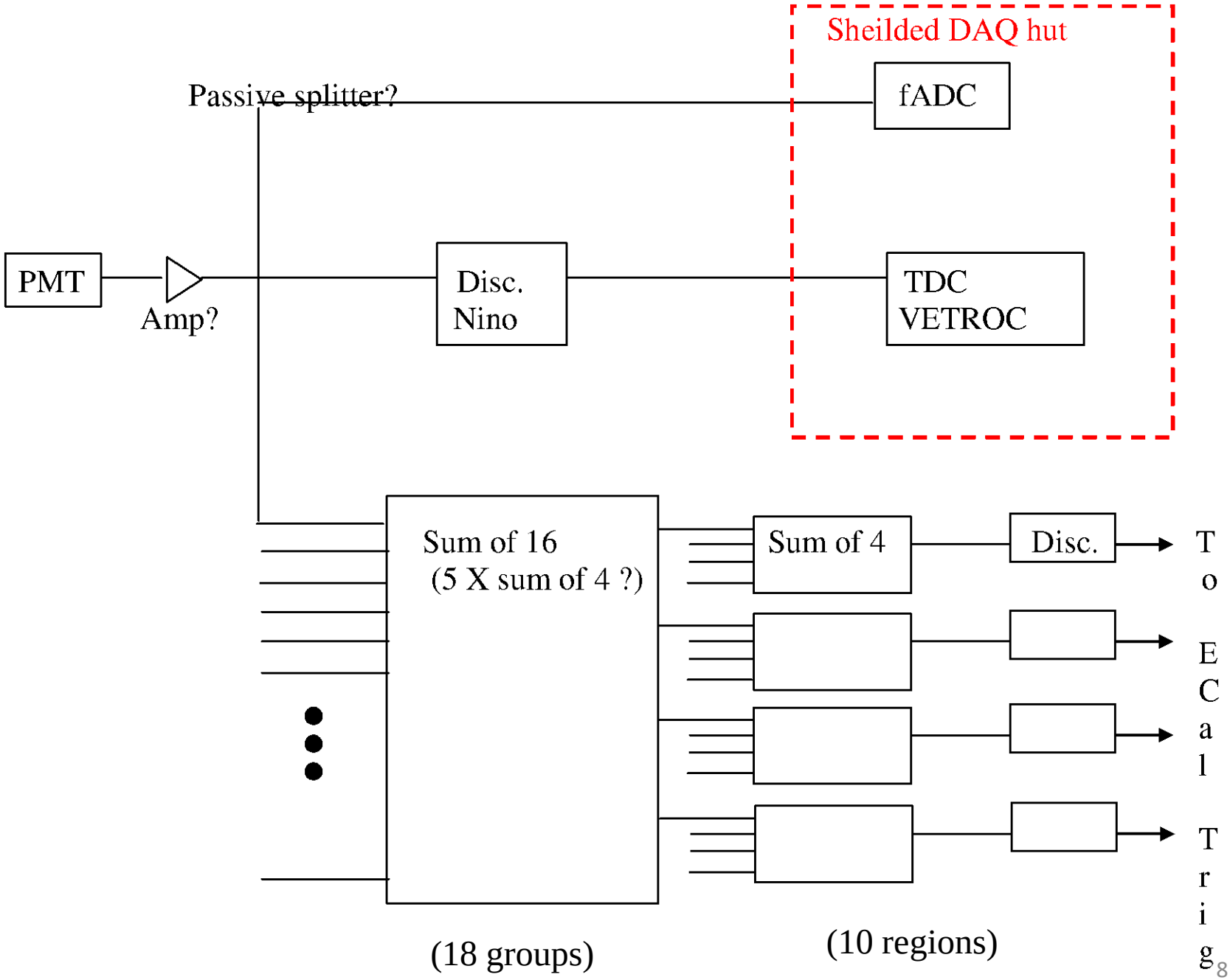
Implementing with available modules may require many modules and has a few hitches

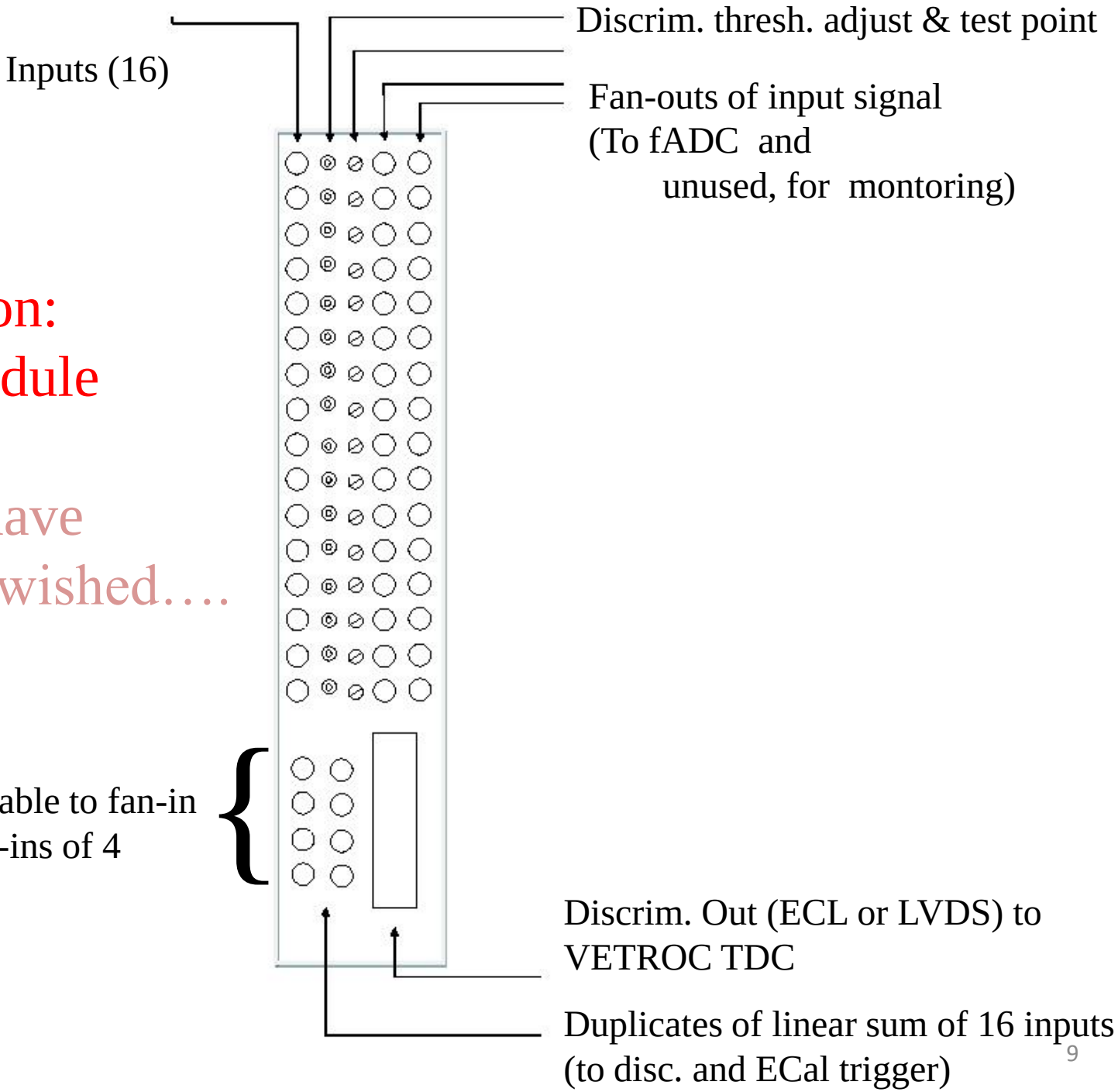
Commercial linear fan-ins are only 4-input. A 16-fold sum would require 5 channels. 18 sums requires 90 channels, 23 NIM modules. (Additional 10 chans for 4-group sums.)

Nino cards require housing, power, input connectors, attenuator (probably shielded within housing).

3-way split may require 288 custom batch panel/splitters
(or 288 linear fanouts=72 NIM modules!)

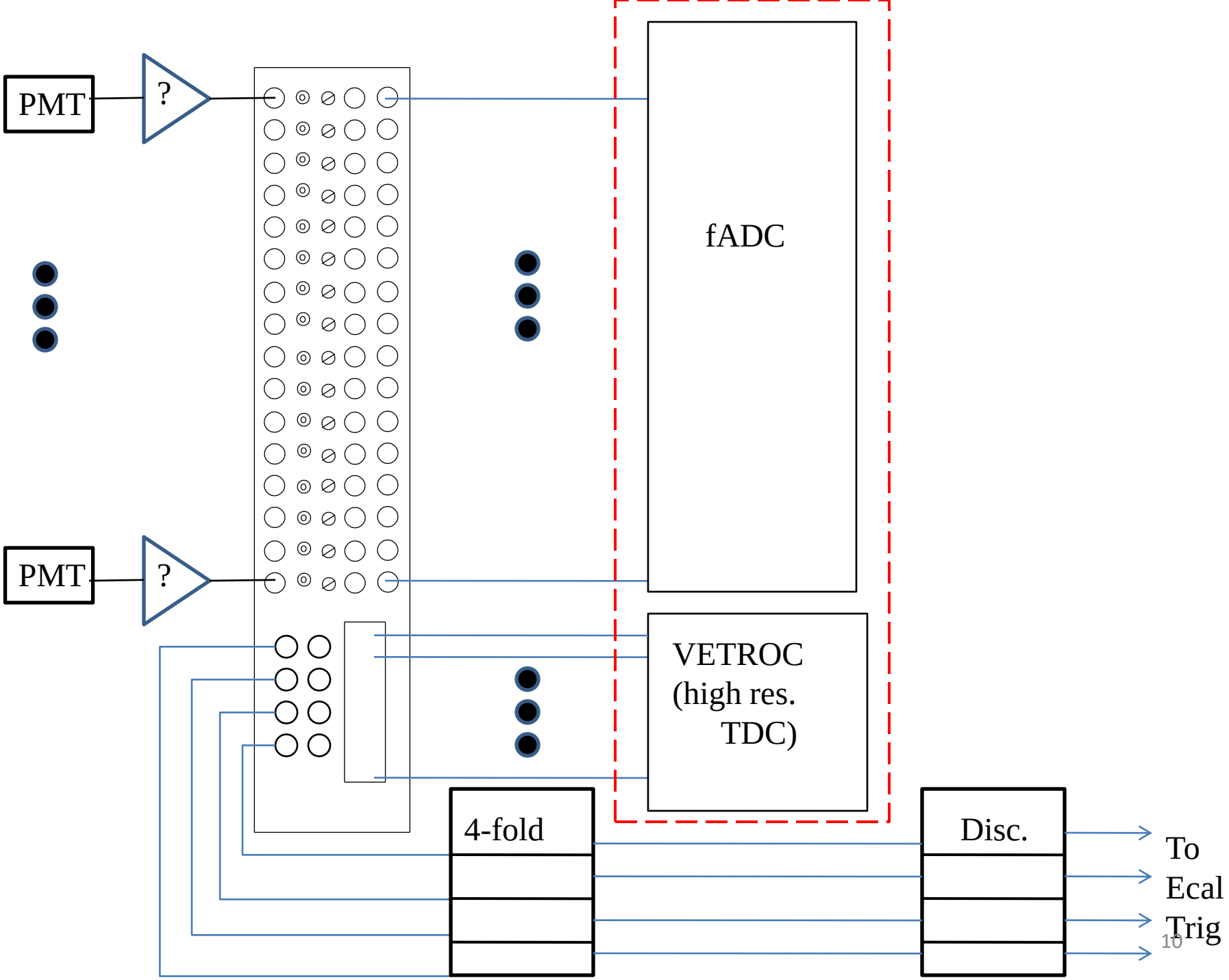
Amplifiers usually have only 2 outputs, so even if amps are used, splitter still required (probably 2-way, asymmetric to feed Nino and amp).


Sheilded DAQ hut
Passive splitter?
fADC
PMT
Amp?
Disc.
Nino
TDC
VETROC
Sum of 16
(5 X sum of 4 ?)
Sum of 4
Disc.
To ECal Trig
(18 groups)
(10 regions)



One solution:
custom module

If I could have
anything I wished….


PMT
?
PMT
?
fADC
VETROC
(high res.
TDC)
4-fold
Disc.
To
Ecal
Trig

Chris Cuevas' suggestion: Do it ALL inside FADC250.

-FADC digitizes all signals, as planned.

-Use timing feature to achieve ~65 ps timing

-Use FPGA firmware to sum signal, compare to threshold (and put out logic signals to ECal)

-No splitters, discriminators, fan-in/fan-outs, cables….

BUT…..

Vahe's study shows only 1.3 ns timing can be achieved**, for HCal signals**, with 4 ns sampling available to timing feature.

Even if transit time for sums is short(??) in FADC cable delays will be long if FADCs are in shielded electronics hut

To Do

Continue discussion with Chris/Mark to see whether anything clever is possible, or whether modest custom module is practical.

Scrounge for 16-input summing circuits? (18 needed plus spares)

Decide whether amplifiers are needed (available? 288 chan)

Consider options for housing for Ninos (vs. available discriminators?)

Consider construction of patch-panel/asymmetric splitter (3 way?)