SBS meeting
VETROC application for Cerenkov triggering

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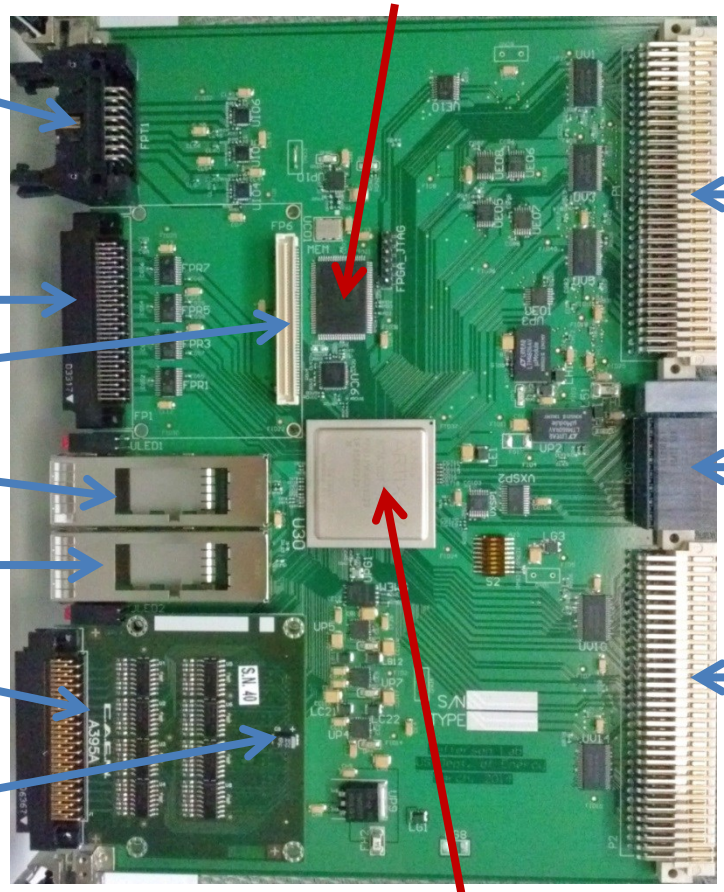
VETROC board

- Developped for Compton and SoLID MRPC
- 64 input + 8 input and 8 output
- Extension with mezannine to 128 channels (compatible with V1495 mezzanines)
- Optical link
- VXS link for triggering purpose
- Will try to develop high resolution TDC (possibly 25 ps resolution)
- Estimate price around 2.5 K$ for 64 channels and about 4 K$ for 128 channels

vXS fPGA-based Time to Digital Converter (vfTDC)

preliminary



Pipelined electronics

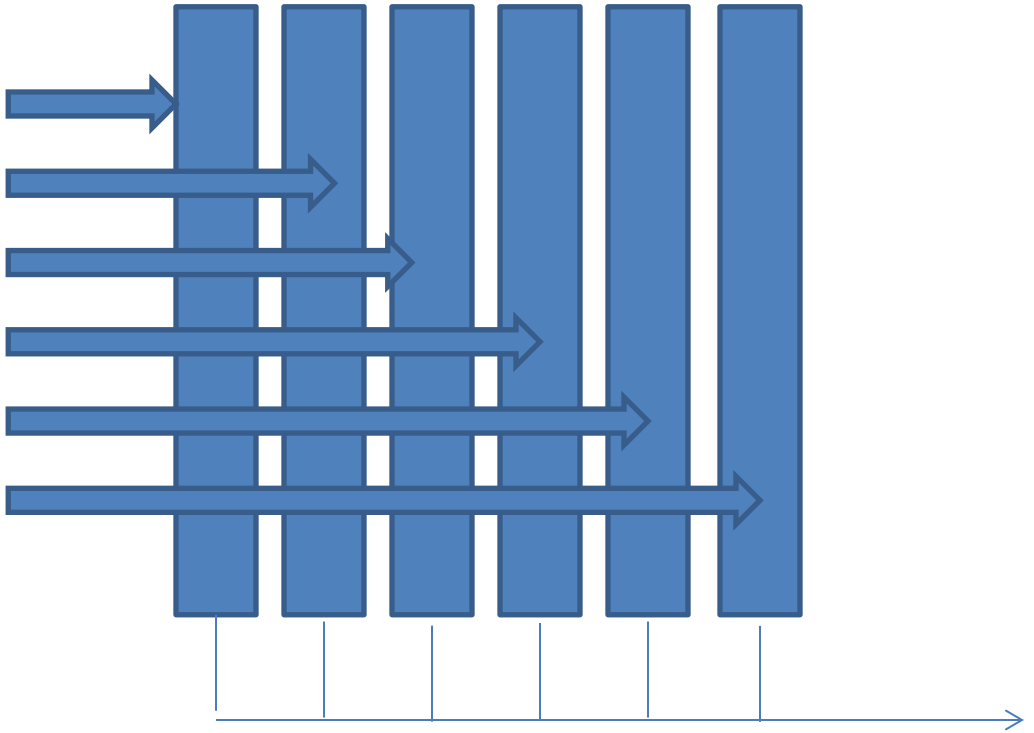
- 250 MHz sampling
- 4x 3 GBps Optical fiber link

- Can process hits every 4 ns or 8 ns

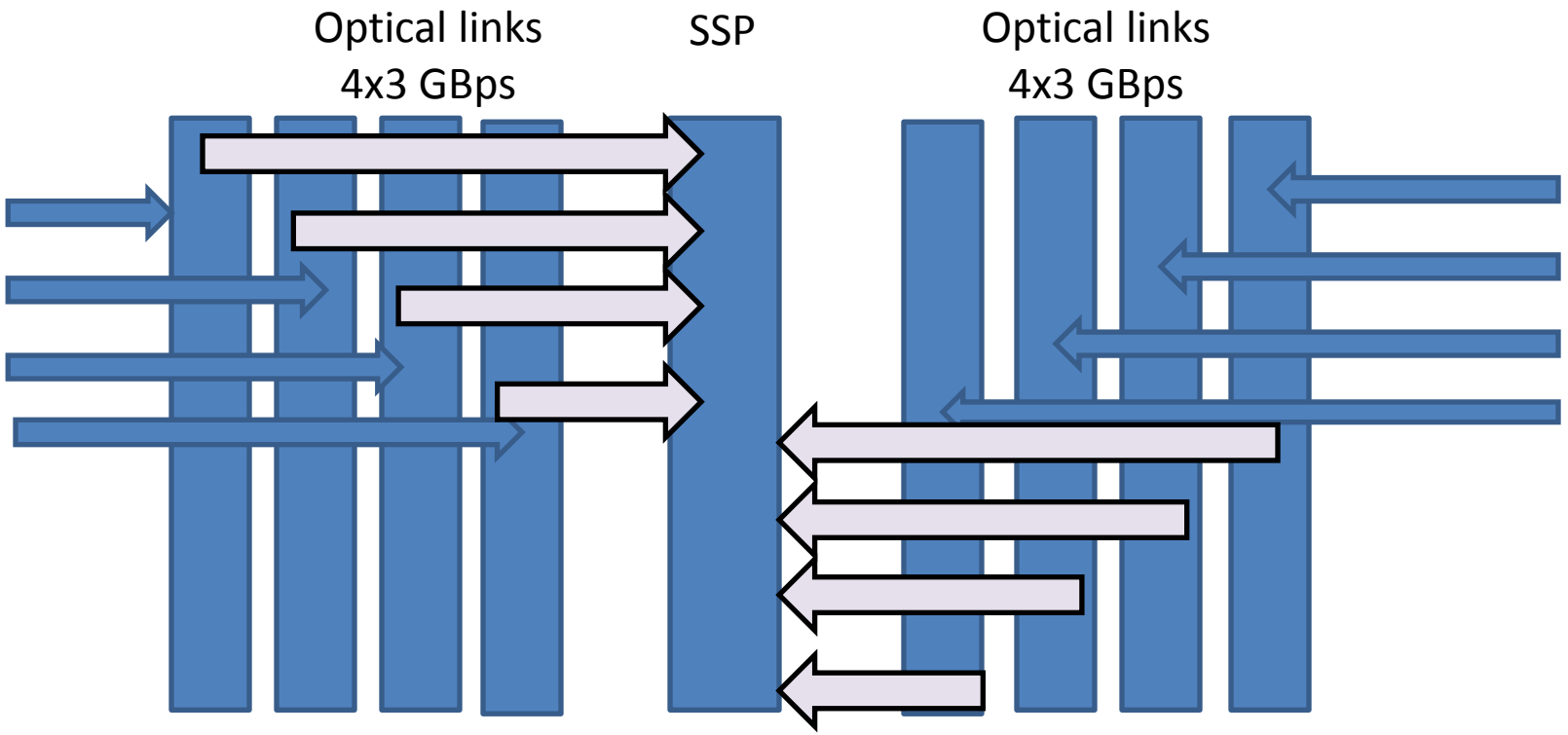
- Readout VME320 : 200 MB/s (5 times faster than Fastbus)

(1) Simple FPGA logic

- Fast, potentially no crate
- OR of all AND of a 3 channels

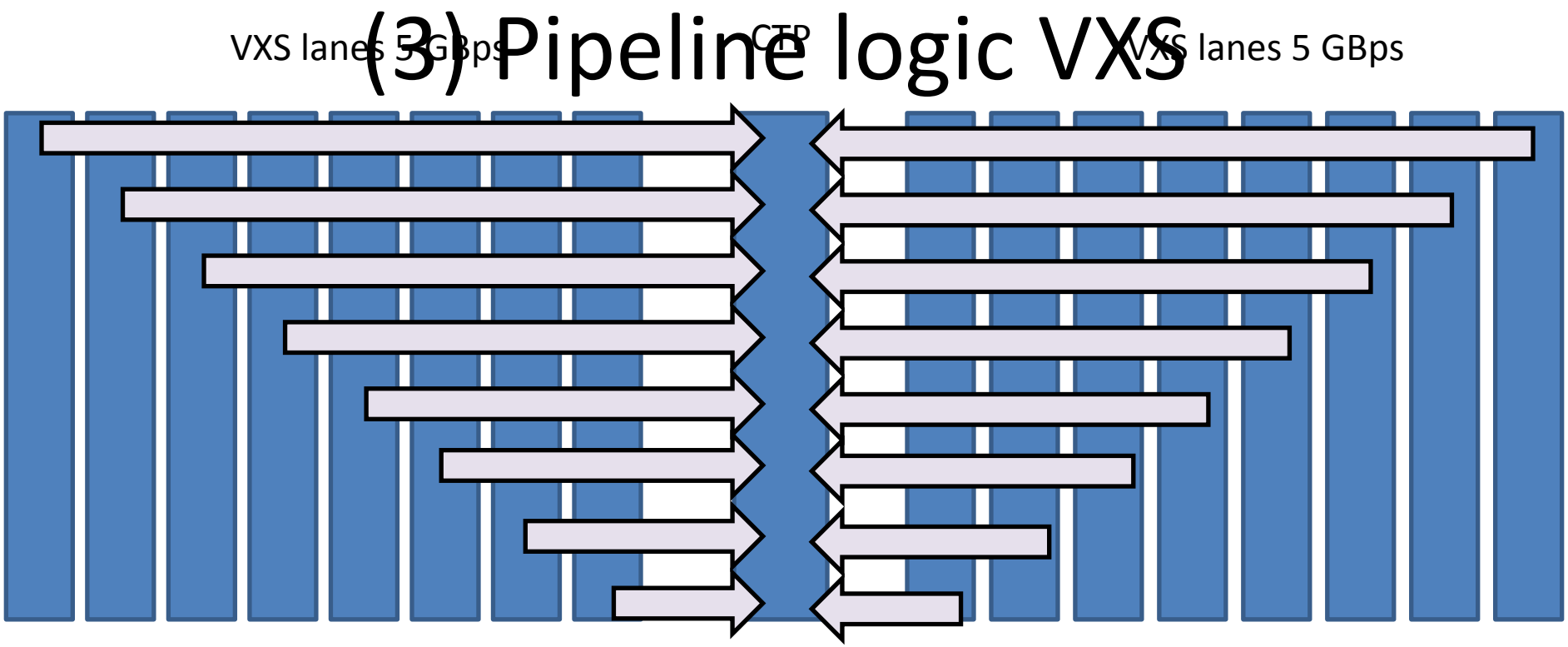


(2) Pipeline logic VME64X



Trigger latency :
250 ns (serialisation / deserialisation)
15 ns data
50 ns Processing
Trigger in about 350 ns for 1024 channels

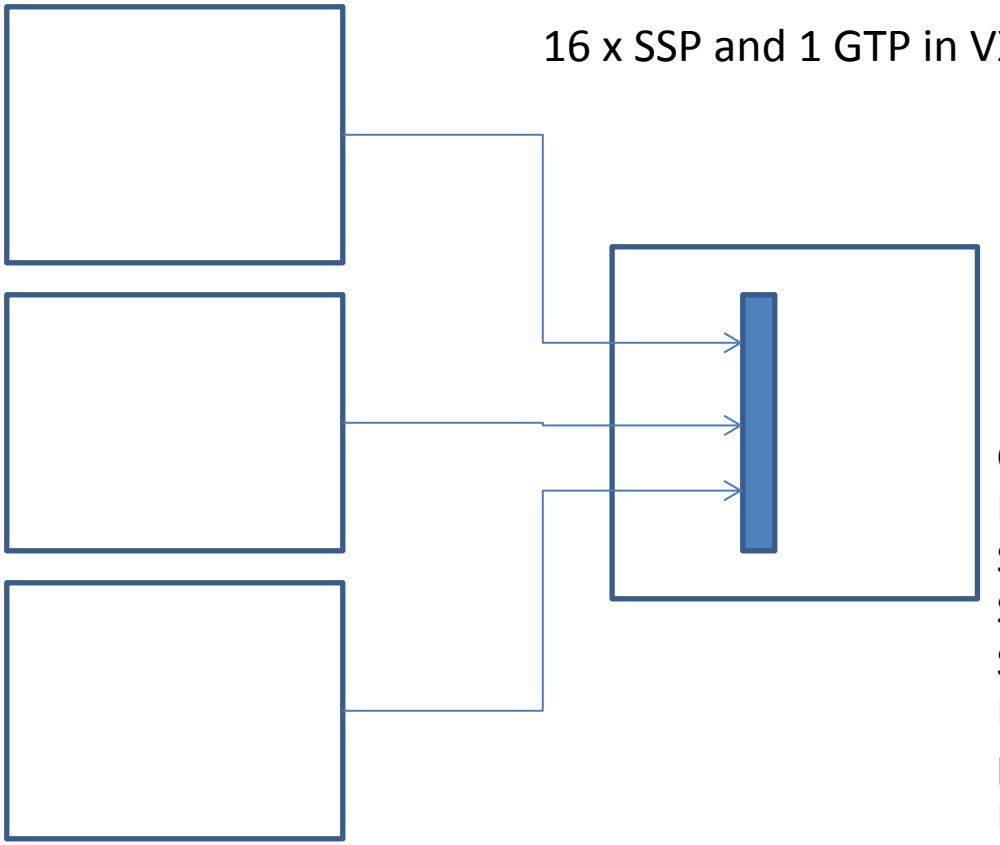
(3) Pipeline logic VXS



Up to 16 VETROC per VXS crates : 2048 channels

Trigger latency :
250 ns (serialisation / deserialisation)
15 ns data (128 bits per board)
50 ns Processing
Trigger in about 350 ns

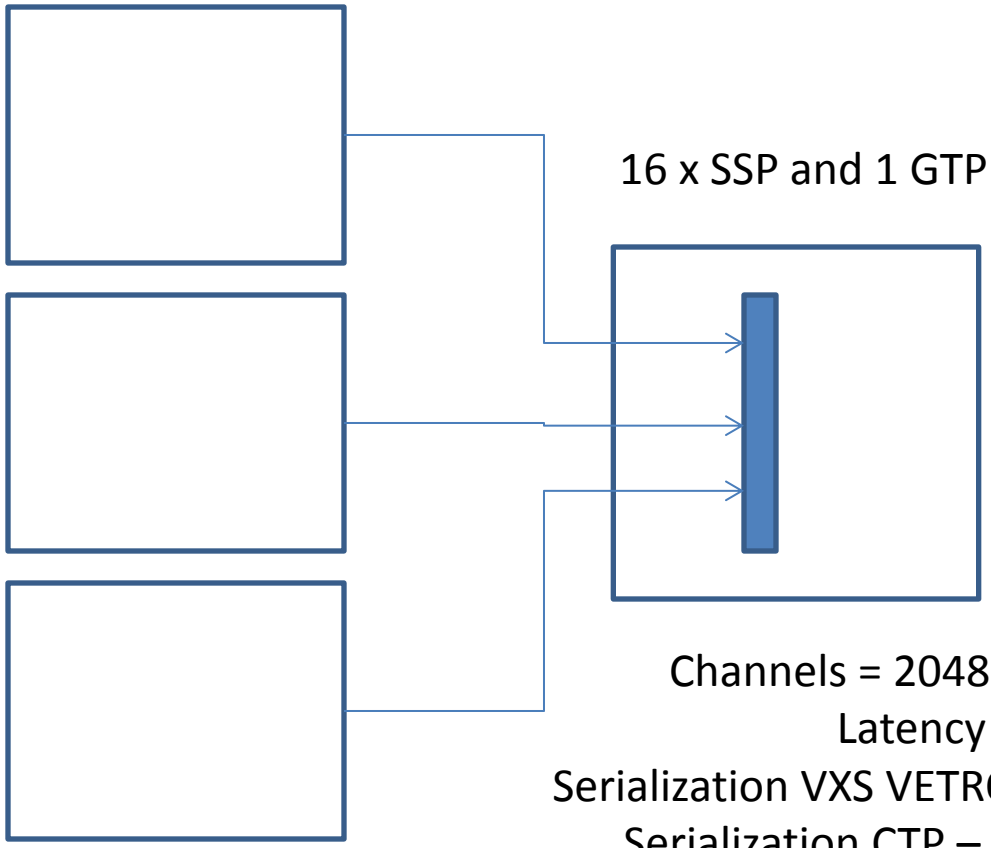
(4) Hybrid pipeline logic VXS



Channels = 2048 * crates
Latency
Serialization VXS VETROC-SSP 250 ns
Serialization SSP 250 ns
Serialization VXS SSP-GTP 250 ns
Data transfer = 2048 / 8 GBps = 256 ns per crate
Processing 500 ns
Trigger latency about 2 us for 2 crates

Up to 16*8=128 VETROC = 16384 channels

(5) Full fledge pipeline logic VXS



VETROC
VXS
Crates
16 VETROC
Per crate
=
2048

Up to 128 x 2048 channels
=
262,144

Channels = 2048 * crates
Latency
Serialization VXS VETROC-CTP 250 ns
Serialization CTP – SSP 250 ns
Serialization SSP-GTP 250 ns
Data transfer = 2048 / 8 GBps = 256 ns per crate
Processing 500 ns
Trigger latency about 2.3 us for 2 crates

Readout

- High resolution TDC available at readout stage (could be made available at trigger level but need redesign) : preliminary resolution 20 ps on 128 channels
- VME320 ：140 MB/s sustained
- Can fully take advantage of event blocking

GRINCH

- 550 PMT
- Option (2)
- 5 x VETROC = 5x4K$ =20 K$
- 1 VME64X crate = 8 K$
- 1 SSP = 5 K$
- 1 TI = 4 K$
- 1 CPU = 4 K$
- Total about 41 K$

RICH

- 2400 channels
- Option (4)
  - 1 VME64X crates = 8 K$ = 8 K$
  - 1 VXS crate = 15 K$
  - 2 CPU = 2 x 4 K$ =16 K$
  - 1 GTP = 6 K$
  - 2 TI = 2 x 3 K$ = 6 K$
  - 3 SSP = 3 x 5 K$ = 15 K$
  - 1 TD = 4 K$
  - 19 VETROC = 19 x 4 K$ = 76 K$
- Total = 146 K$

RICH

- 2400 channels
- Option (5)
  - 3 VXS crate = 3x 15 K$ = 45 K$
  - 2 CTP = 2 x 5 K$ = 10 K$
  - 3 CPU = 2 x 4 K$ =12 K$
  - 1 GTP = 6 K$
  - 3 TI = 2 x 3 K$ = 6 K$
  - 1 SSP = 5 K$
  - 19 VETROC = 19 x 4 K$ = 76 K$
- Total = 160 K$

RICH triggers

- Have all PMTs every 4 ns
  - Clustering
  - Ring ?
- If redesign of firmware logic to have high resolution at L1
  - Could have time over threshold and have amplitude at L1
  - Cut on single PMT amplitude
  - Threshold on digital sum all PMTs
  - Threshold on digital sum on ring or clusters

Conclusion

- VETROC can form prompt trigger and do readout
- Pipeline logic can be used for more complicated triggers (more latency around 300 ns) might be still fast enough for L1A within a crate, can be used for L2 with HCAL
- Cost ranges from
- High resolution readout developed 25 ps resolution
- Might be able to have high resolution at trigger level with investment