SBS DAQ

E. Cisbani / INFN Sanità

SBS DOE Review

7/Nov/2016 - GeorgeTown

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- *Mark Jones*
- *Paolo Musico*
- *…*
- *…*

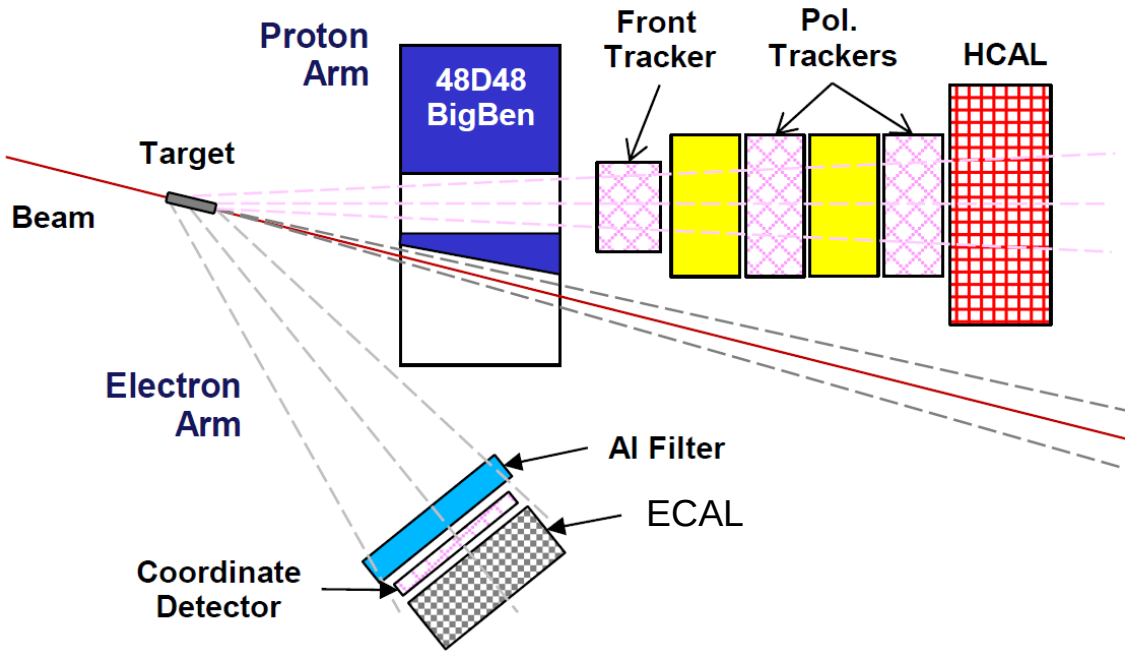
Outline
- **Experiment Rates**
- **Fastbus for SBS: performance**
- **Trigger and DAQ**
- **HCAL DAQ**
- **GEM readout**

Overview at SBS Meeting 20/Oct/2016 presentation is in progress …

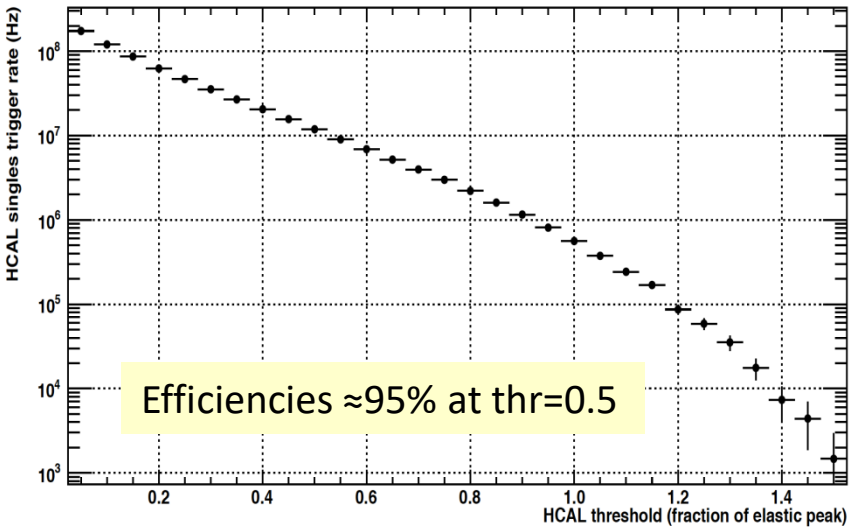
Main guidelines

- **Reuse available equipment (Fastbus) to reduce cost**
- **Exploit JLab CODA3 VME hardware largely based on powerful FPGA**
- **GEM processing in hardware**

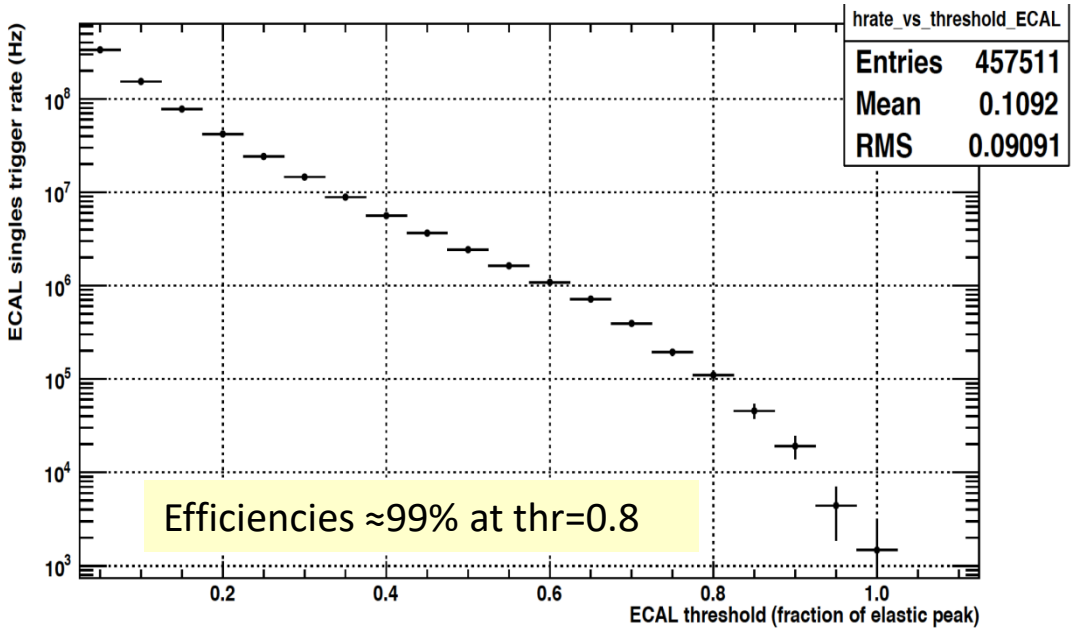
Most Demanding Rate - GEP experiment

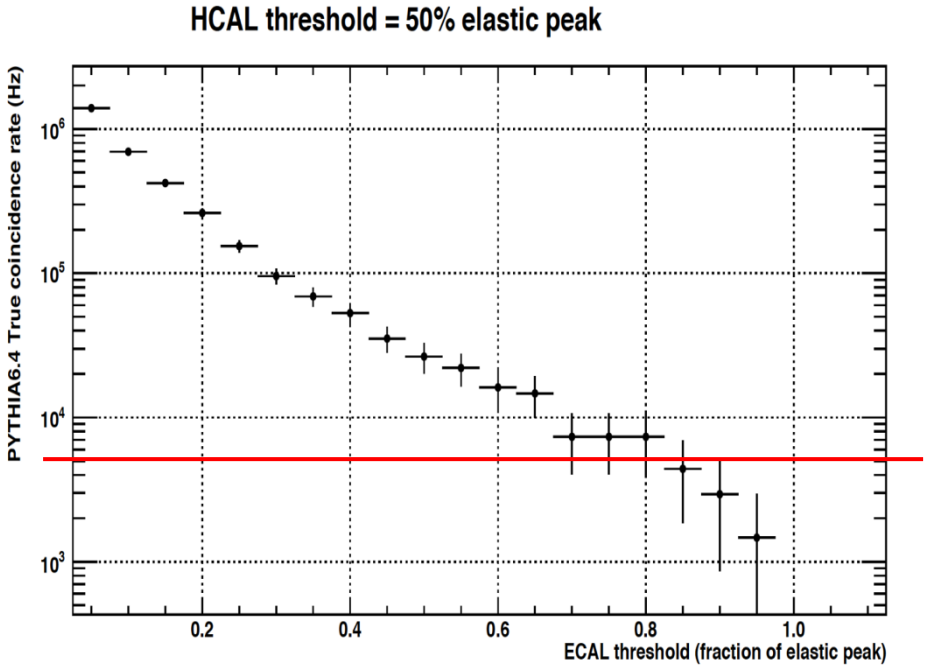


HCAL Singles: SLAC+DESY data in Wiser Code



ECAL Singles: from RCS exp (?)





DAQ Concepts

- Hybrid Fastbus & Pipelined Electronics
- **Level 1 Trigger**
  - latency ~100 ns (analog sum and discrimination)
  - originated by the ECAL electron arm (~200 kHz rate)
  - GATE for Fastbus and non-pipelined VME BigCal
- **Level 2 Trigger**
  - Latency ≤1.8 us (formation 0.8 us max + fast clear timeout ~1 us)
  - originated by electron ECAL & proton HCAL
  - 30 ns coincidence window at 9 kHz
  - *FPGA-based coincidence logic using elastic e-p geometrical constraints ⇨* ***2 kHz DAQ rate***
  - *FB & VME Fast clear after L2 timeout ⇨ 13% electronics dead time*

DAQ configuration for SBS GEP experiment

GEp Detectors	Channels	Readout	Type
SBS Proton arm			
Front tracker (6 GEM chambers)	41,472	APV25 MPD	VME
Rear tracker (10 GEM chambers)	61,440	APV25 MPD	VME
HCAL	288	FADC 250	VME
Electron arm			
ECAL	1710	ADCs 1881M	Fastbus
ECAL sums	219	TDCs 1877S	Fastbus
CDET	2688	TDCs 1877S	Fastbus

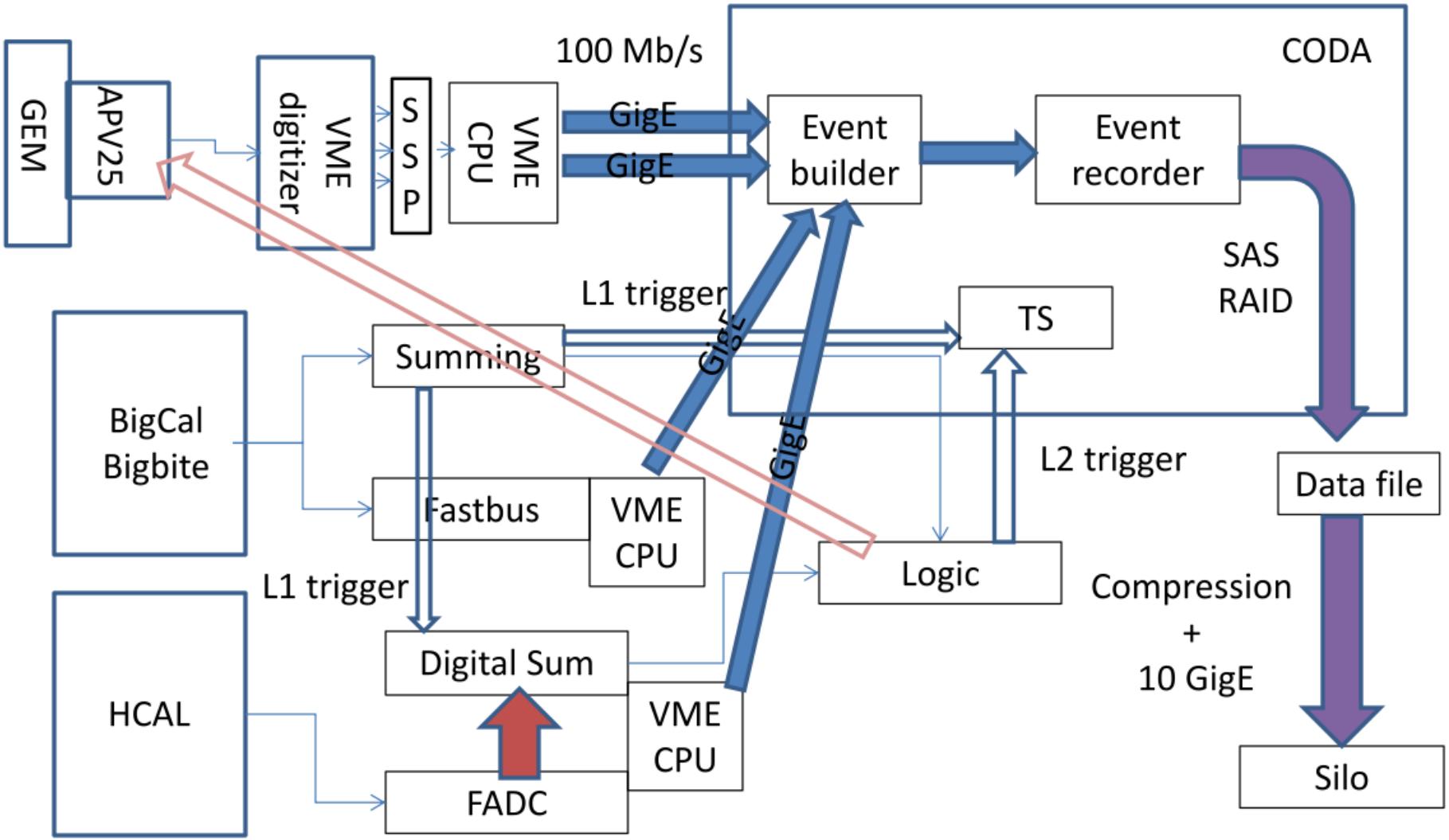
- Reuse the NIM and Fastbus equipment already available at JLab
- Lot's of channels on VME, Fiber Optics and new CODA

Additional components (modules):

- SSP: Sub-System Processor:
- TS: Trigger Supervisor / TI: Trigger Interface
- GTP: Global Trigger Processor / CTP: Crate Trigger Processor
- SD: Signal Distribution
- VETROC: Trigger and Digital Readout
- VTP: VXS-Trigger Processor

Slide needs improvements

DAQ Data Flow



SILO : LTO7 since 2015 , 6.25 TB per tape and 300 MB/s per arm
Network upgradeable to 40 Gbit when cost effective

FASTBUS for ECAL and CDET

Struck Fastbus Interface (SFI) is the Fastbus Master (18 available at JLab)

- Allows control the Fastbus modules through any VME CPU (Intel or old vxworks)
- Has slot for standard JLab Trigger Interface Module

New TI's for all ECAL e CDET Fastbus crates

Amplitude: 64 channel Lecroy ADC 1881M (113 available at JLab)

- 9μs encoding time in 12 bit resolution and 12μs in 13 bit resolution.
- use the FAST CLEAR feature: module is ready to accept another event after 1ms.

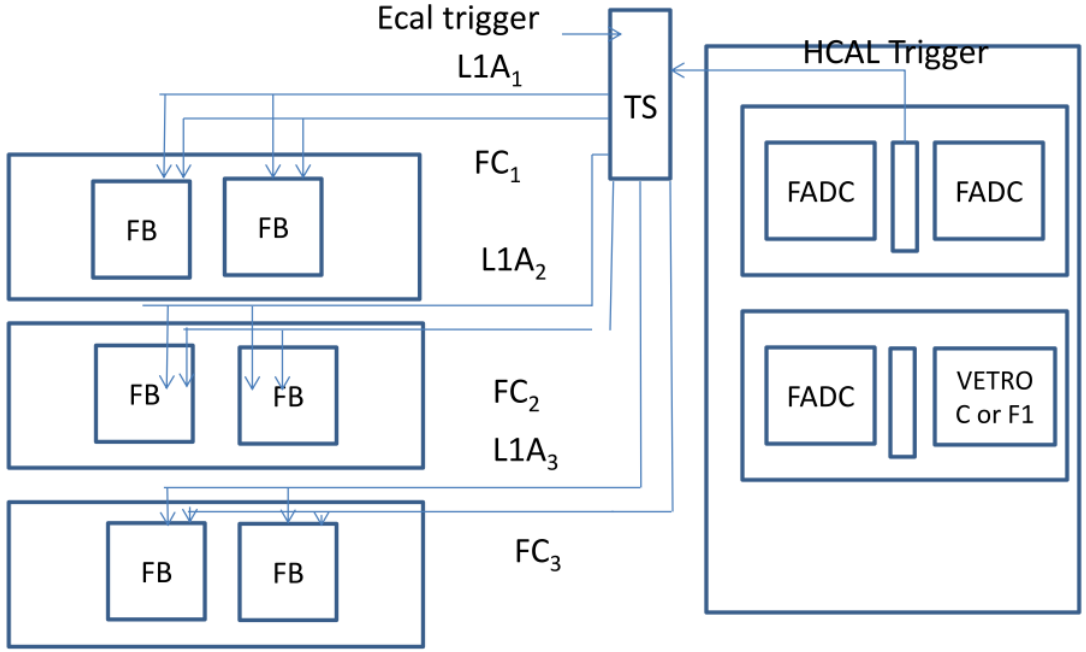
Time: 96 channel Lecroy TDC 1877s (236 available at JLab)

- Built-in Data Zero Suppression and Data Compaction (sparsification)
- Capable of multihit with an event buffer of 8 events.
- Encoding time 1.7μs plus 50 ns per hit per channel giving a maximum encoding time of 78μs.
- FAST CLEAR settling time < 250ns

Fastbus Crates holds up to 25 modules
(30 available at JLab)

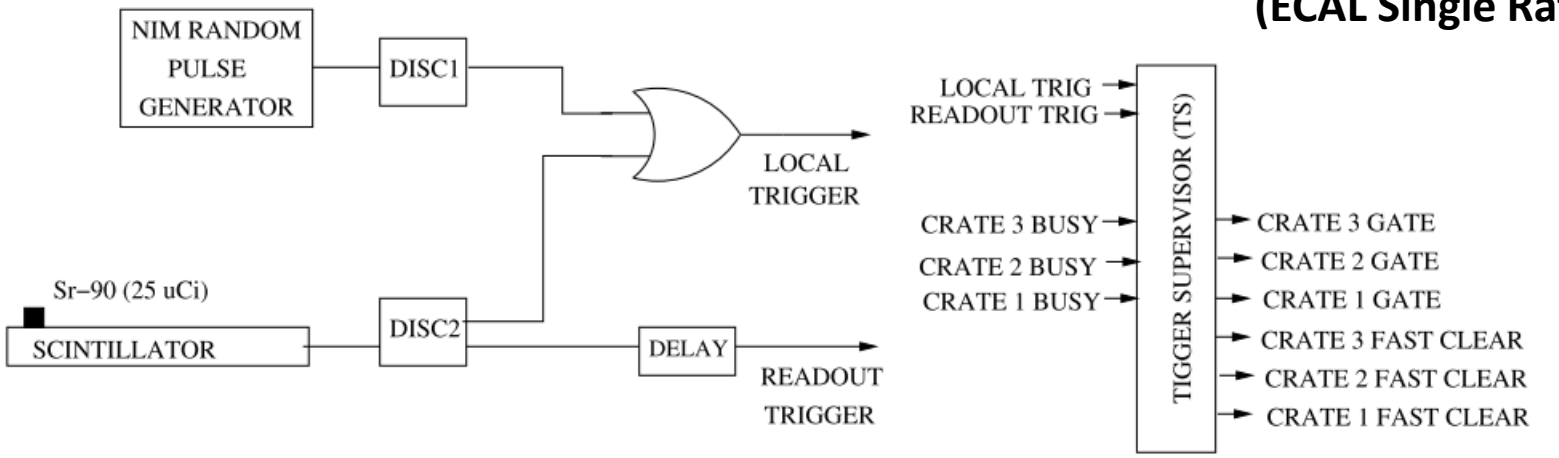
Fastbus standard transfer rate:
40 MB/s (sustainable 15 MB/s)

Plenty of FASTBUS modules:
-> use:
event switching (3 to 1)
sparsification, event blocking



ECAL/Fastbus – Event Switching Dead Time Study

(ECAL Single Rate ~200 kHz)

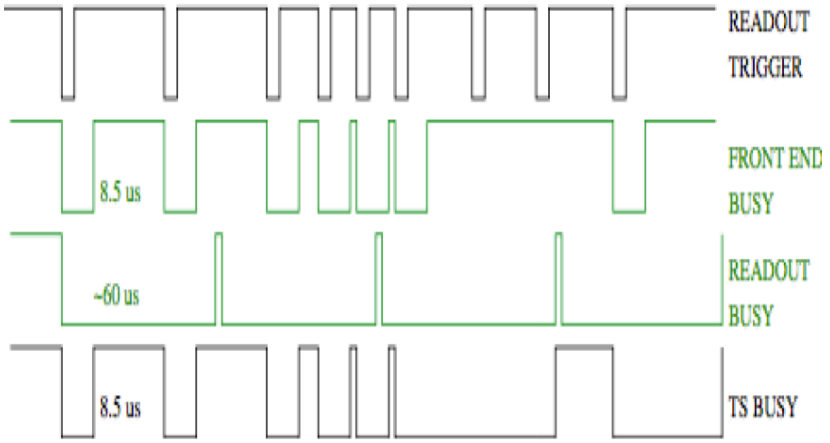


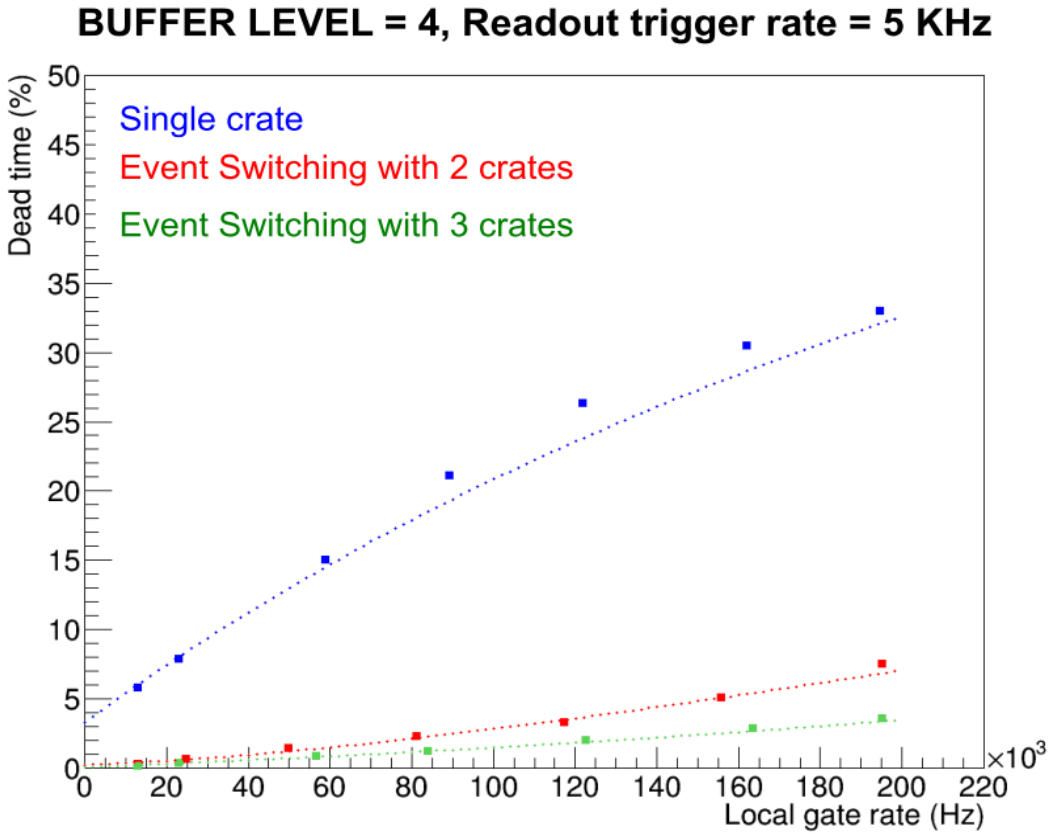
Local Trigger = L1

Readout Trigger = L2

Reading 6 channels in each ADC

Buffer Level = 4; up to 4 events can be processed while system is busy





New TS Firmware

- New firmware implementing event switching in the TS up to 4 branches
- Inputs:
  - T1 Lvl 1 trigger, T2 Lvl2,
  - 4 busy inputs, 4 fast L1, 4 Fast Clear output
- A single TS for synchronization
- Single data stream
- Fully compatible with event blocking
- New TIs for Fastbus
- 250 MHz clock distribution on fiber : absolute timestamp and counters on the new TI (replace scalers)

VETROC

- VETROC : VXS Electron Trigger Read Out Controller
  - Logic input and output pipeline board up to 192 channels
  - Optical link and VXS port to communicate with other pipelined electronics
  - FPGA programmable logic
  - Will be used to input the ECAL sum to the trigger module for geometrical matching of ECAL and HCAL
  - Prototype being tested
  - 2 boards procured for SBS

VTP

- VTP : VXS Trigger Processor
  - New generation of Trigger Processor
  - Larger FPGA than previous CTP and GTP
  - Will do HCAL clustering and geometrical matching with ECAL
  - Allow readout of modules through VXS increasing the bandwidth to 16x8 Gbit /s could be used for FADC fast readout or SSP if required
  - On board processor
  - Board received, firmware and interface are being implemented

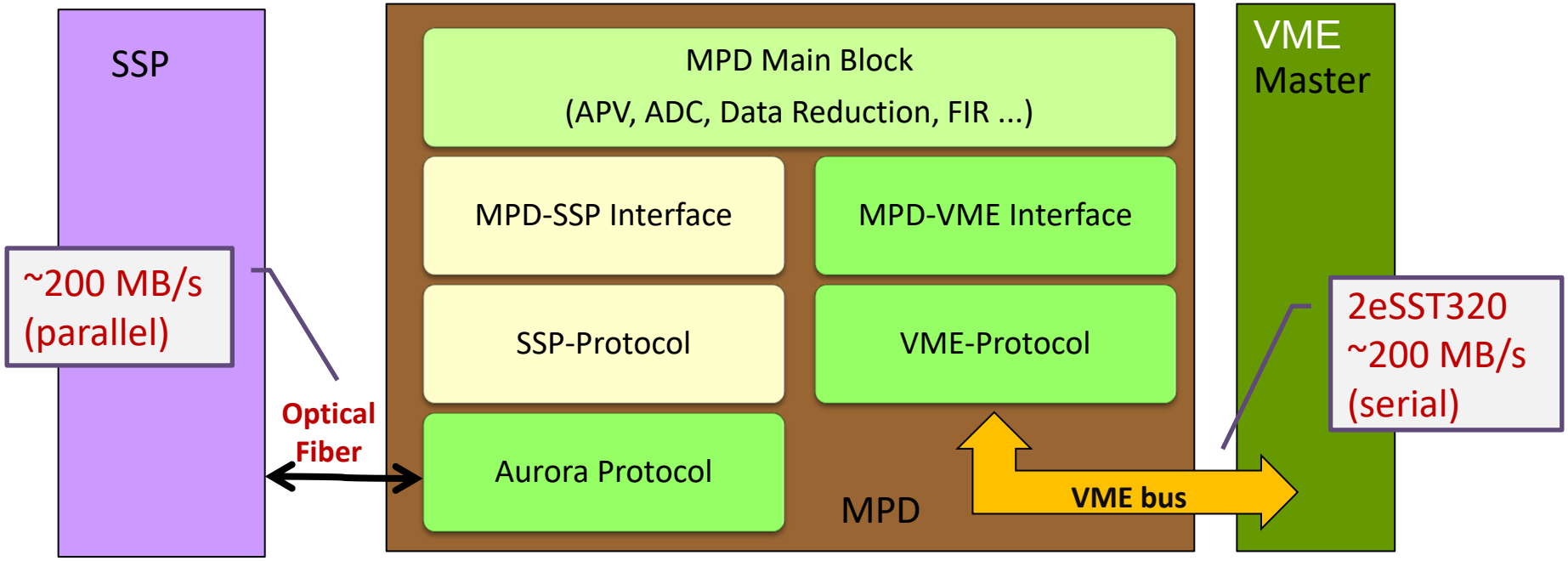
GEM – Readout Electronics

- 128 analog ch / APV25 ASIC
- 3.4 μs trigger latency (analog pipeline)
- Capable of sampling signal at 40 MHz
- Multiplexed analog output (100 kHz readout rate)

	Channels	APV25	MPDs
Front Tracker	41472	324	24
Rear Tracker	61440	480	34

- **Up to 16 APV25 cards (2048 chs) on a single MPD (parallel readout)**
- Altera Arriga GX FPGA / RAM: DDR2 (128 MB)
- **Optical Fiber Link interface (Aurora ~2 Gb/s peak)**
- 110 MHz system clock and Front panel coax clock
- Used HDMI-A for analog and digital signals
- **VME/32, VME64, VME64-VXS compliant (up to 200 MB/s peak)**
- 4 high speed line on the VXS available for data transfer
- Firmware v. 4.0 (74% resources):
  - Finite-Impulse-Response Filter (16 parameters)
  - Zero Suppression (sparse readout)
  - Common mode and pedestal subtraction
  - Remore reconfiguration
  - ~2 ns trigger time resolution
  - VME / Optical Fiber simultaneous implementation

MPD Status (version 4.0)



- All VME cycles tested in Italy (STRUCK SIS-3104 controller) and in JLab DAQ except 2eSST
  - Measured data transfer speeds agree with simulations
  - 2eSST in JLab show data misalignments (firmware/software debugging)
- Optical link MPD – SSP:
  - MPD can be configured by SSP; data transfer still suffer some misalignments but all data are readout
- CODA system (Intel CPU + SSP) now running in Italy
  - deep tests MPD – VME – SSP are in progress

GEp: GEM Data rate

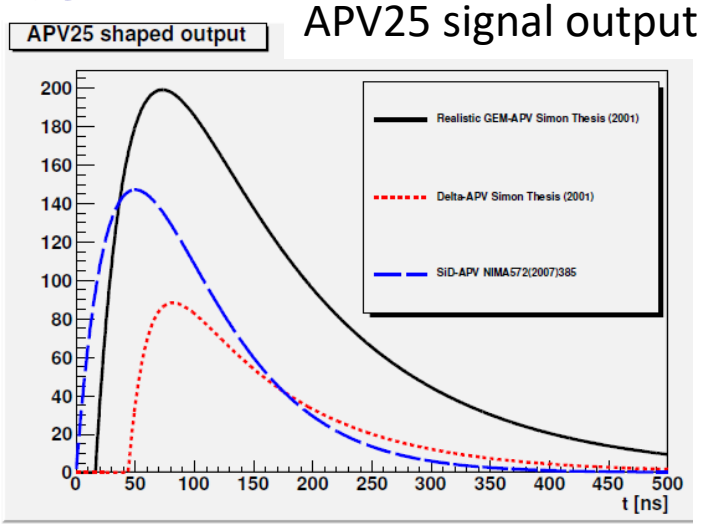
Tracker	Area of interest for tracking, cm^2	Rate, kHz/cm^2	Strip pitch, mm	Strip occupancy, %	Number of pseudo-tracks per event	Number of strip planes
First	0.20 x 18	400	0.4	13.5	1.65×10^{-2}	12
Second	2π 0.35^2	130	1.6	7.4	8.7×10^{-3}	8
Third	π 4.8^2	64	1.6	3.6	5.2×10^{-4}	8
BigCal	π 1.2^2	173	1	2.4	2.8×10^{-2}	2

CDR rate estimation

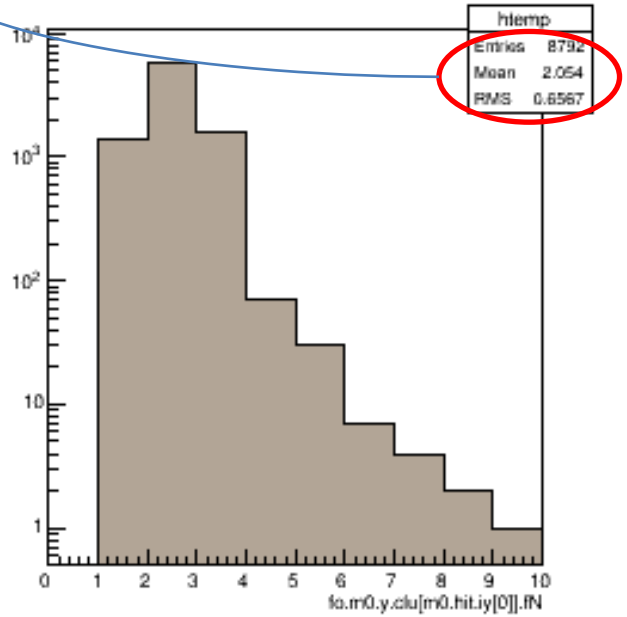
- Expected Hits Rate (Front Tracker): ~ 500 kHz/cm2
- GEM signal width: ~ 250 ns
- Cluster width (MIP particles): 2.5 strips
  - ➢ Strip Occupancy: 60%
- Samples/Events: 3
- Bits/Sample = 24 = 12 ADC + 7 CH-APV + 5 CH-ADC
- Trigger rate: 5 kHz
  - ➢ MPD-SSP Transfer Rate: **45.2 MB/s** (after sparsification)

200 kHz/cm2 Rear Tracker – same occupancy and transfer rate

APV25 signal output



Cluster Width

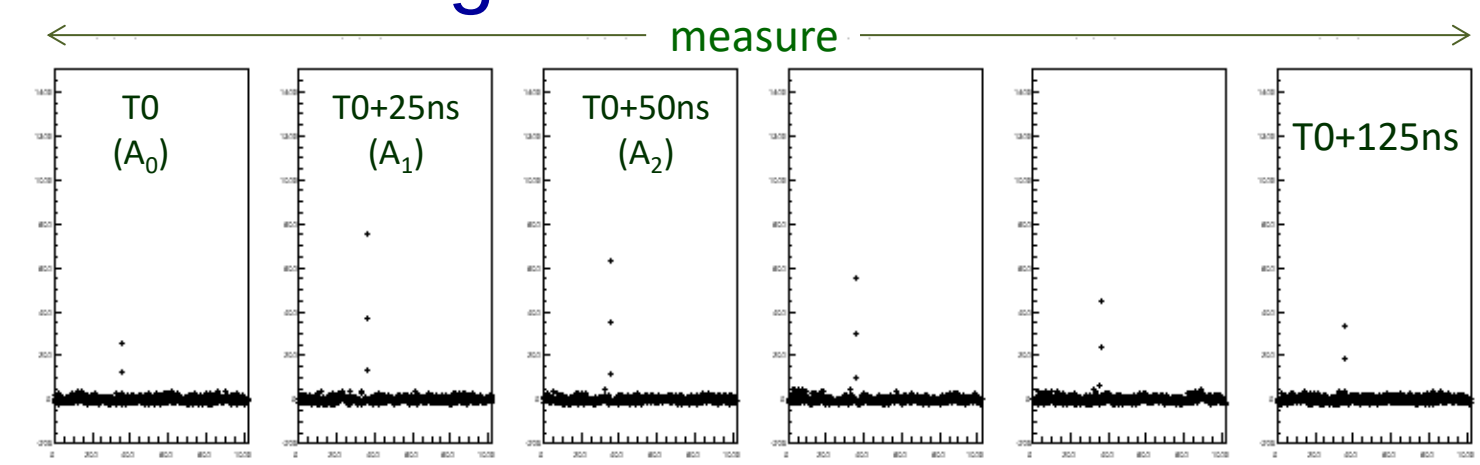


SSP to DAQ-CPU data rate is 200 MB/s (VME bus)
→ require MPD/SSP=4 and SSP/VME64_crate=1
FEASIBLE BUT NOT EFFORDABLE!

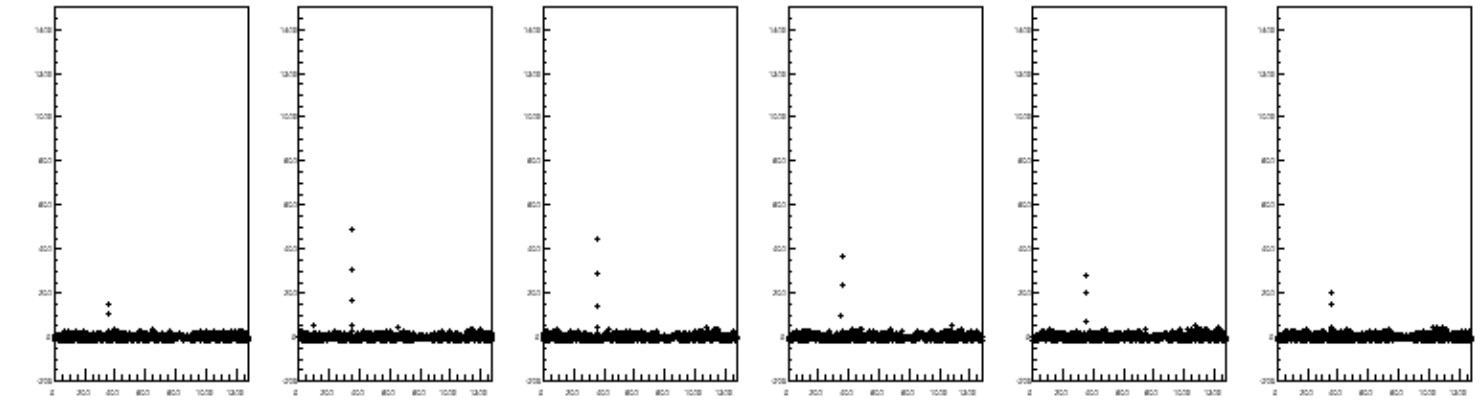
We must connect 14-16 MPD to a single SSP
⇨ need data processing on SSP (and MPD), reduce data by factor of ~10 (<30% dead time)

Better Time-Correlation, e-p geometrical constraints, x/y clustering with charge/time correlation

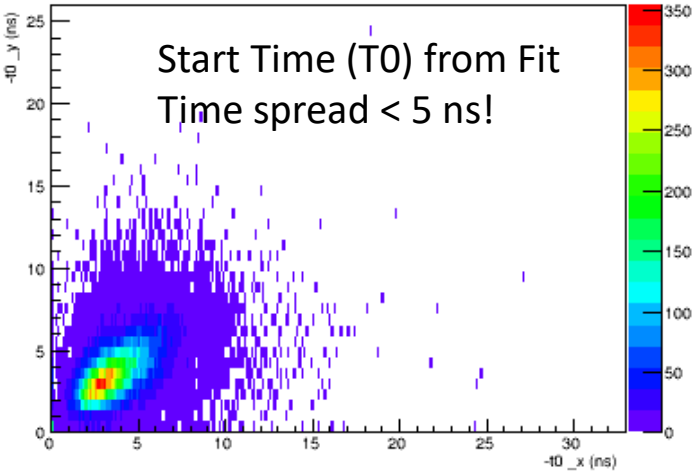
GEM Signal Deconvolution / 2014 Test Data

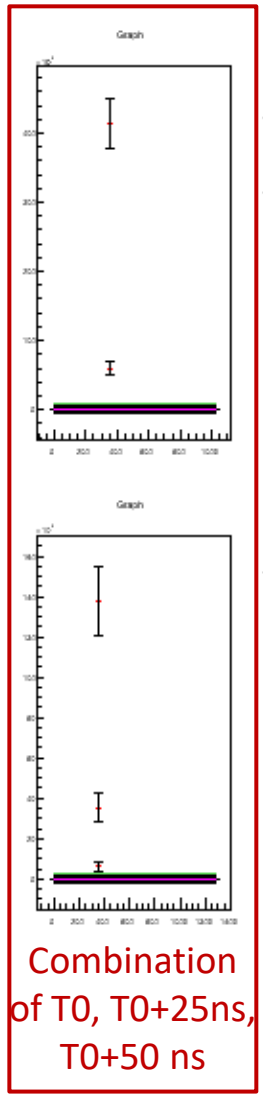


x - Strips

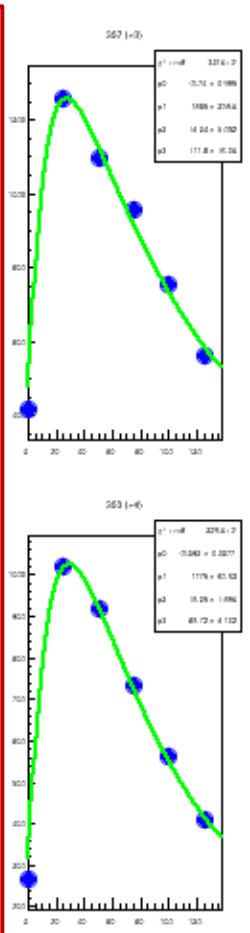


y - Strips





Combination of T0, T0+25ns, T0+50 ns



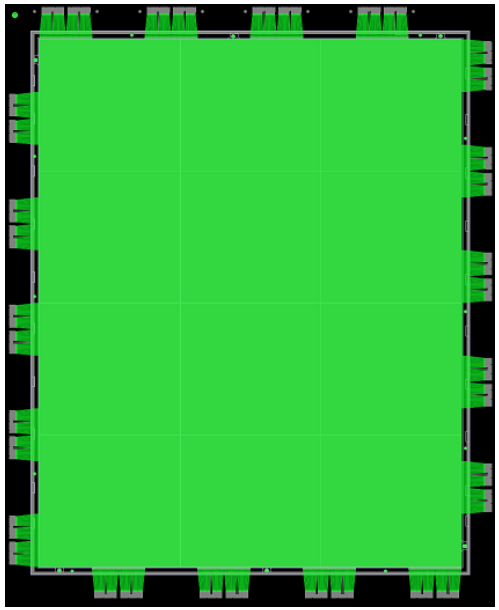
Fit of 6 samples

$$A_1 \cdot A_2 \cdot [A_1 + A_2 - A_0] \cdot (A_1 > 0) \cdot (A_2 > 0) \cdot$$
$$[(A_1 - A_0) > 0] \cdot [(A_2 - A_0) > 0] \cdot$$
$$\left[(A_1 - A_2) < \left(\frac{A_1 + A_2}{2} - A_0\right)\right] \cdot \left[(A_1 + A_2) > 2\sqrt{RMS_{ped}}\right]$$

«Simple» combination of 3 samples enhances the SNR
6 samples fit provides excellent time correlation

GEM / Additional firmware processing

- Geometrical matching
  - VTP has information on e-p geometrical matching by ECAL and HCAL
  - VTP send a special pattern to GEM-SSP's
  - SSP filter APVs according to geometrical matching (1 APV = 5 cm), e.g. 4 APV along each axis (20 cm x 20 cm) suppress FT data by a factor of 0.15 !



Work in progress …

APV Signal Analysis for Hit Discrimination in Firmware

GOAL: Find a simple and robust function (to be implemented in firmware) that can discriminate real hits from background

Try: Artificial Intelligence methods (AI)

Select (unbiased) learning subsets of the data (signals and noise)

Use Neuro-Genetic Programming (Brain Project) to determine the optimal function that approximate the experimental data (symbolic regression)

M. Russo, «A distributed Neuro-Genetic Programming Tool», Swarm and Evolutionary Computation 27 (2015) 145-155

Validate on a large set of data

«Brain Project» provide a simple function of the data samples

One PhD student (L. Re) workin on that in Catania/Italy
Supervisioned by M. Russo

Data Storage

		Days	Data rate MB/s	Seconds	Total data TB	Double	LTO5 in $	LTO6 in $	LTO7 in $
E12-12-09-019	GMN	25	1000	2160000	2160	4320	216000	129600	86400
E12-09-016	GEN	50	1000	4320000	4320	8640	432000	259200	172800
E12-07-109	GEP/GMP	45	1000	3888000	3888	7776	388800	233280	155520
E12-09-018	SIDIS	64	1000	5529600	5529.6	11059.2	552960	331776	221184
	Total	184		15897600	15897.6	31795.2	1589760	953856	635904
Actual days	Actual years		Time in s						
368	1.01	184	15897600					Total	635 K$

LTO7 since 2015 : 300 MB/s per arm (up to 15) and 6.25 TB per table uncompressed

Cost was divided by a factor of 2 : 500 MB/s reasonable, 1 GB/s doable if needed for about 635 K$ of tape split over several years and cost expected to go down

Network link upgrade to 10 Gbit/s = 1.25 GB/s possible: possibility for L3 farm in computer center

DAQ: Man power

	Coordination	VME-DAQ	Fastbus	HCAL-Trigger	GEM-MPD	BigBite
A. Camsonne	X			X	X	
M. Jones			X			
D. Adikaram			X			
J. Gu			X			
S. Malace			X			
B. Moffit		X	X		X	
B. Raydo		X		X	X	
S. Riordan					X	
D. Di					X	
E. Cisbani					X	
P. Musico					X	
E. McLelan			X			X

DAQ: Short Term plan

- Parassitic test run during DVCS/GMp experiment
  - Some description
- GEM/MPD-SSP/CODA Integration
  - Finalizing tests and correct potential bugs
- Software
  - Ongoing study of GEM firmware data processing
- xxx
  - yyy
- zzz

Summary

Trigger:

- …
- ….

Fastbus:

- Sparsification, event buffering and crate switching to reduce dead time – works!

VME:

- FADC amplitude and time information for HCAL
- MPD + Optical Link + SSP under testing
- “Smart” processing in MPD and SSP to reduce data by 1/10

JLab CODA3

- hardware/software framework integration in progress