Minutes: SBS Meeting March 9, 2016

Agenda: Todd - Update on GRINCH
Vitaly - SBS CDet module construction
Brian - HCal electronics with UVa summing modules

Attendees: Brian Quinn, Gregg Franklin, Todd Averett, Vitaly Baturin, Mark Jones, Mitra Shabestari, Dasuni Adikaram, Peter Monaghan, Gordon Cates, Andrew Puckett, Carlos Ayerbe Gayoso, Dipangkar Dutta, Kieran Hamilton, Seamus Riordan, Tommy Miller, Alexandre Camsonne, Bogdan Wojtsekhowski.

Todd - Update on GRINCH detector

- Received the vessel in January
- Work on PMT array is in progress
- Mirror assembly is complete; working with ECI on coating aluminum.
- Wavelength shifting paint-measuring absorption and emission spectra
- Gas panel is complete
- DAQ work is in progress:
  - Fastbus TDC and ADC system working with prototype GRINCH in TestLab
  - VETROC FPGA system initial tests complete; allows GRDINCH trigger
  - Single event display is working
- To Do:
  - Test VETROC with prototype detector in ESB
  - PMT Array: Seal seams, mirror coat iron plates, re-assemble, install PMTs leak test
  - Vessel: Seal all seams & bolts, install rail system, install windows, install mirrors
  - Coating and alignment of mirrors
  - PMTs: Finish WLS paint studies and coat all tubes
  - DAQ: Finish prototype tests, assemble full system
  - HV: Construct distribution system
  - NINO cards: Construct mounting system

Vitaly - SBS Coordinate Detector fabrication status

- Discussing one of the CDet modules
- Reviewing the assembly progress of the 14-scintillator block
- Discussing the construction of the 16-fiber bundles
- Central module was assembled before Christmas
- To Do:
  - Fabrication of Scintillator blocks in progress
  - Fiber bundle fabrication/ polishing
  - Precision Scintillator module assembling techniques need to be developed

Brian - HCal electronics with UVa summing modules

- HCal Electronics test with First-level ECal trigger
- Discussing the test results of the U.Va. 36-fold summing module
- To Do / Open Questions:
  - Continue discussion with Chris/Mark to see whether anything clever is possible, or whether modest custom module/board is practical.
  - Consider construction of patch-panel/asymmetric splitter
  - Understand 16-input summing circuits (18 needed plus spares)
    ~20 ns walk acceptable for ECal trigger? Monte Carlo pileup effects
  - Decide whether amplifiers are needed (available? 288 chan)
    Current due to signal rate + bkg for ~0.2 to 1.0 V signal?
  - Consider options for housing/power for NINOs Location? Are long LVCS cables acceptable?