SBS Data Acquisition

Jens-Ole Hansen

SBS Collaboration Meeting

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SBS DAQ Requirements

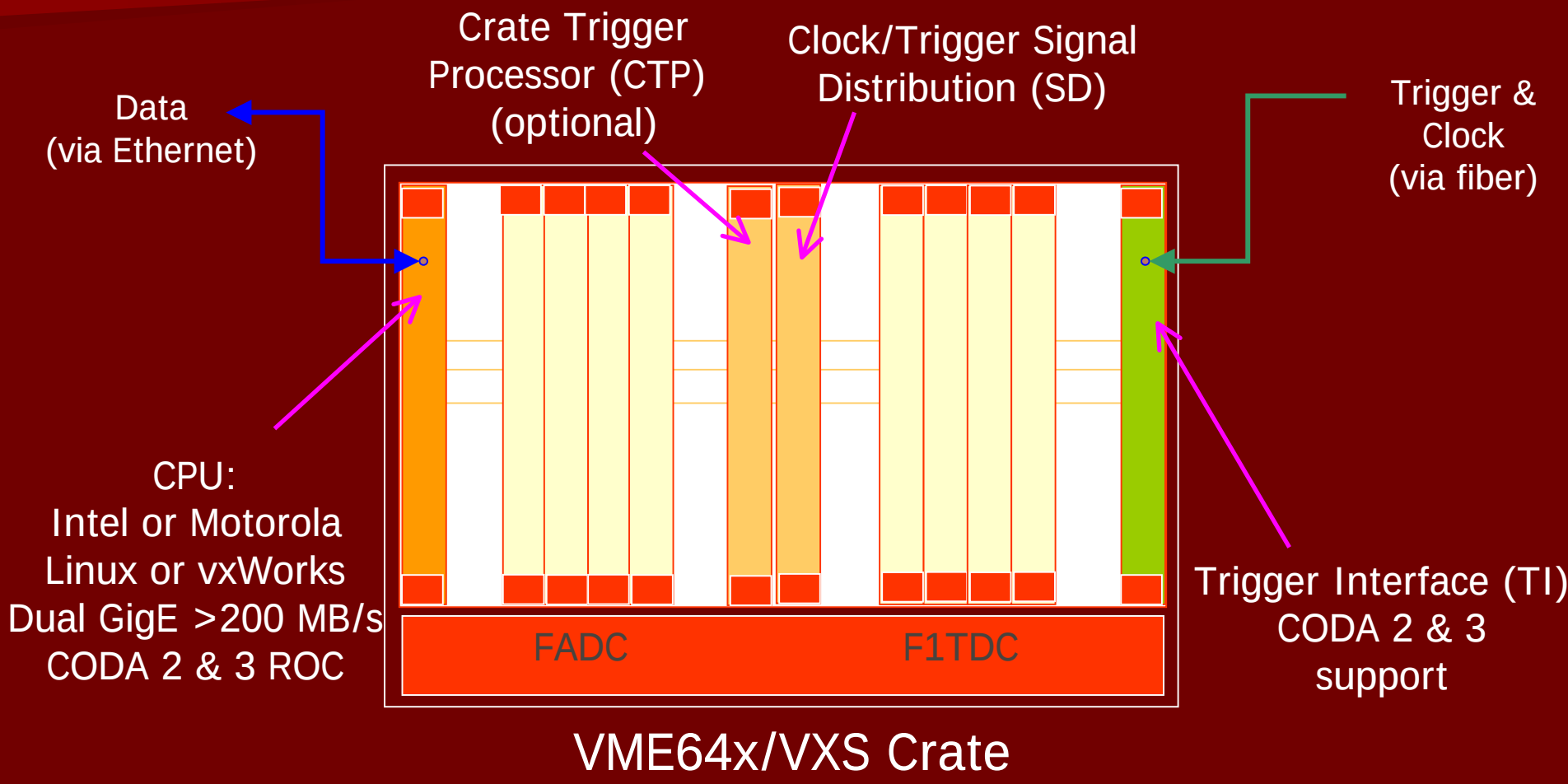
- Data rate driven by GEMs:
  - 65000 channels, 10% occupancy, 2 bytes/channel
  - 13 kB event size @ 5 kHz = 65 MB/s
- Add other detectors, higher trigger rates ...
- Far exceeds current Hall A capabilities
- Need 12 GeV DAQ upgrade to meet the requirements
  - Plan exists for Hall A
  - http://hallaweb.jlab.org/equipment/daq/daq_12gev.pdf

JLab 12 GeV DAQ Upgrade

- Geared towards GlueX
- 200 kHz L1 trigger rate capability
- Deadtime-less electronics (fully pipelined)
- VME64x front-ends with support for
  - High-speed readout modes (2eVME, 2eSST) up to 200 MB/s
  - Event “blocking” (buffering, caching) - up to 200 events
  - Custom serial (VXS) bus:
    - Bi-directional trigger path
    - Optional data path
  - Trigger blocking
  - (Trunked) Gigabit Ethernet or VXS fiber uplinks to event builder
- Synchronous trigger distribution, 250 MHz ref. clock

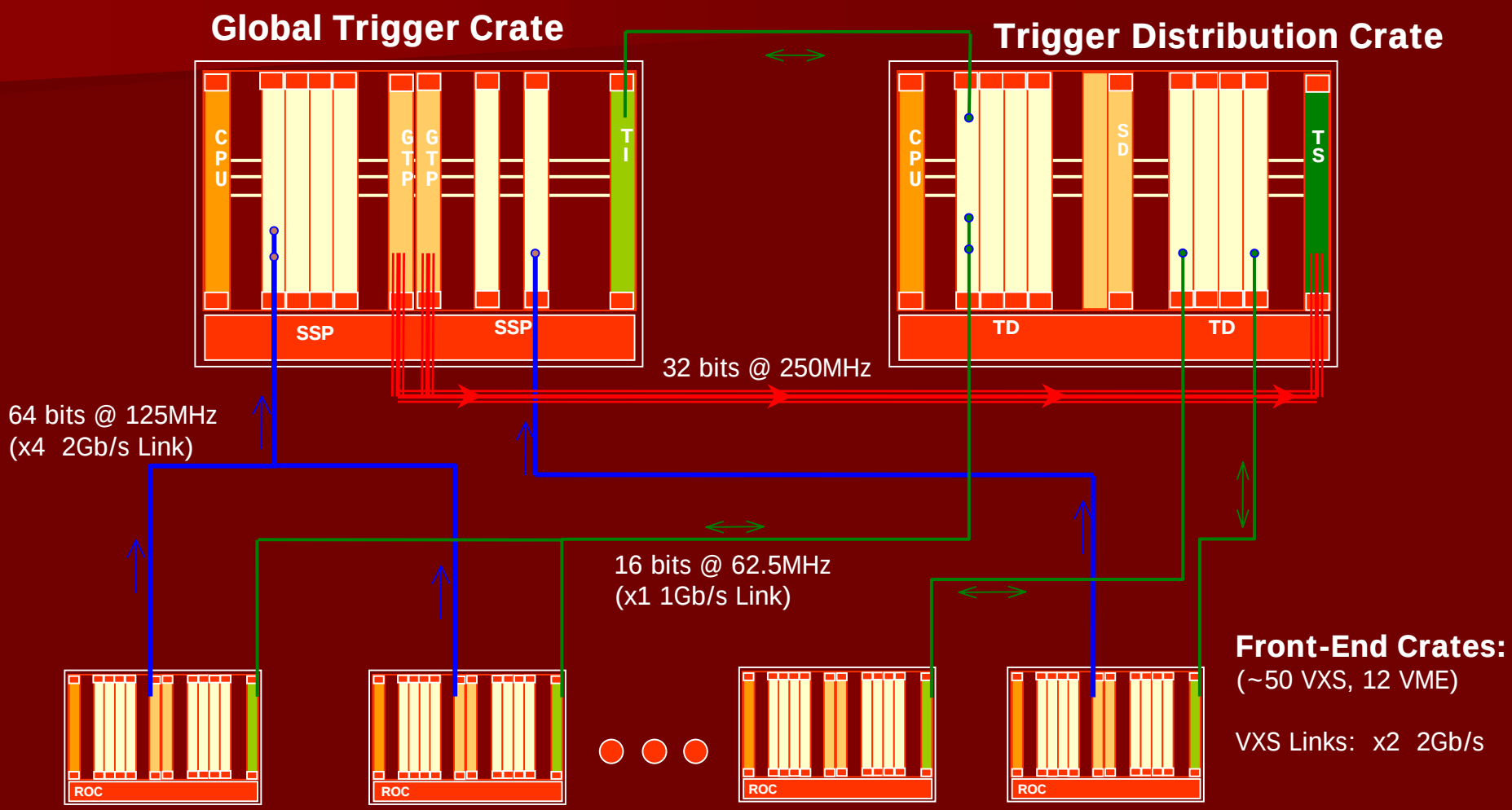
Future Front Ends

(graphics from Dave Abbott)

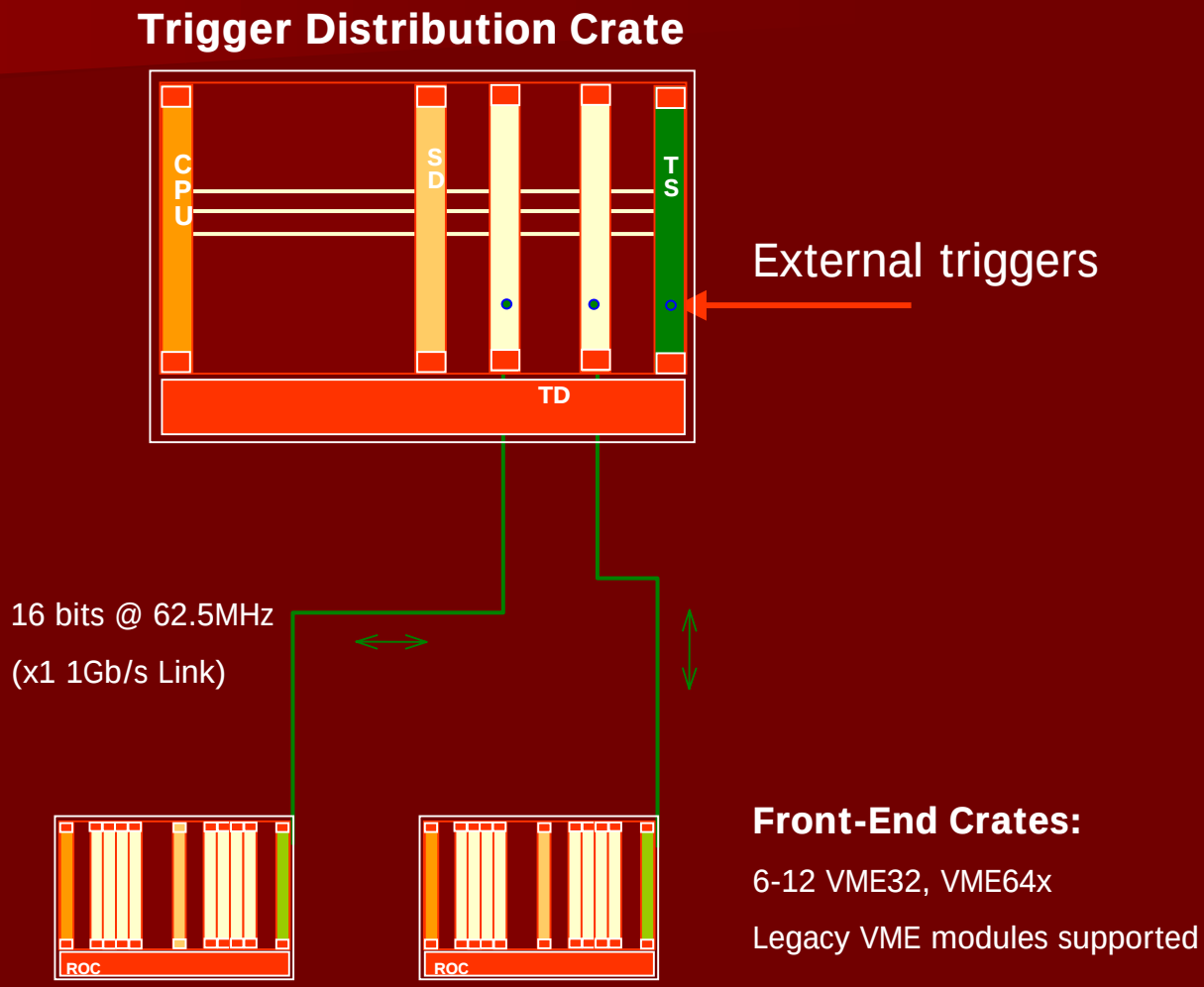


GlueX L1 Trigger

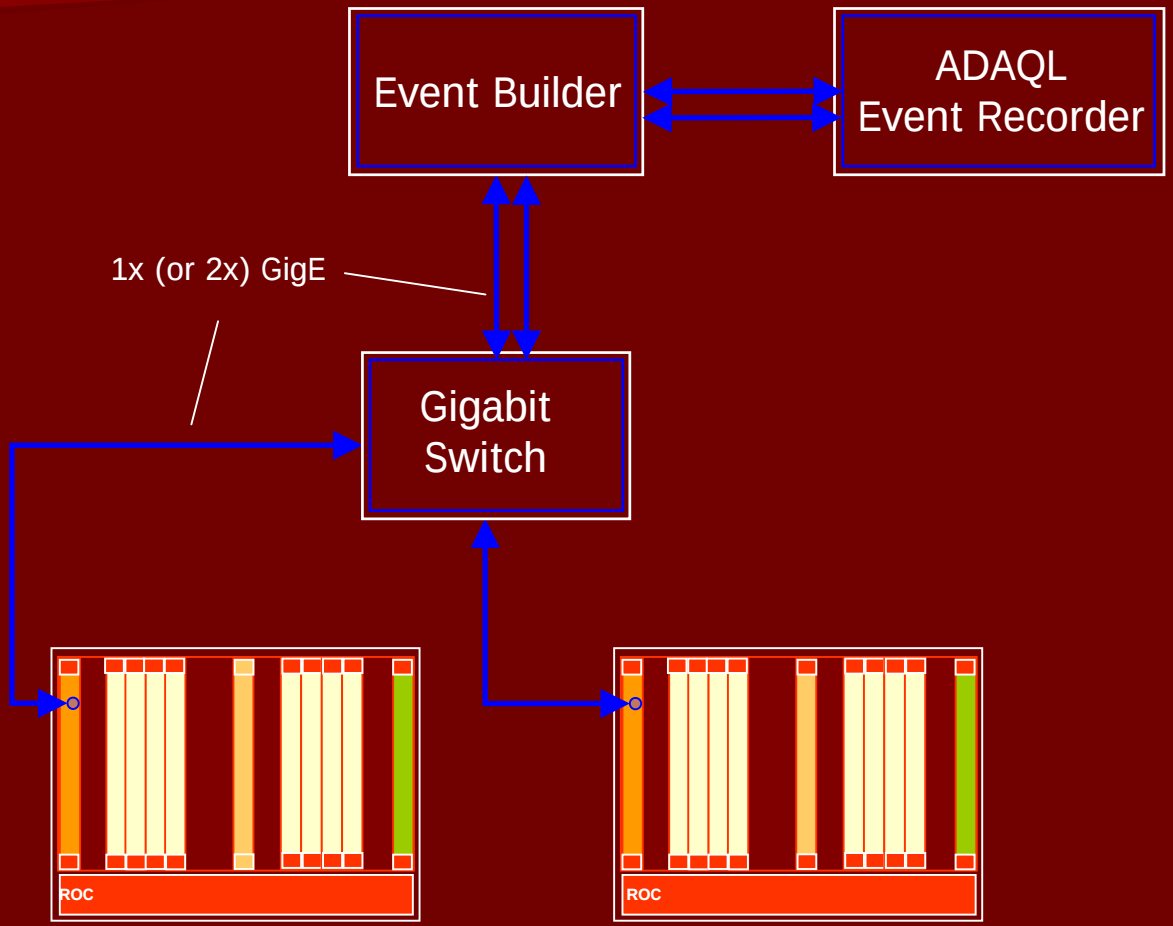
(slide from Dave Abbott)



Future Hall A Trigger



Hall A Data Path



Implications for SBS

- GEM ADC/MUX best implemented as custom VME board:
  - Most efficient integration into 12 GeV DAQ
  - Extensive design expertise available at JLab
- Key design elements:
  - VME64x (6U)
  - Support 2eSST high-speed synchronous readout mode via VME
  - Interface to JLab VXS bus (via P0) for trigger & clock signals
  - Forward trigger to APV25 front ends
  - Support on-board event “blocking” – perhaps 10-20 events deep
- Decide how advanced a system we want/need:
  - Trigger group may want to investigate on-crate trigger formation capability (CTP modules)
  - Investigate if trigger blocking beneficial (buffering of multiple triggers before crate readout)