Fastbus Update

R. Michaels, JLab

The design and R&D phases are completed.

Sergey Abrahamyan, Dasuni Adikaram, Alexandre Camsonne, Mark Jones, Mahlon Long,
Igor Rachek, Albert Shahinyan
DAQ group: Dave Abbott, William Gu, Bryan Moffit

Last 8 months (primarily me, with advice from DAQ group)

- **Finishing the hardware setup**
- **Unifying the Readout list : one list used by all crates**
- **Porting to Linux/Intel** (it had been done, I think, but not with new TI. Now done.)
- **Using Podd analyzer to analyze data**
- **Synchronization checks between Fastbus and VXS-HCAL crate.**

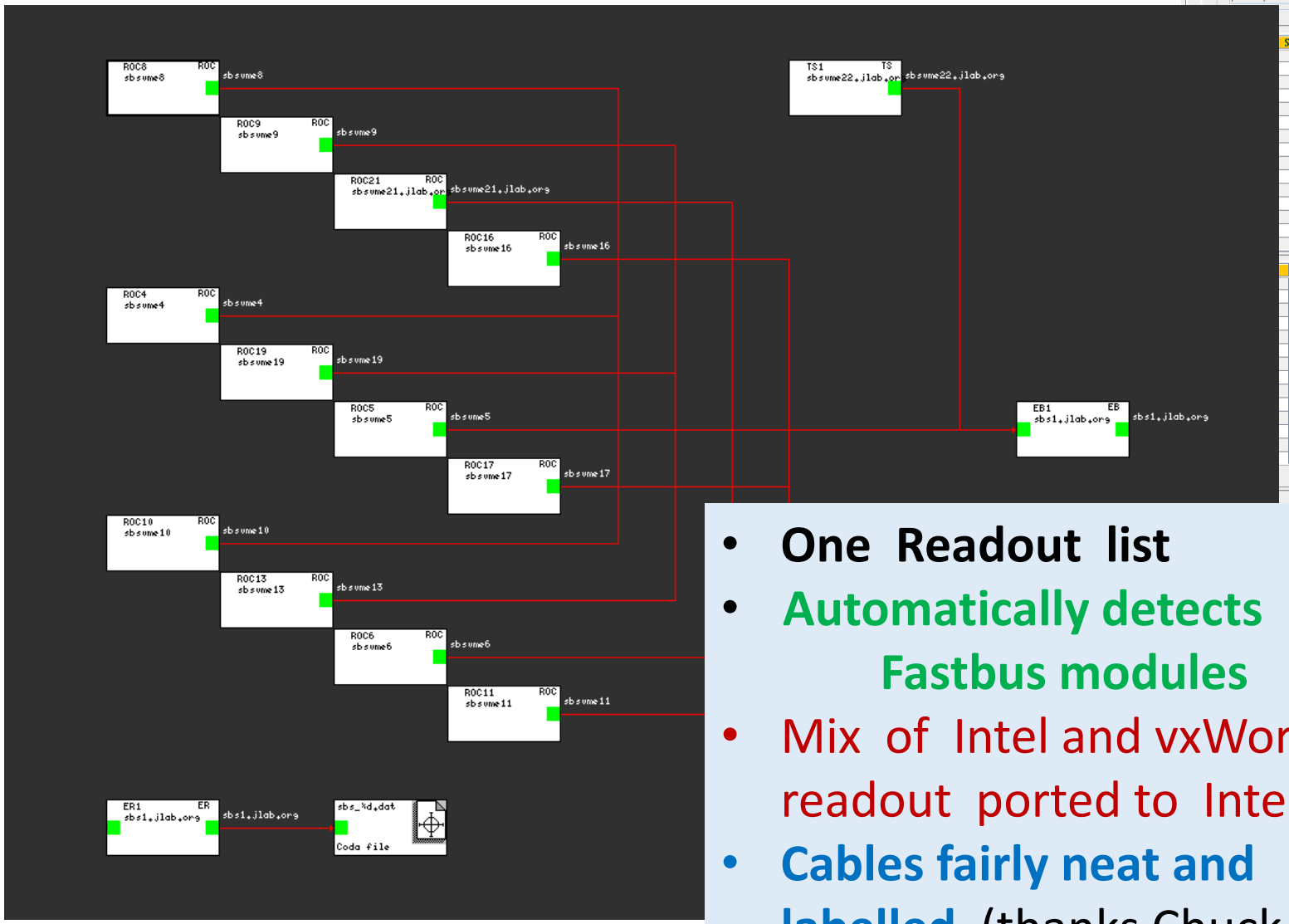
→ Yes, they are synched.

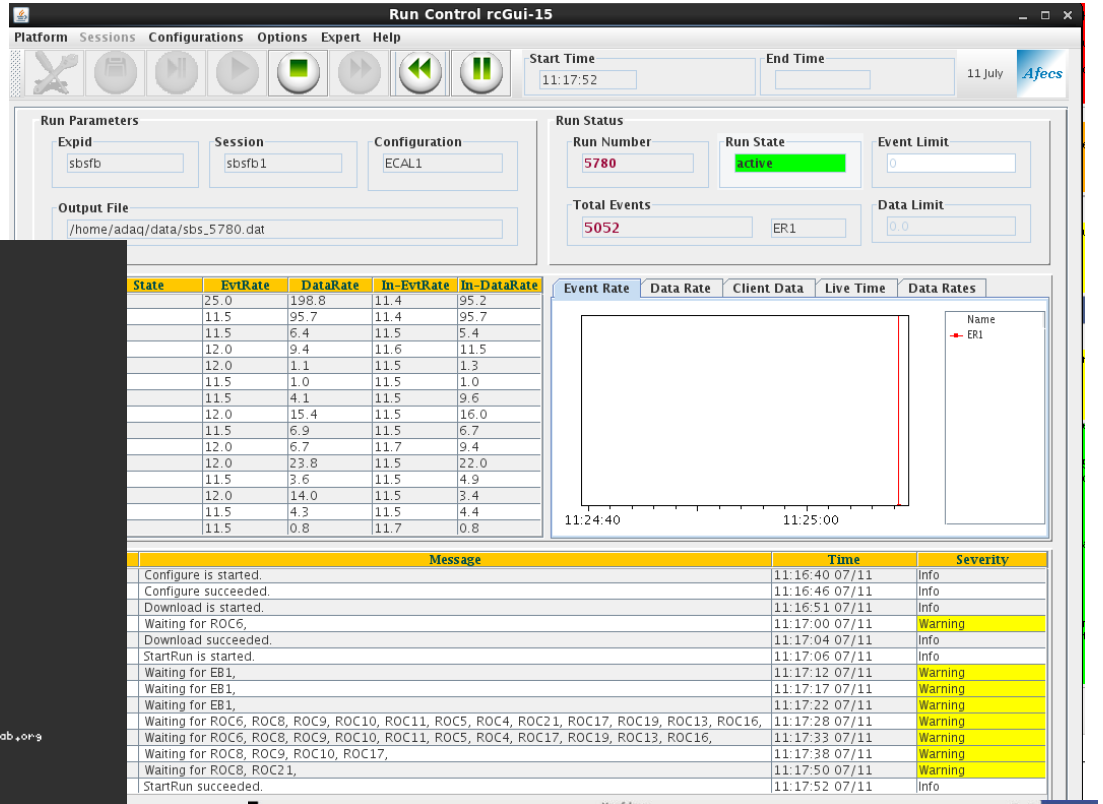
Design and R&D Phases -- summary

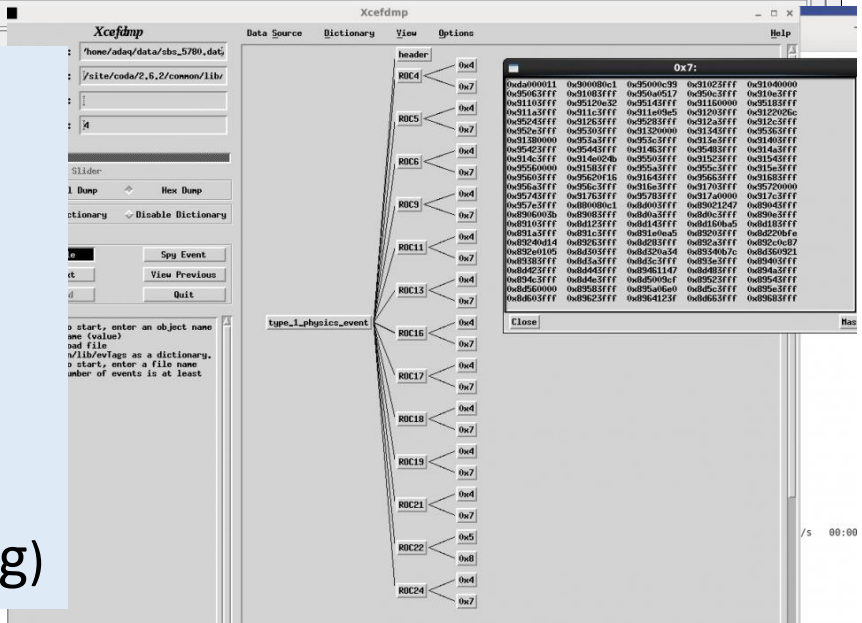
- See previous years' collab. mtg. talks for details
- **A sufficiently large collection of Fastbus parts was assembled and tested.**
- **Two DAQ weldments were set up (ECAL 12 crates, CDET 9 crates). There's also the Bigbite weldment with some Fastbus. However, not all crates online.**
- **Sparsification and event blocking demonstrated by Sergey Abrahamyan.**
- **Event switching demonstrated by Dasuni Adikaram and Mark Jones.**
- **A detailed mathematical model of the deadtime was developed, demonstrated to fit the data, and proven adequate for planned experiments. (Dasuni and Mark)**

ECAL DAQ Configuration

Recent work. All 12 Fastbus crates operational







- **One Readout list**
- **Automatically detects Fastbus modules**
- Mix of Intel and vxWorks, readout ported to Intel.
- **Cables fairly neat and labelled** (thanks Chuck Long)

R. Michaels, July 2017, SBS Mtg

Readout software on GitHub

(fastbus only)

https://github.com/rwmichaels/SBS_DAQ

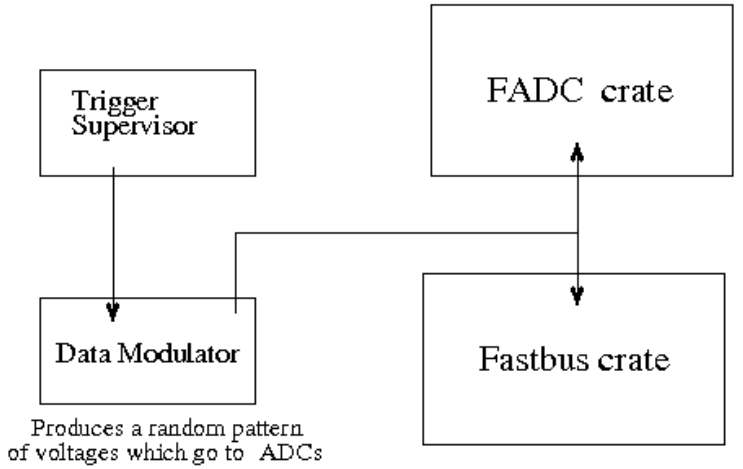
- Diagnostic libraries from Dave Abbott (ca 1996), vxWorks version, also ported to Linux/Intel
- Single readout list shared by all Fastbus crates. Also ported to Linux/Intel.

Synchronization Checks

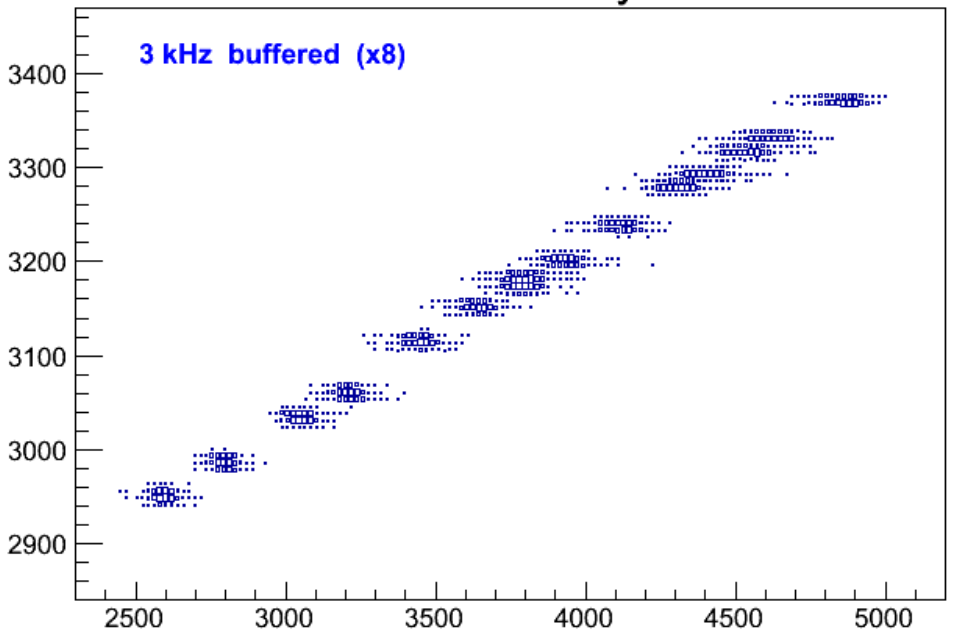
Triggers
(random)

Analog levels sent to ADCs

Synchronization Check Setup

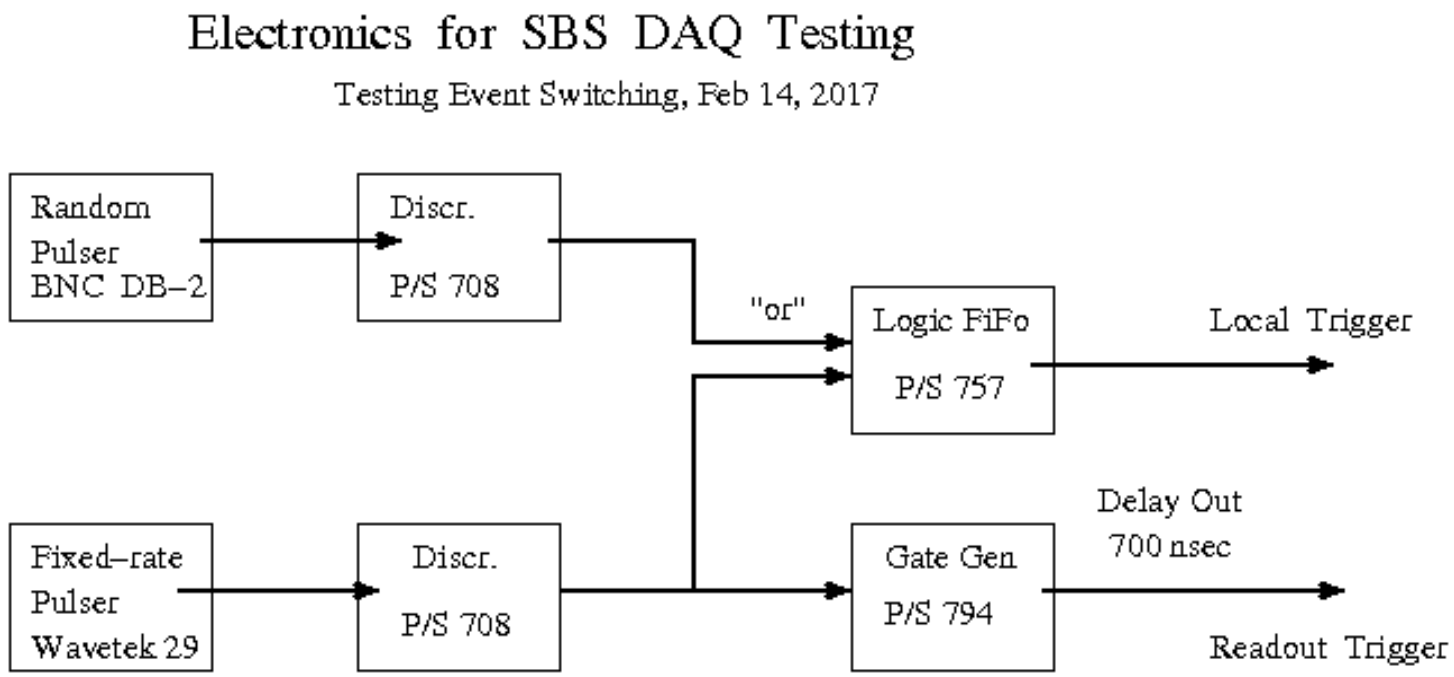


FADC 1 vs Fastbus synch check



My Checks of Event Switching

- DAQ runs at readout trigger rate independently of extra triggers. (good)
- Fast clear is 100% correlated with extra triggers. (good)
- Data were synched but at high rates 2% of FB crates were missing a gate. (not as good)



Data Analysis Plug-ins in Podd V1.6 SDK

```
class HadArmApparatus : public THaApparatus

        AddDetector( new HcalDetector("hcal", "Hcal Detector 1"));
```

```
class FbusTestApparatus : public THaApparatus

       AddDetector( new FbusDet1("fb1", "FbusTest Detector 1"));
```

```
{
  //  R. Michaels, Jan 2017
   //  Steering script for Hall A analyzer

   gSystem->Load("libSBS.so");

   THaApparatus* SBSFb = new FbusTestApparatus("S","SBS Fastbus Test Stand");
   gHaApps->Add( SBSFb );

   THaApparatus* HadArm = new HadArmApparatus("H","SBS Hadron Arm HCAL");
   gHaApps->Add( HadArm );
```

Problems and To-Do List

- **Fastbus Data for BLOCKLEVEL > 1 are not yet decoded. However, the events look ok "by eye". Need work on decoder. (Note, VME Pipelining modules are decoded properly.)**

- **MULTIBLOCK readout does not yet work on Intel/Linux. Instead, individual modules are addressed and read out. (However, it does work on vxWorks). This might be easy to fix, not sure.** *[Clarification: MULTIBLOCK is DMA transfer from a group of contiguous ADCs or TDCs, it's not the same as "BLOCKLEVEL > 1"].*

- **Continue to set up and test remaining Fastbus on CDET and Bigbite; define the configuration needed for first experiments. Ready in 6 months is possible if necessary.**