HCal Electronics
with First-level ECal trig

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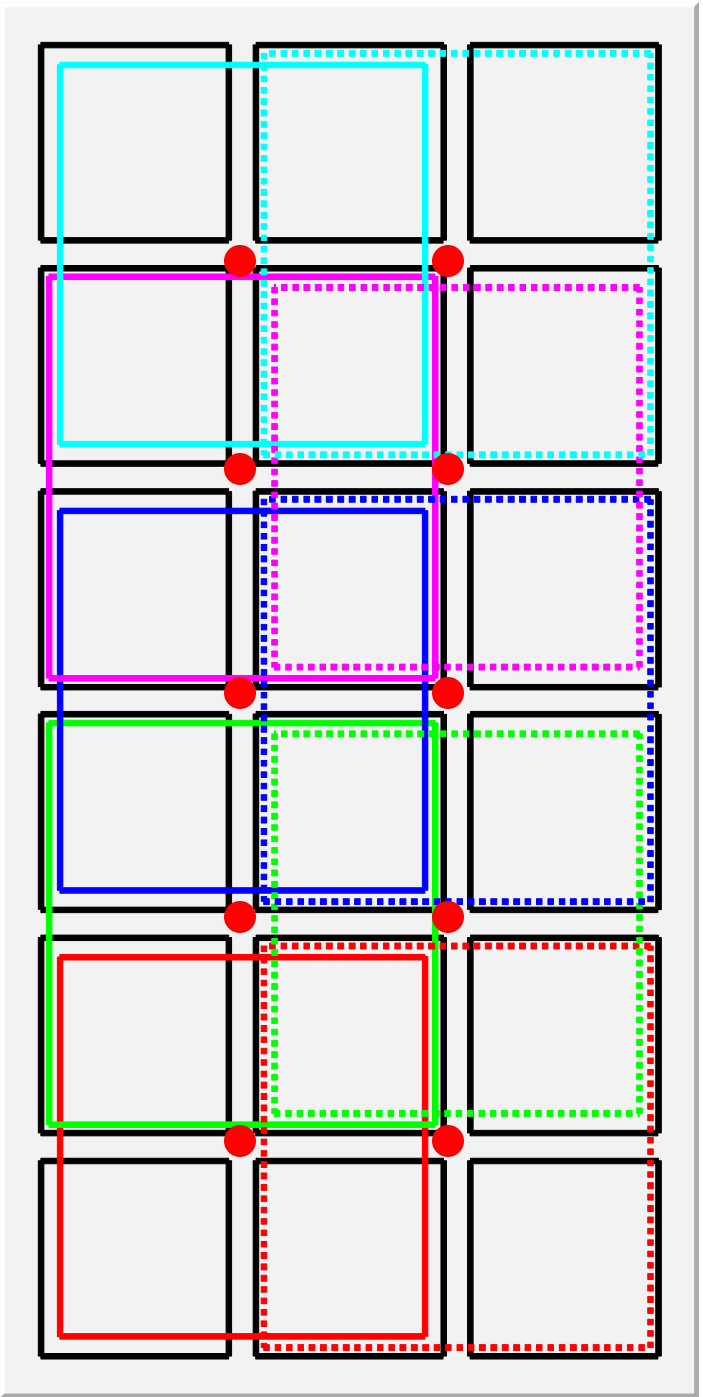
Jul. 22, 2016

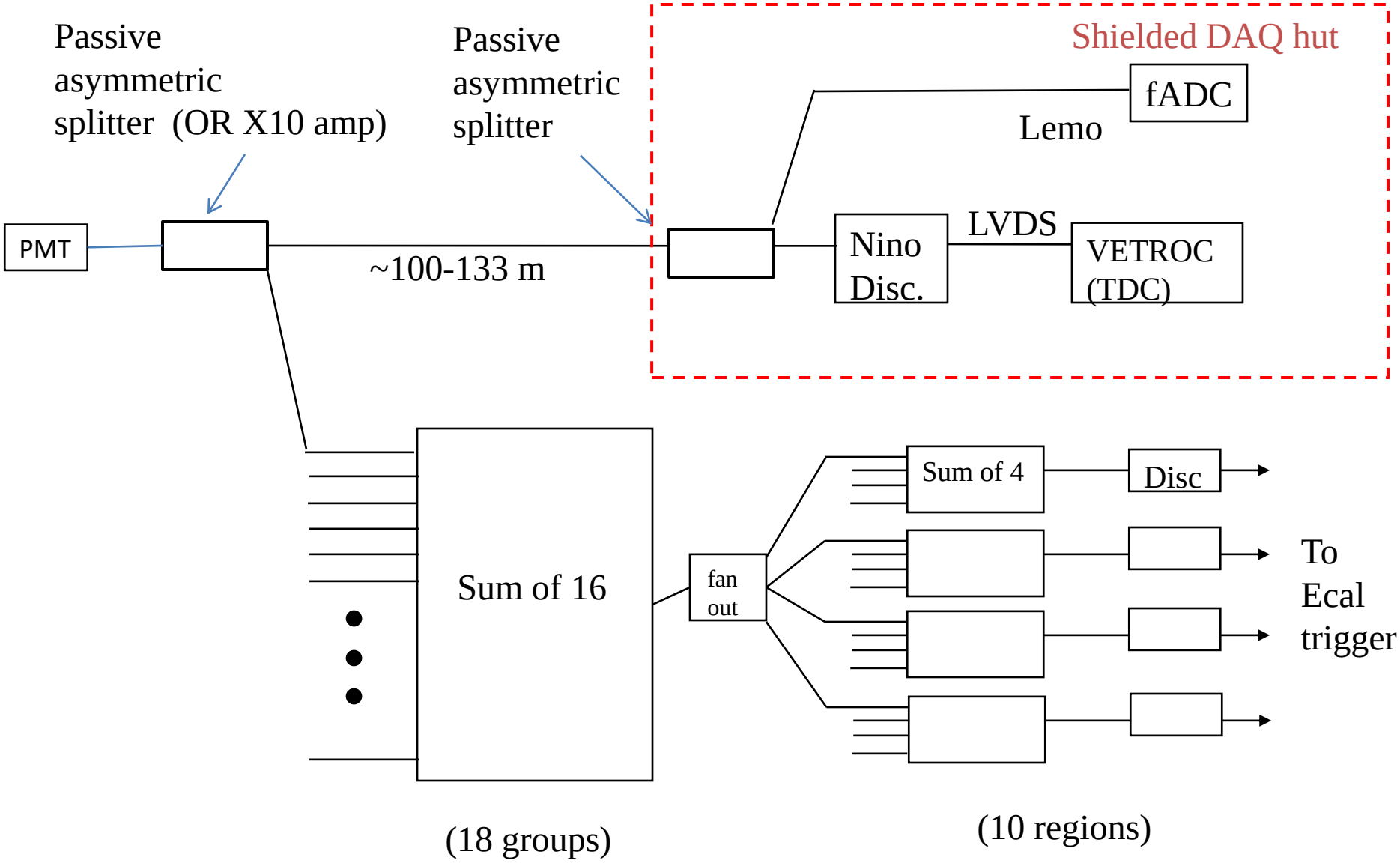


HCal is 12X24 array of modules.

Form overlapping regions by taking all possible 2X2 sets of (4X4 module) groups. Each group is a member of four regions (or less).

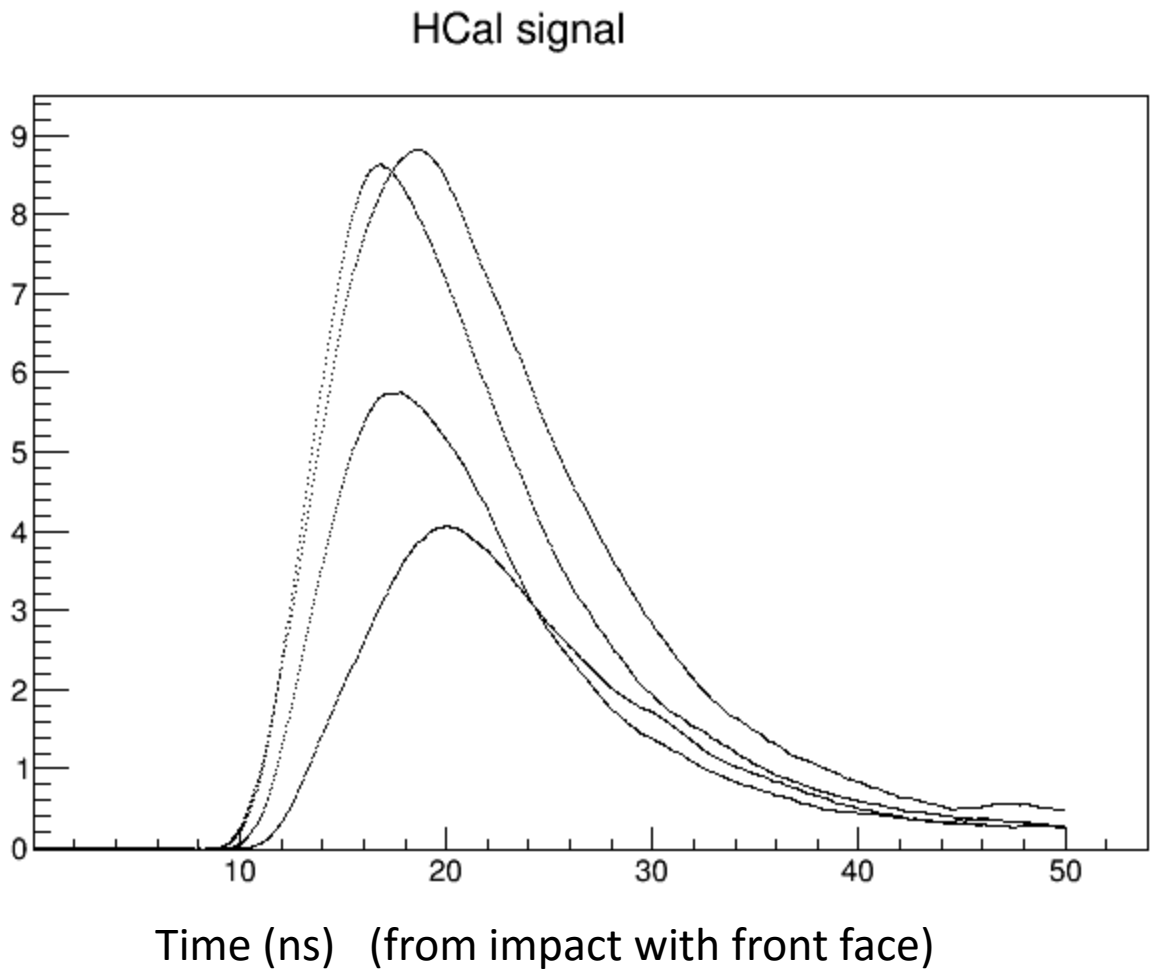
Total of 10 regions to be summed to give total energy in region. Each sum can be compared to threshold.

Ten logic signals to send to ECal to look for energy in region of HCal expected to correspond to ECal hit.


Passive
asymmetric
splitter (OR X10 amp)
Passive
asymmetric
splitter
Shielded DAQ hut
fADC
Lemo
PMT
~100-133 m
Nino
Disc.
LVDS
VETROC
(TDC)
Sum of 16
fan
out
Sum of 4
Disc
To
Ecal
trigger
(18 groups)
(10 regions)
18 UVa Summing mod.
36 in -> 18 in (16 used)
7 quad linear FI/FO (e.g. Phillips 740 2.5V)
3 quad L.E. Disc.

~325 p.e. for 2.6 GeV n
to
~1700 p.e. for 10.5 GeV n

325 p.e. X 10^7
= 520 pC = 26 nVs
~ 2 V signal



Cabling scheme for HCal

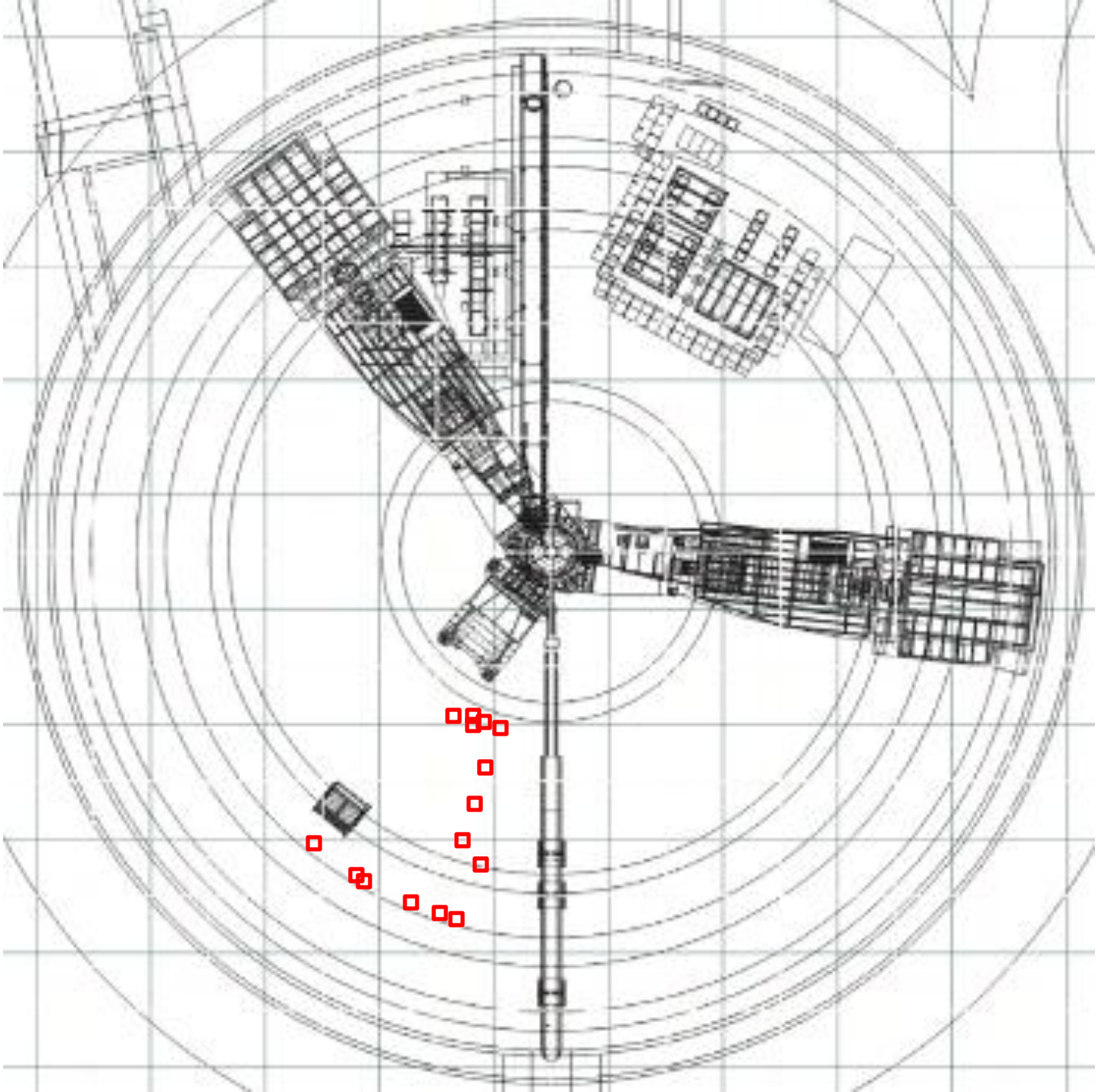
One signal, one HV cable to each tube. (Plus one HV & 3 signal/section for pulser)
Cables secured, strain-relieved on gantry behind HCal.
Cables held in place by gantry so they can be quickly re-connected to correct tubes.

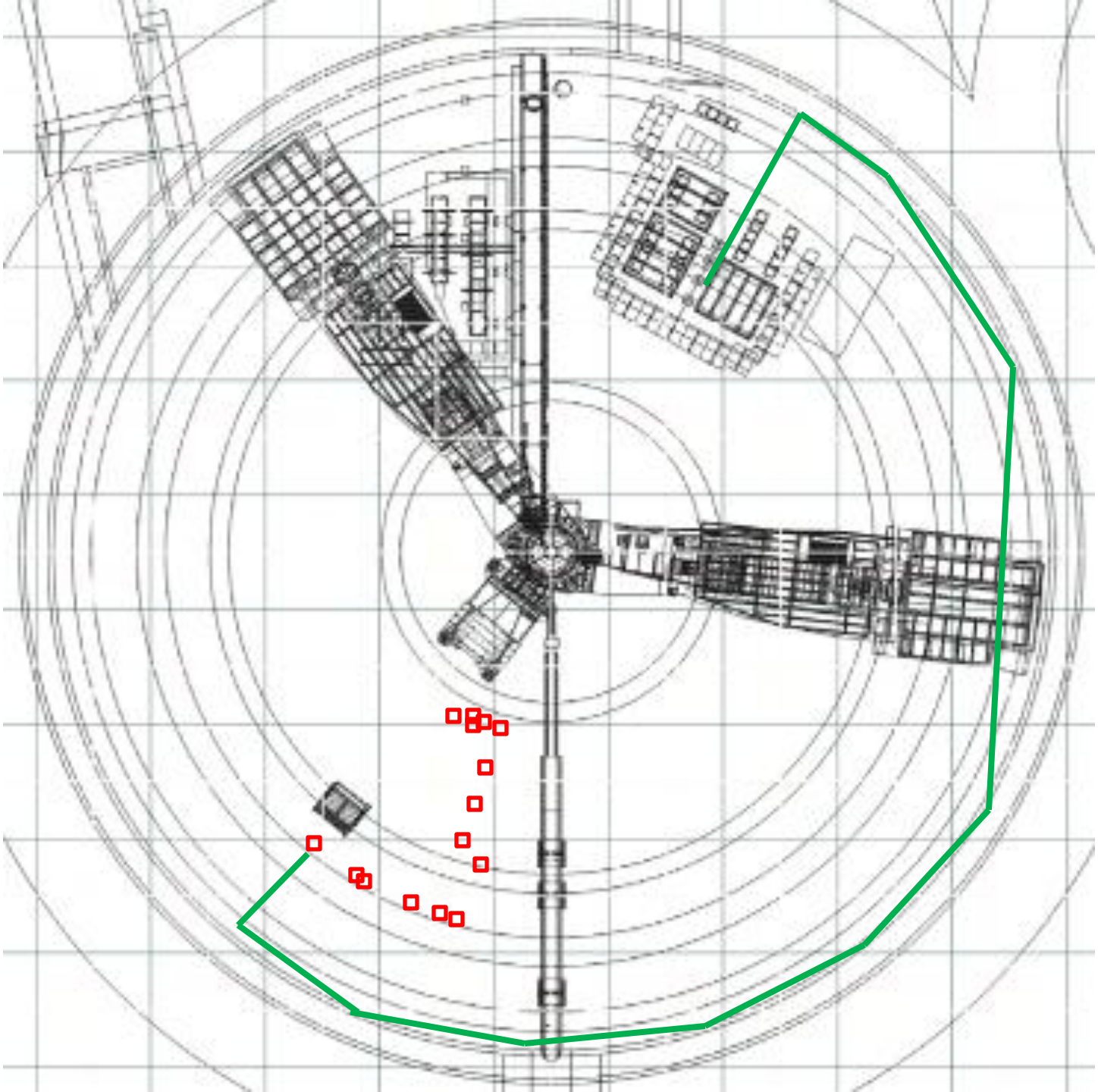
On HCal electronics/cabling platform

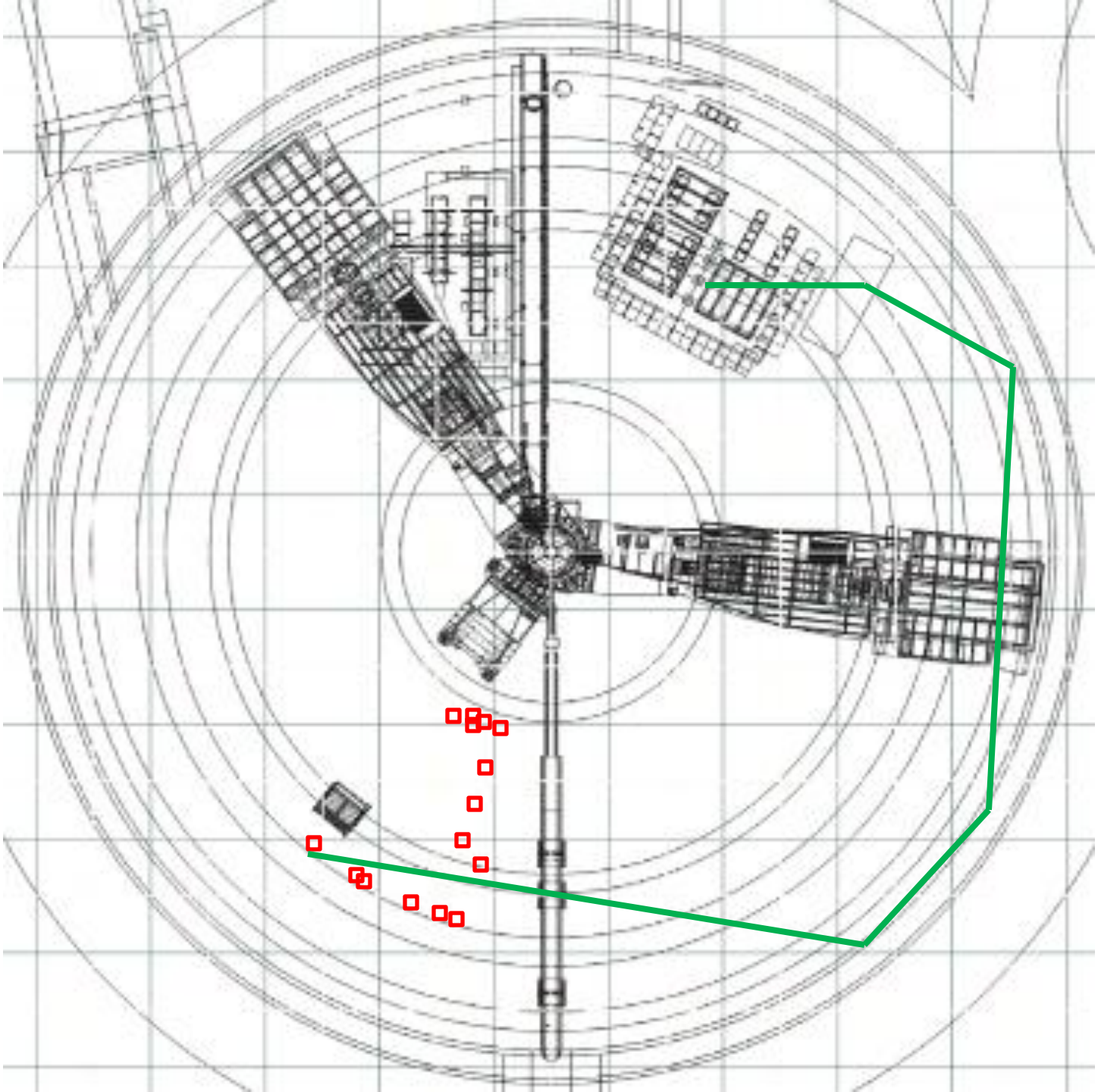
- Asymmetric? passive splitter (or X10 amp)
- Outputs to electronics hut (BNC ~100-133 m. long)
- Lemo cable outputs to UVa summing module (hardwired?? to patch panel)
  in same rack as patch panel

Second patch panel in electronics hut

- Asymmetric passive splitter (board with connection/housing/power for Nino)
- Signal cables run to one of eighteen 16-input BNC sub-panels (a-r)
- Sequential inputs go to sequential channels of Nino, fADC
- Nino outputs go to VETROC-based TDC







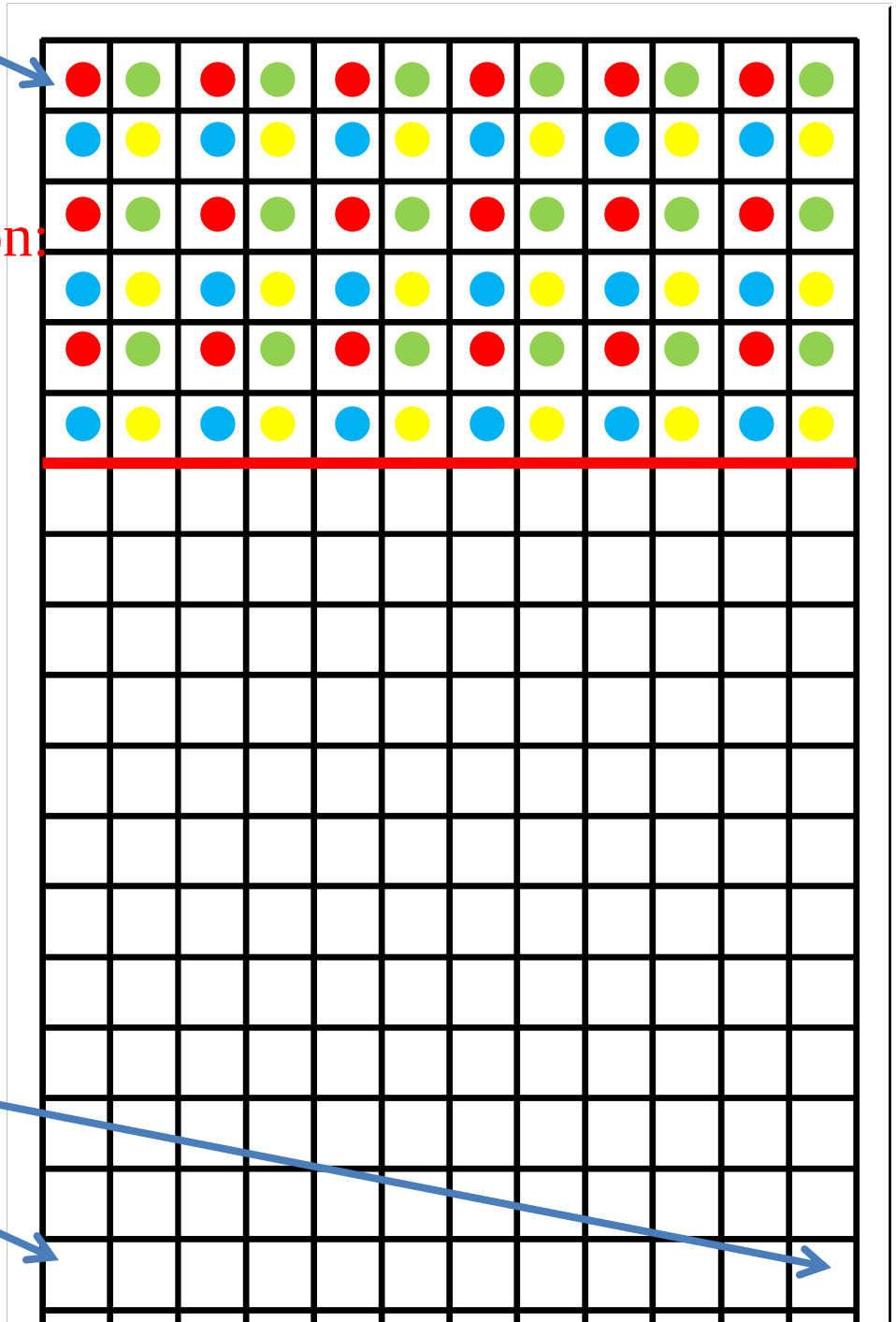
Suggested module-naming convention:

Row-Column
Rows numbered top down starting at 1.
Columns numbered left to right (***as viewed from back***) starting at 1.
Modules 1-1 through 24-12

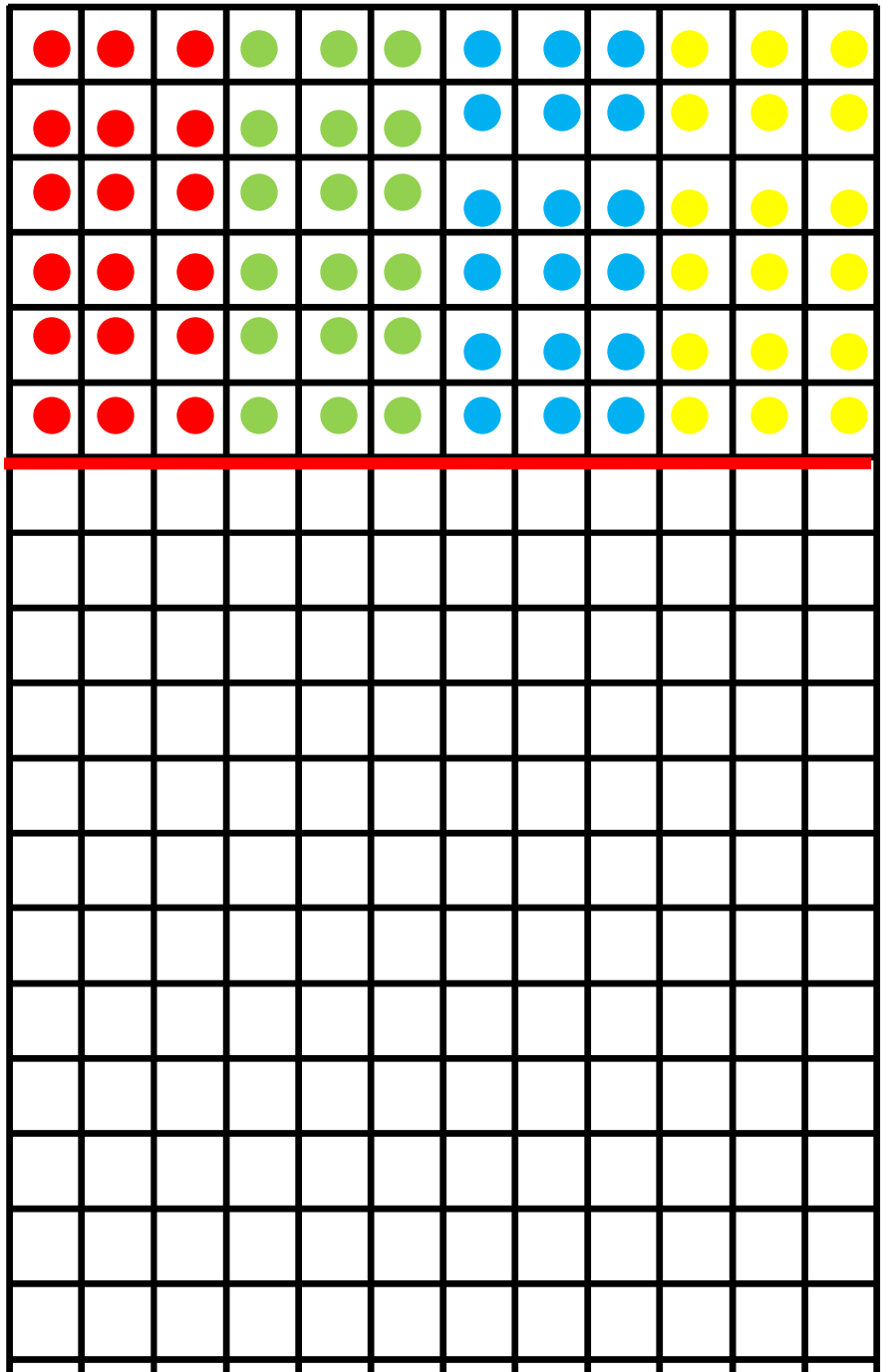
Original plan for LED pulsing:

Simultaneous pulse in all ●
then ● , ● and then ●

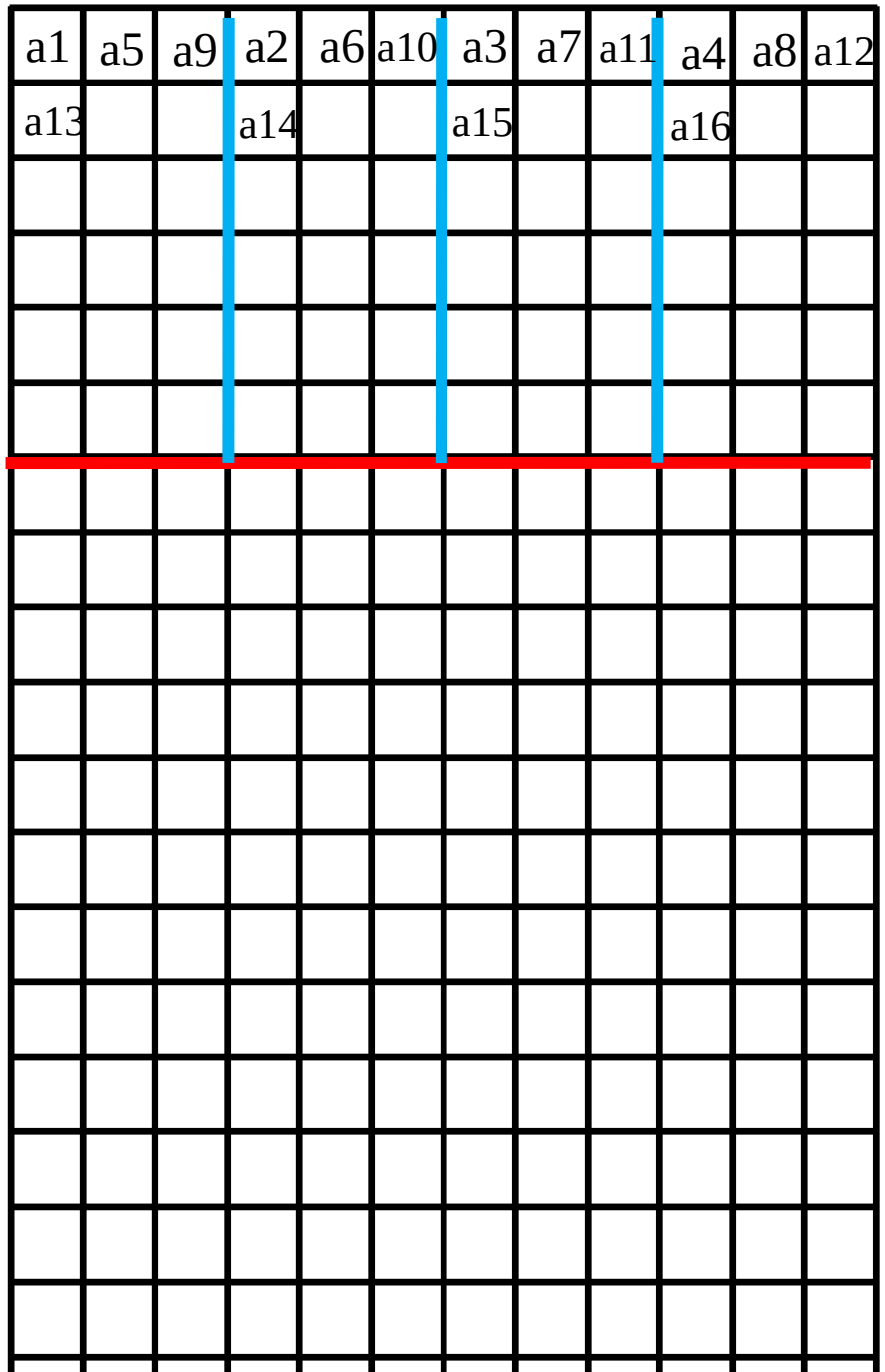
Avoids firing adjacent PMTs simultaneously



New plan for LED pulsing.
Don’t worry about firing adjacent PMTs simultaneously but avoid having adjacent electronics channels for same LED pulse.



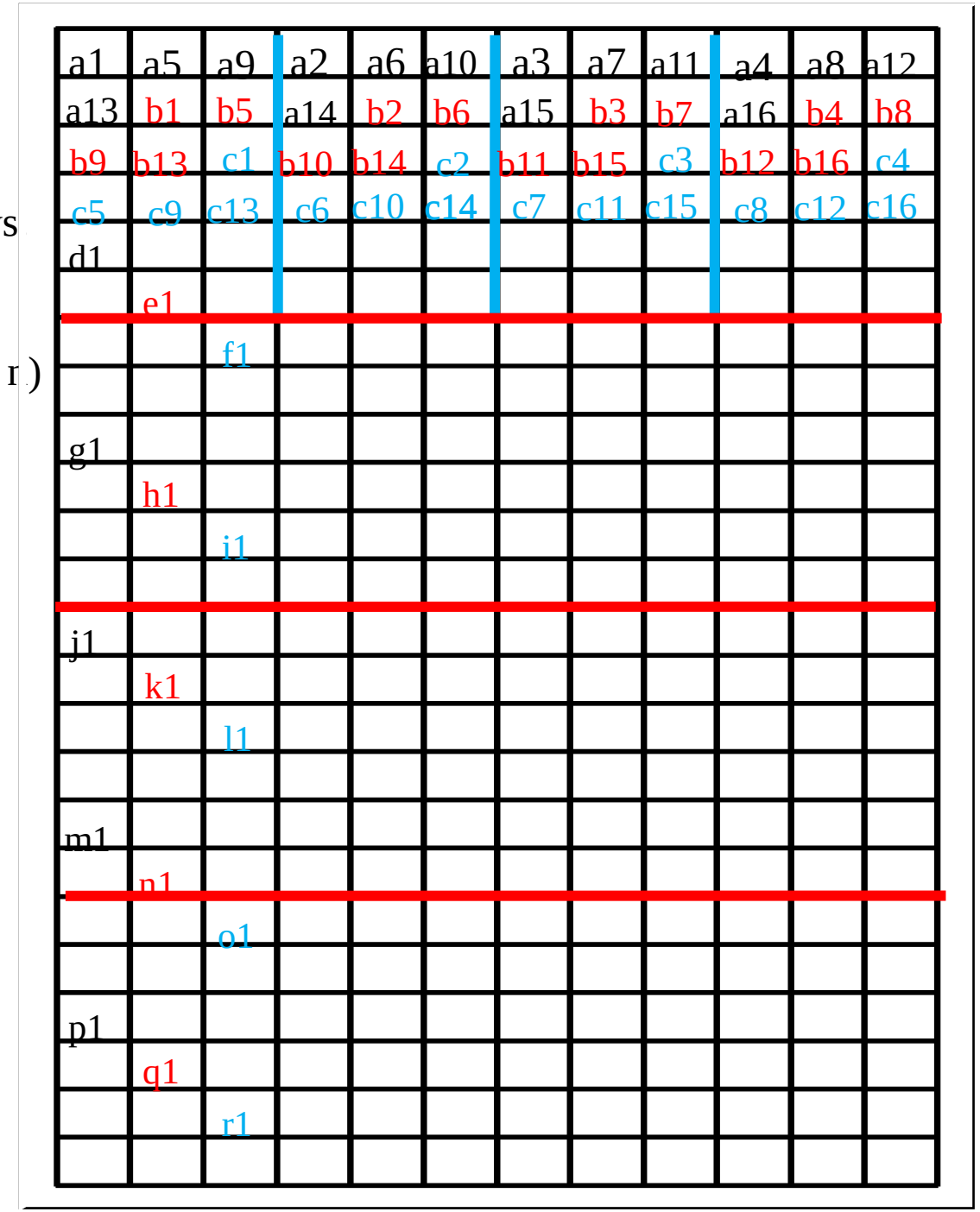
Simpler cabling pattern.
Adjacent electronics channels don’t fire on same LED pulse and unlikely to fire in same cluster.
Module problems show up as many bad modules in two rows, easier to spot.
Somewhat easier to track down single-module problems.



Simpler cabling pattern.

Three patch panels for each four rows

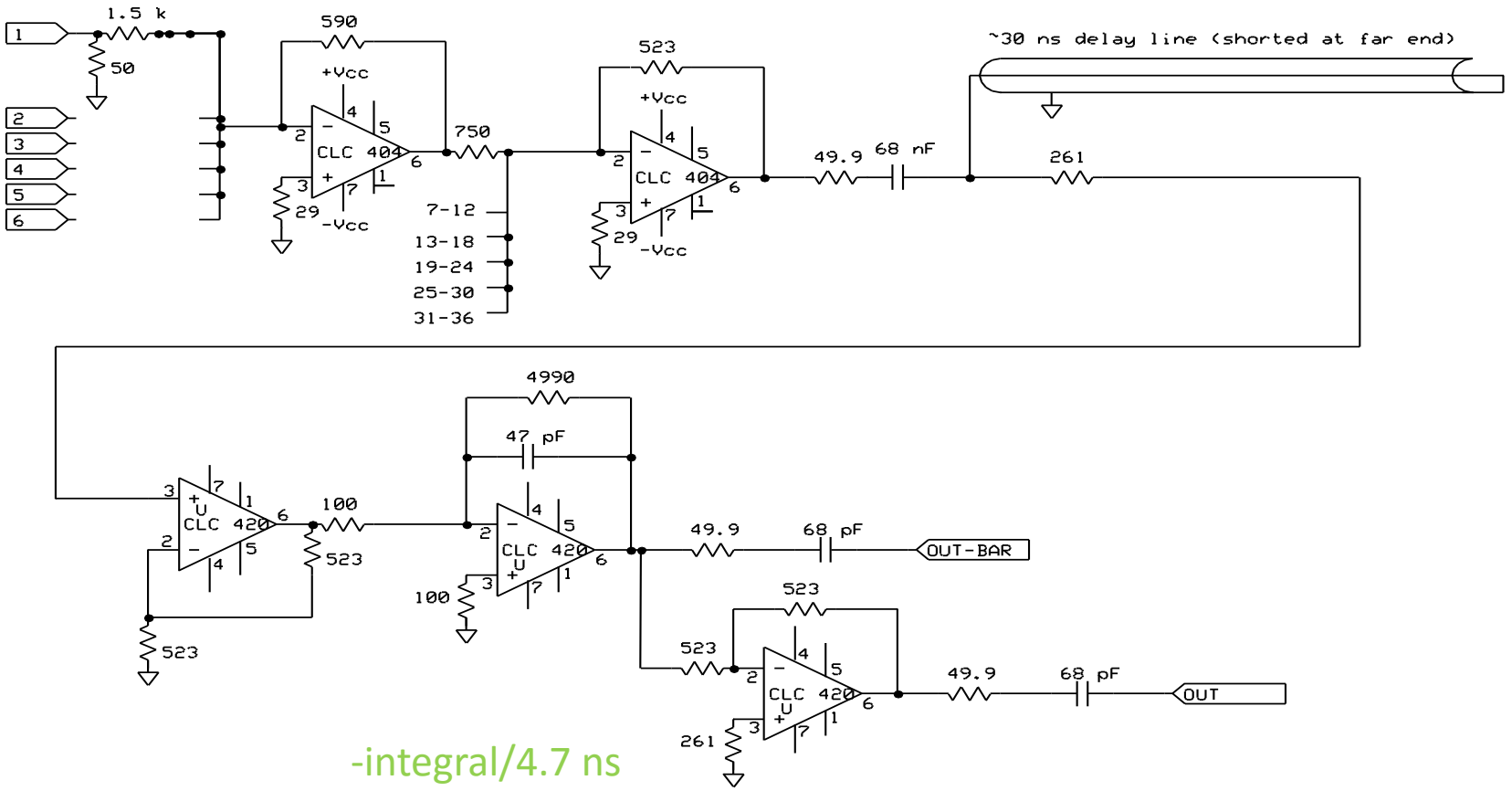
Only one patch panel straddles each
of two sub-module divisions (e and r)



18 (at least?) U.Va. 36-fold summing modules available from CLAS

Sum X -0.393

Sum X -0.697



-integral/4.7 ns

X 2

-decay time=
-230 ns

X -1


File
Edit
Vertical
Horiz/Acq
Trig
Display
Cursors
Measure
Mask
Math
MyScope
Analyze
Utilities
Help
Tek
a
b
1
C1 500mV/div 50Ω BW:1.0G
C3 50.0mV/div 50Ω BW:1.0G
t1 11.5ns
t2 50.2ns
Δt 38.7ns
1/Δt 25.84MHz
A Pat LXLX AND
10.0ns/div 10.0GS/s IT 50.0ps/pt
Run Sample
724 acqs RL:2.0k
Auto March 08, 2016 20:27:53
Value Mean Min Max St Dev Count Info
C1 Area* -1.076nVs -1.0289254n -1.203n -866.5p 55.03p 725.0
C3 Area -13.08nVs -13.114279n -13.18n -13.05n 19.38p 725.0
Cursor Controls
Source
Cursor 1
Cursor 2
Cursor Type
H Bars
V Bars
Waveform
Screen
Move Cursors to Center
Setup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Help
Tek
a
b
1
C1 500mV/div 50Ω BW:1.0G
C3 50.0mV/div 50Ω BW:1.0G
t1 260ns
t2 647ns
Δt 387ns
1/Δt 2.584MHz
A Pat LXLX AND
100ns/div 10.0GS/s IT 50.0
Run Sample
246 acqs RL:20
Auto March 08, 2016
Value Mean Min Max St Dev Count Info
C1 Area* -10.78nVs -10.830973n -11.62n -10.07n 316.7p 245.0
C3 Area 9.078nVs 9.1152693n 8.822n 9.362n 112.7p 245.0
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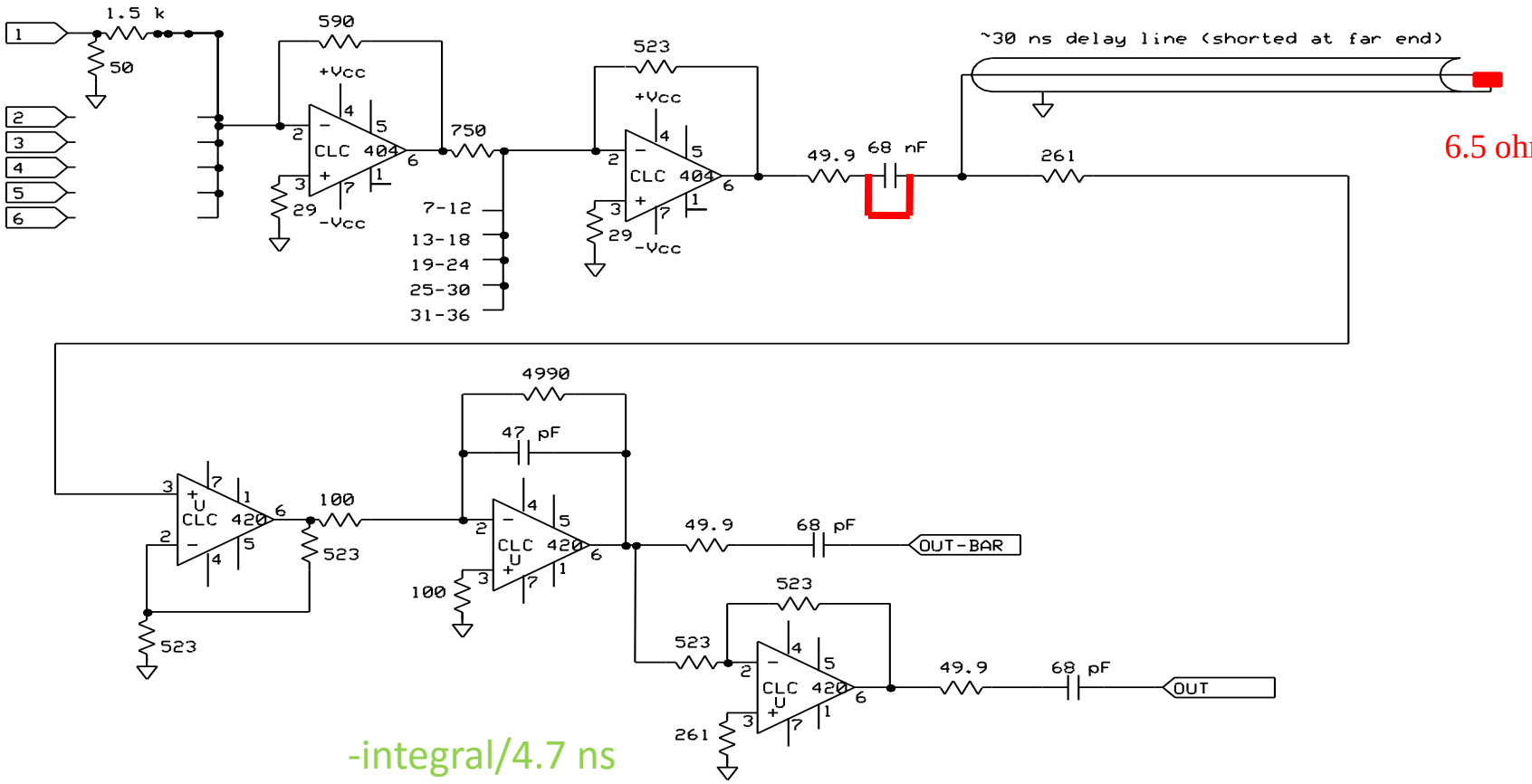
Sum X -0.393

Sum X -0.697



-integral/4.7 ns

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-decay time=
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File
Edit
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Help
Tek
C1 80.0mV/div 50Ω BW:1.0G
C3 200mV/div 50Ω BW:1.0G
t1 594ns
t2 -22.0ns
Δt -616ns
1/Δt 1.623MHz
A' C3 -488mV
100ns/div 1.0GS/s 1.0ns/pt
Run Average:16
365 acqs RL:1.0k
Auto March 26, 2016 22:20:36
Value Mean Min Max St Dev Count Info
C1 Area* -39.16nVs -39.177836n -39.37n -39.01n 78.11p 46.0
C3 Area -36.15nVs -36.096814n -36.2n -35.98n 56.73p 46.0
Cursor Controls
Source
Cursor 1
Ch 1
Cursor 2
Ch 1
Cursor Type
H Bars
V Bars
Waveform
Screen
Move Cursors to Center
Setup


File
Edit
Vertical
Horiz/Acq
Trig
Display
Cursors
Measure
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Math
MyScope
Analyze
Utilities
Help
Tek
C1 80.0mV/div 50Ω BW:1.0G
C3 200mV/div 50Ω BW:1.0G
t1 -400ns
t2 14.4µs
Δt 14.8µs
1/Δt 67.568kHz
A' C3 -488mV
2.0µs/div 500MS/s 2.0ns/pt
Run Average:16
737 acqs RL:10.0k
Auto March 26, 2016 22:28:54
Value Mean Min Max St Dev Count Info
C1 Area* 8.888nVs 9.1461536n 7.169n 10.94n 798.5p 95.0
C3 Area -649.5nVs -648.74048n -651.3n -646.2n 1.189n 95.0
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Cursor 1
Ch 1
Cursor 2
Ch 1
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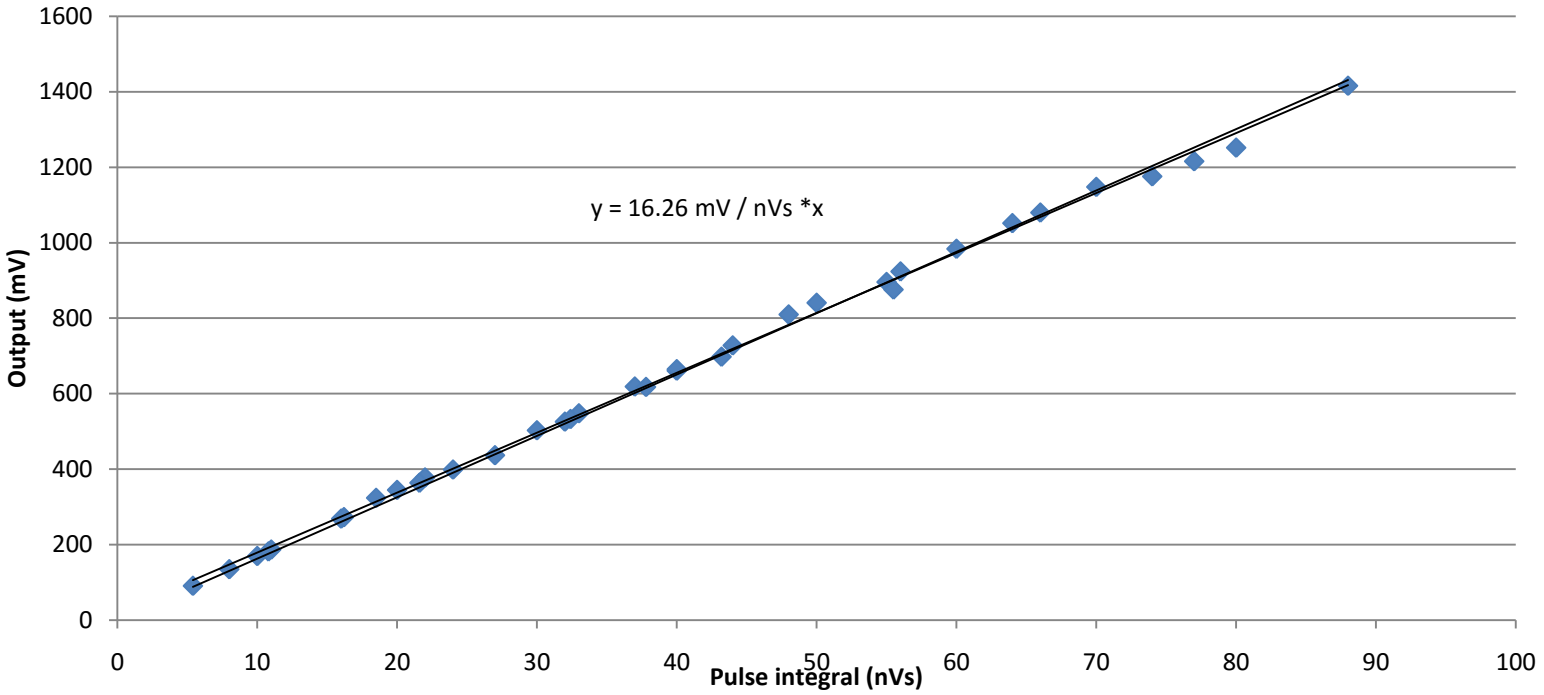


Choose PMT gain so expected signal sums to ~60 nVs giving ~1V output. Discriminate at eg. ~0.25 V.

For all experiments:

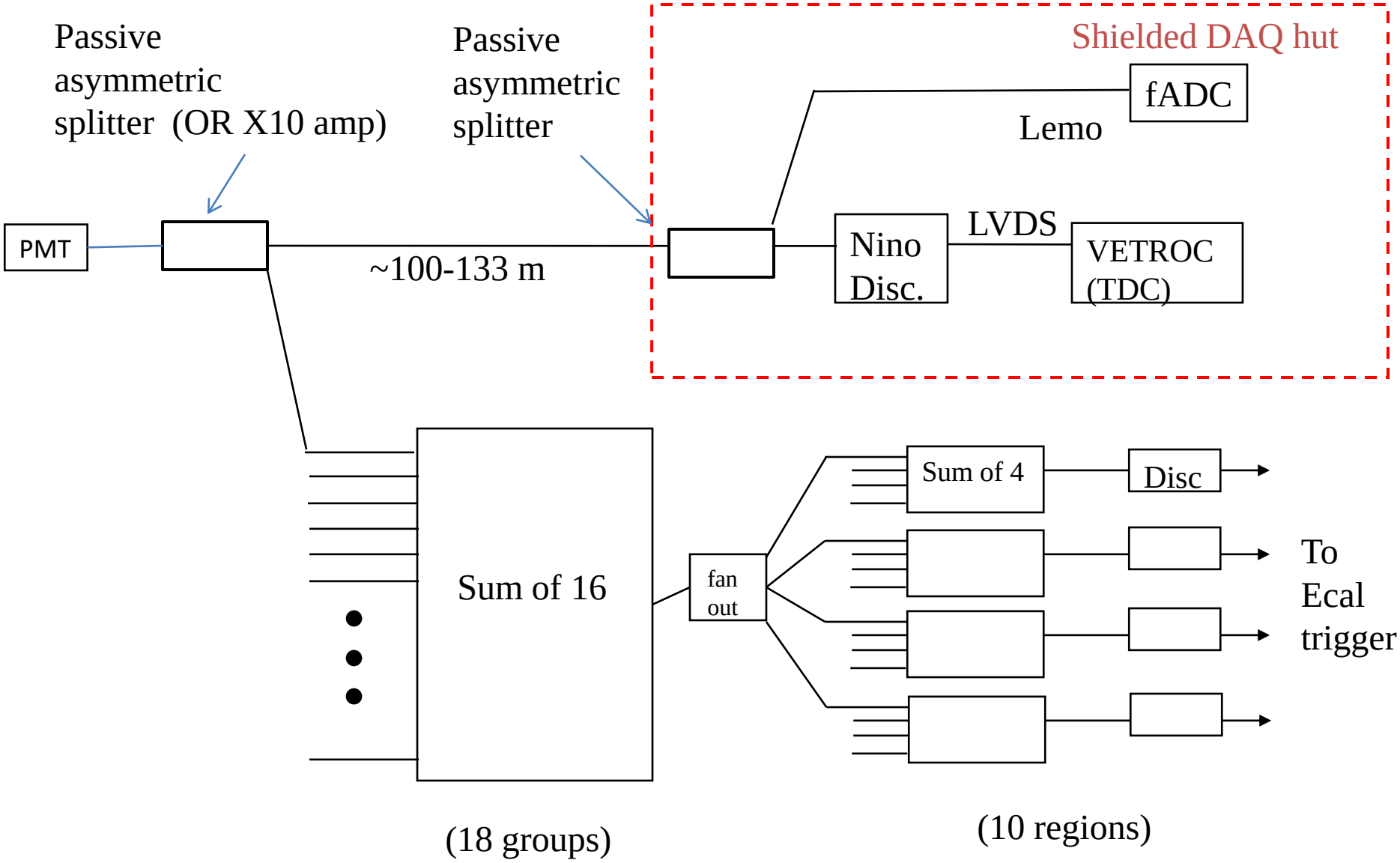
288 ~5m BNC (or BNC/lemo) cables
24 12-chan amps &2 NIM bins
288 lemo/BNC jumper cables
288 chan BNC-BNC patch panel
** 288 long BNC low loss cables **
3 long cables +1 SHV for pulser
Asymmetric splitter panel in Electronics hut
with connection/housing for Nino cards
18 Nino cards (with pin connectors)
18 sixteen channel LVDS cables
18 VETROCs (or F1 ?)
288 lemo cables
18 fADCs
2VXI crates (+1?)
2? ROCs & TIs

288 chan HV (2 1458 crates
24 1461N)
12 24-conductor HV cables
24 24-chan. SHV boxes
288 1.5 m SHV
288 5 m SHV

} Acquisition in progress

For GEp:

288 channels patch-panel/splitter custom
(not needed with amps)
288 lemo cables
18 UVa Summing modules (modified)
7 quad linear FI/FO (e.g. Phillips 740 2.5V)
3 quad L.E. Disc.
3 NIM crates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Sum of 16
fan
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Sum of 4
Disc
To
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trigger
(18 groups)
(10 regions)
18 UVa Summing mod.
36 in -> 18 in (16 used)
7 quad linear FI/FO (e.g. Phillips 740 2.5V)
3 quad L.E. Disc.

To do:

Understand expected PMT current
Make final decision on amp/splitter (by end of summer)

Make final decision on Nino card (borrow and test one)

Layout racks for gantry and electronics hut

Choose cable route in hall, set all cable lengths/types.