ECAL FASTBUS

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SBS Collaboration Meeting
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Experiment Overview

GEp Detectors	Channels	Readout	Type
SBS Proton arm			
Front tracker (6 GEM chambers)	41,472	APV25 MPD	VME
Rear tracker (10 GEM chambers)	61,440	APV25 MPD	VME
HCAL	288	FADC 250	VME
Electron arm			
ECAL	1776	ADCs 1881M	Fastbus
ECAL sums	214	TDCs 1877S	Fastbus
CDET	2688	TDCs 1877S	Fastbus

GEn/GMn Detectors	Channels	Readout	Type
SBS Proton arm			
HCAL	288	FADC 250	VME
CDet	2688	TDCs 1877S	Fastbus
BigBite Electron arm			
PreShower/Shower	243	ADCs 1881M	Fastbus
Scintillator	180	ADCs 1877S	Fastbus
Gas Cerenkov	550	ADCs 1877S	Fastbus
Front Tracker (4 GEM chambers)	27648	APV25 MPD	VME
Rear Tracker (1 GEM chamber)	6144	APV25 MPD	VME

SBS FASTBUS inventory as of May 2016

Item	We need	We have	Comments
Fastbus Crate	21	21	12 (ECal) + 9 (CDet)
VXS crate	1	1	For ECal
CPU	22	20	MVME 24XX(9)+ GE XVR (2) + GE XVB 602(9) + MVME 23XX (5)?
TI	21	23	2 (at GEM)
SFI	21	21	2 (at BigBite)
TS	1	1	
SD	1	1	
TD	3	4	
ATC	21	> 21	
GAC	21	> 21	
Signal Dist. Card	21	36	
ADC 1881M	93	84	loaned few modules to PRAD
TDC 1877S	84	> 84	

* Optical cables/twisted pair wires/network cables

FASTBUS Dead time

- GEp experiment will trigger on coincidence. Coincidence rate will be 5kHz.
  Singles rates: ECAL ~200kHz, HCAL ~2 MHz
  - Estimated dead time ~40%. => Need to reduce.
  - Forming the HCAL trigger takes 1 ms. Too long to delay the ECAL ADC signals. => Will have use ECAL trigger as a LEVEL 1 gate and fast clear if no LEVEL 2 coincidence.

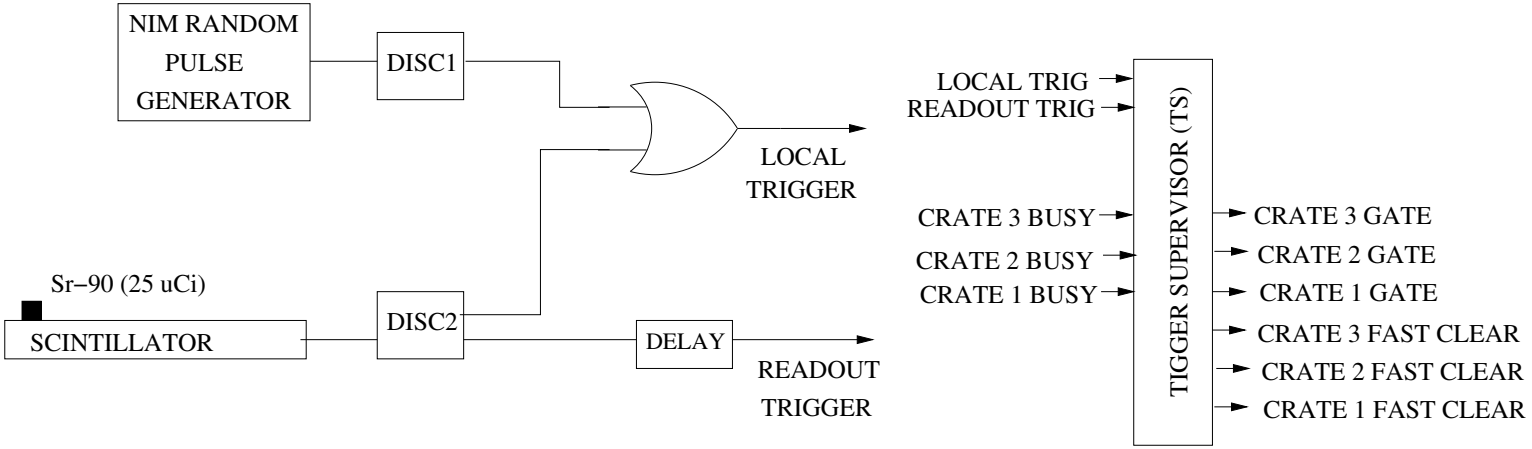
- To reduce the time, we can use
  1. Sparsification
     Zero suppression on channels without a signal
  2. Event blocking
     Buffers the dead time and reduces over head

  Already tested By Sergey et al.

  3. Event Switching
     Switching trigger between multiple (3) FB crates

Dead time studies are completed. Tests are in progress along with other VME systems.

Event Switching - Test Setup

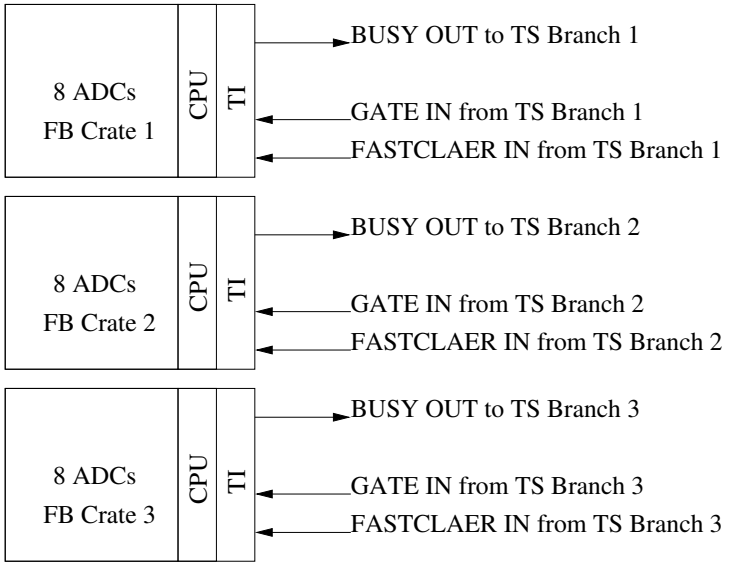


Readout trigger ~500 Hz - 10 kHz

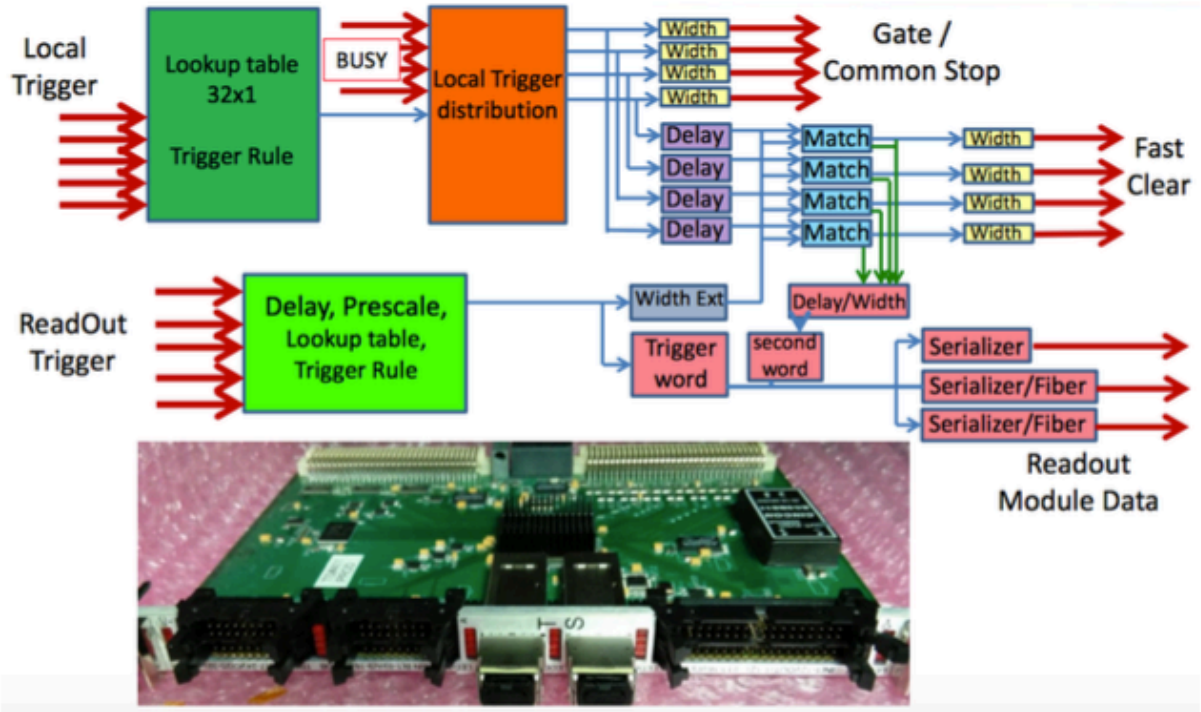
Local trigger ~10kHz - 200 kHz

The trigger signals from TS pass (through SD and TD) to the TIs in FB crates via optical transceivers.

The busy signals from front end can propagate back to the TS.

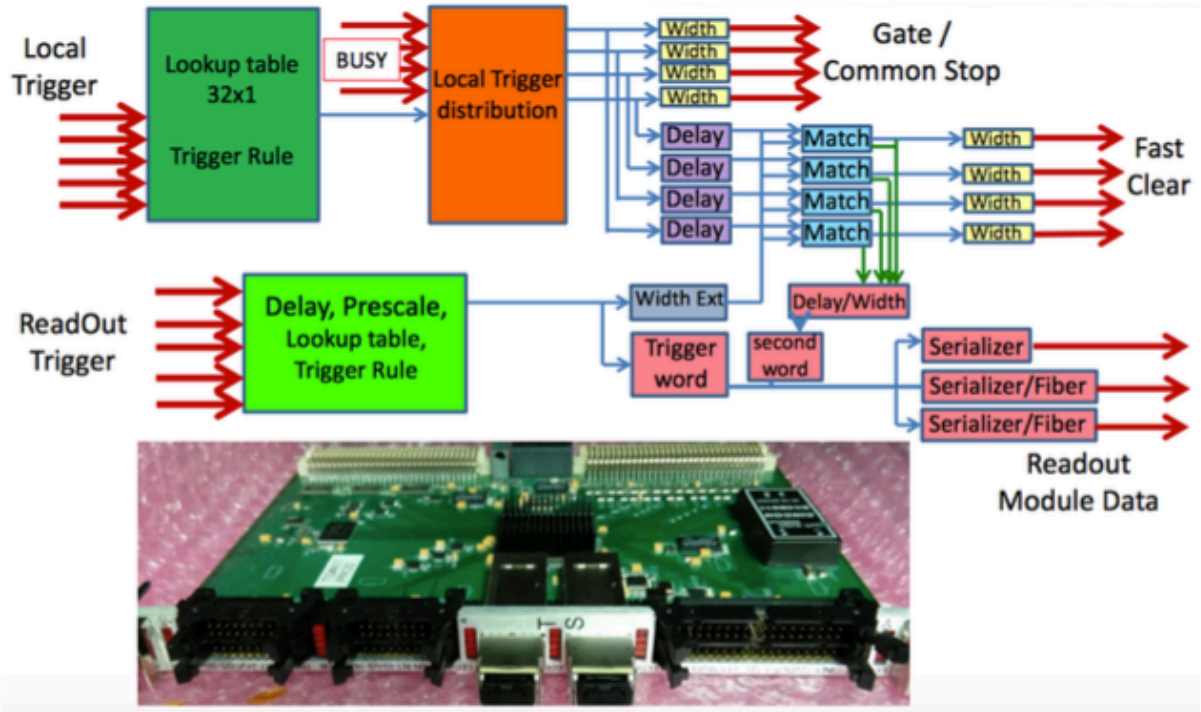


SBS Trigger Supervisor



- We can use up to five local trigger inputs to generates the local trigger. The simple rule is that there is no more than ONE local trigger in time *T*. *T* was set to 128 ns during the test.
- The Local Trigger can be distributed to (up to) four duplication branches, each links to one FB crate.

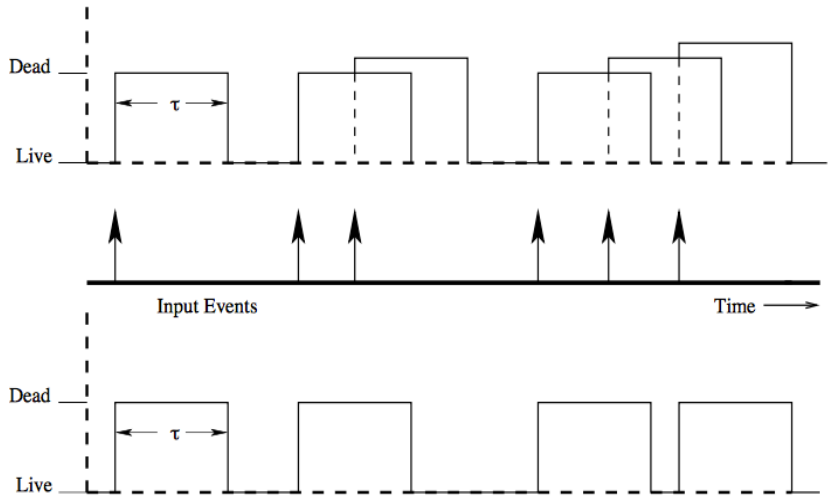
SBS Trigger Supervisor



- Once TS receives a Local trigger, it sends a ADC gate signal to the next non-BUSY crate.
- Local trigger can be delayed up to ~2 μs in FPGA to match with readout trigger to generate ”*Fast Clear*” or ”*Not Fast Clear*” signal. The Fast Clear signal is delayed Local trigger vetoed by the Readout trigger.
- The readout trigger is common for all branches.

Dead time model

Dead times are typically modeled as being of two varieties:



Extendable

Non-extendable

f = average random rate
μ = fτ

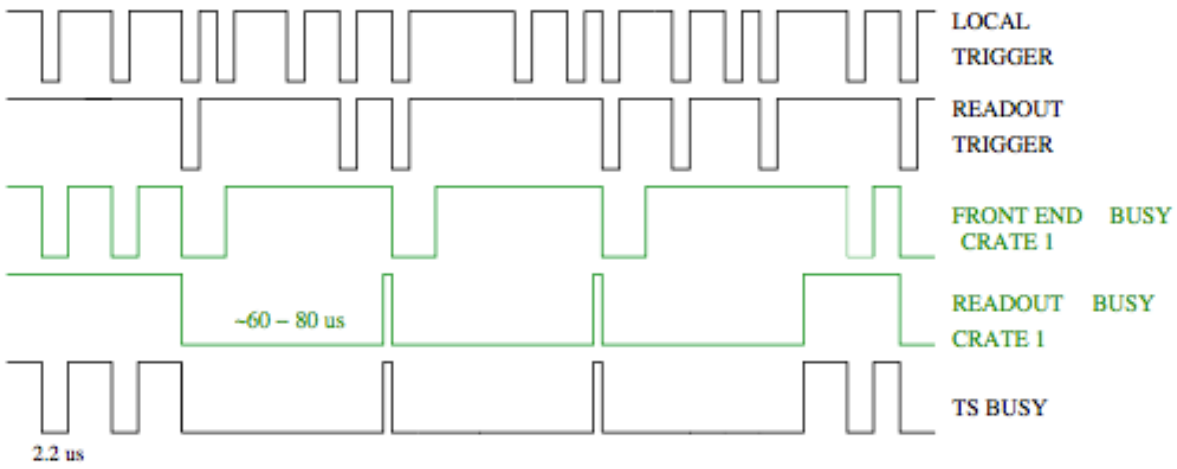
- **Non-extendable** - An event happening during the dead time is simply lost.

$$DT = \frac{f\tau}{f\tau + 1}$$

- **Extendable** - An event happening during the dead time will not just be missed, but will restart the dead time.

$$DT = \sum_{n=1}^{\infty} \frac{\mu^n e^{-\mu}}{n\,!}$$

Non-buffered mode – Single Crate



Dead time is caused by 2 ways.

- **Readout busy (dt_R)**: If the event is accepted, DAQ system is dead for some period to read that event out. No other events will be accepted during that time.

- **Fast Clear (dt_{FC})**: If there is a local trigger, but no readout trigger, then TS issues a CLEAR signal to the front end modules. Following a Local trigger, there is a dead period in TS until the Readout trigger or Fast Clear is issued.

Non-buffered mode – Single Crate

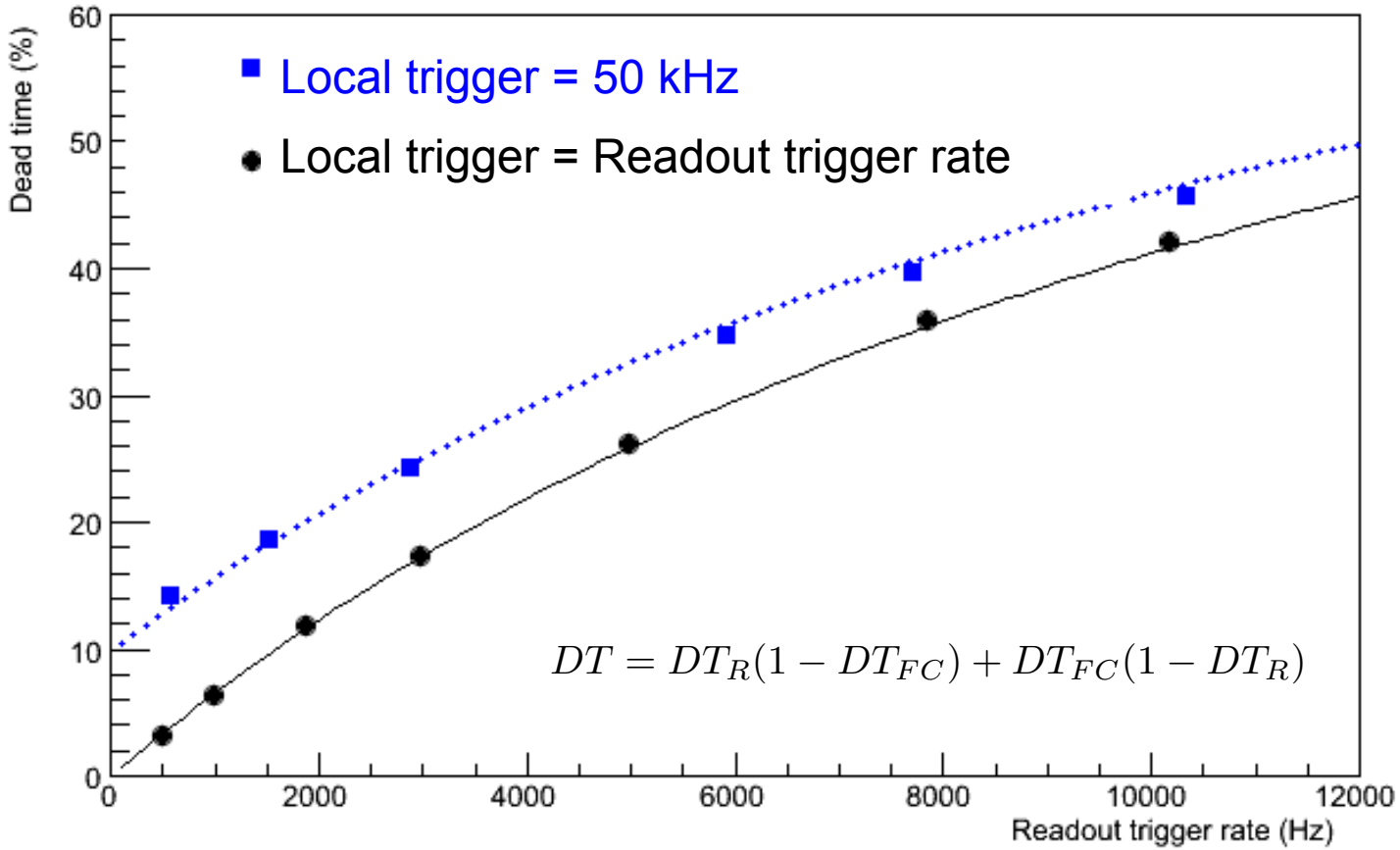
Dead time due to readout event,
L2 – average readout trigger rate

$$DT_R = \frac{\mathrm{L2}dt_R}{\mathrm{L2}dt_R + 1}$$

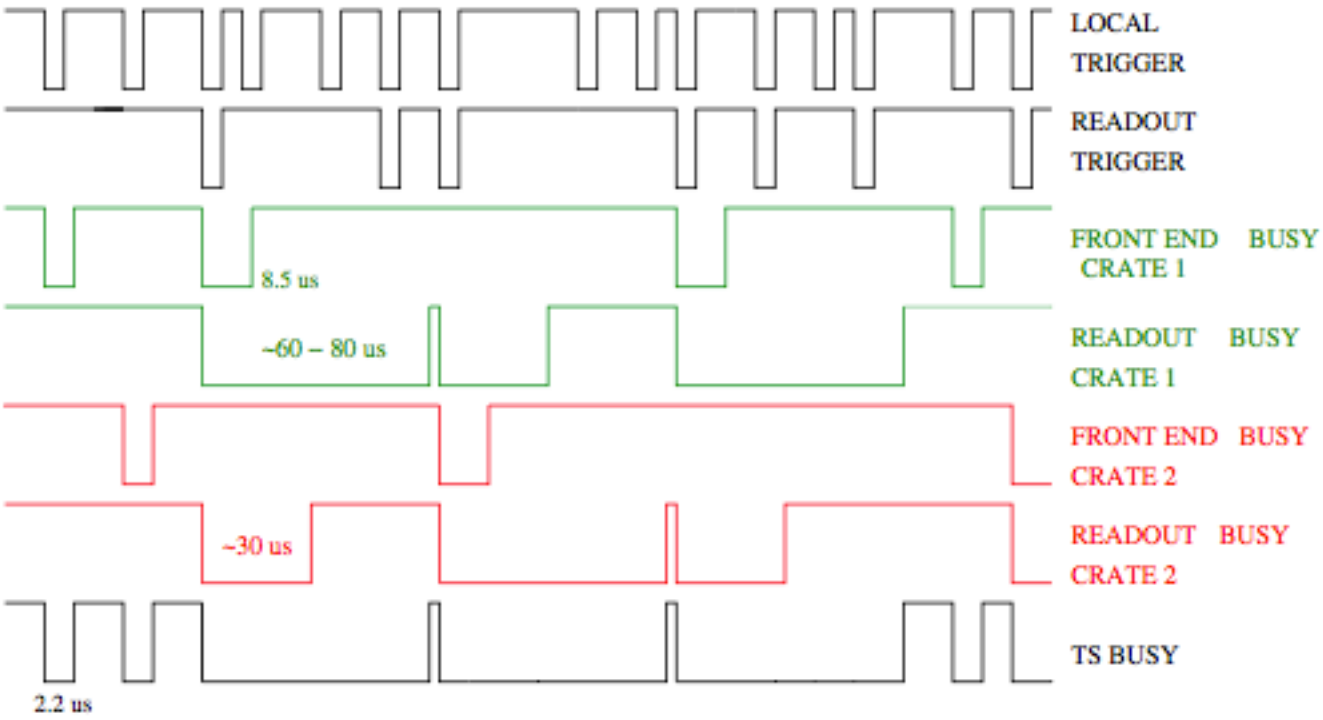
$dt_R \approx 70\mu s$

Dead time due to the fast cleared event,
L1 – average local trigger rate

$$DT_{FC} = \frac{(\mathrm{L1\text{-}L2})dt_{FC}}{(\mathrm{L1\text{-}L2})dt_{FC} + 1}$$



Non-buffered mode – Event Switching



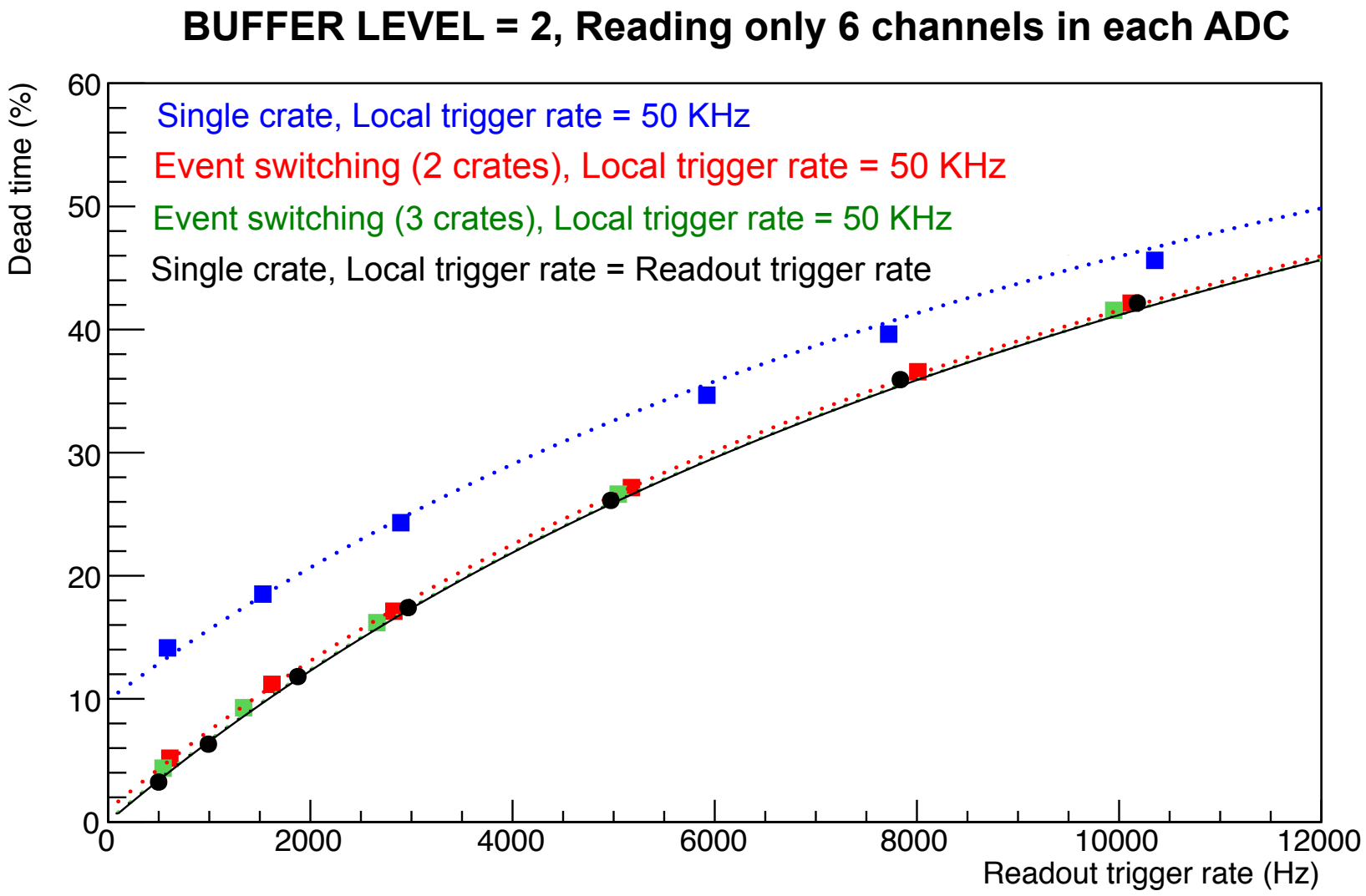
$$DT_R = \frac{\mathrm{L2}dt_R}{\mathrm{L2}dt_R + 1}$$

$$DT_{FC} = \frac{(\mathrm{L1\text{-}L2})dt_{FC}}{(\mathrm{L1\text{-}L2})dt_{FC} + 1}$$

Note that the dead time due to fast cleared events, is only occurred if all ***n*** crates are busy.

$$DT_{FC} = {DT_{FC}}^n$$

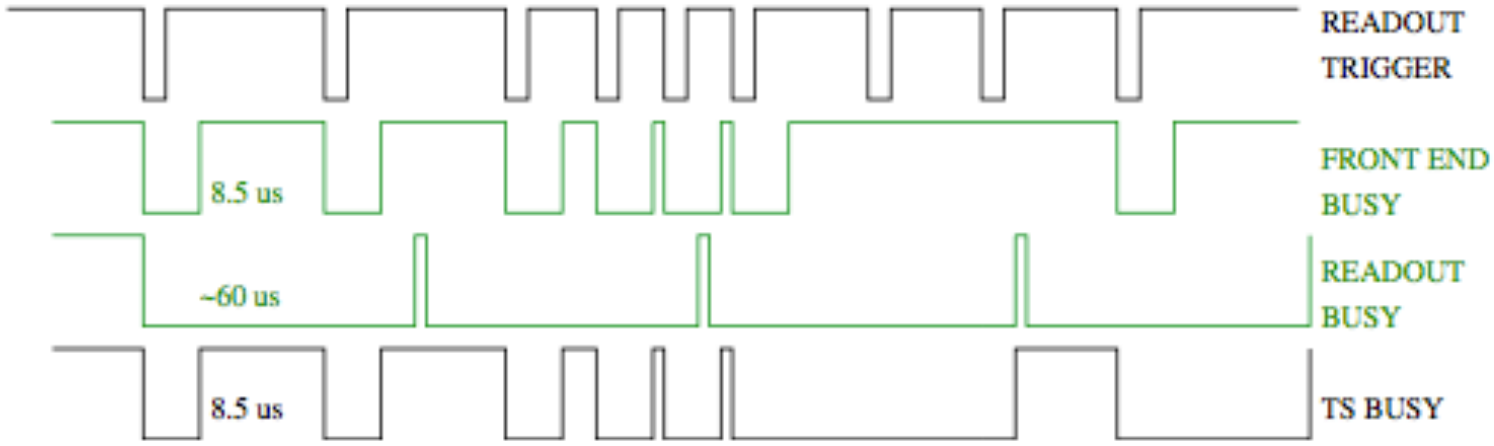
Non-buffered mode – Event Switching



Buffered Mode – Single Crate

Now, TS can process a new event while reading out previous event. The number of events processes at a time is defined as **BUFFER LEVEL**.

BUFFER LEVEL = 4



Dead time due to readout,

$$DT_R = \sum_{n=b}^{\infty} \frac{\mu_R^n e^{-\mu_R}}{n\ !}$$

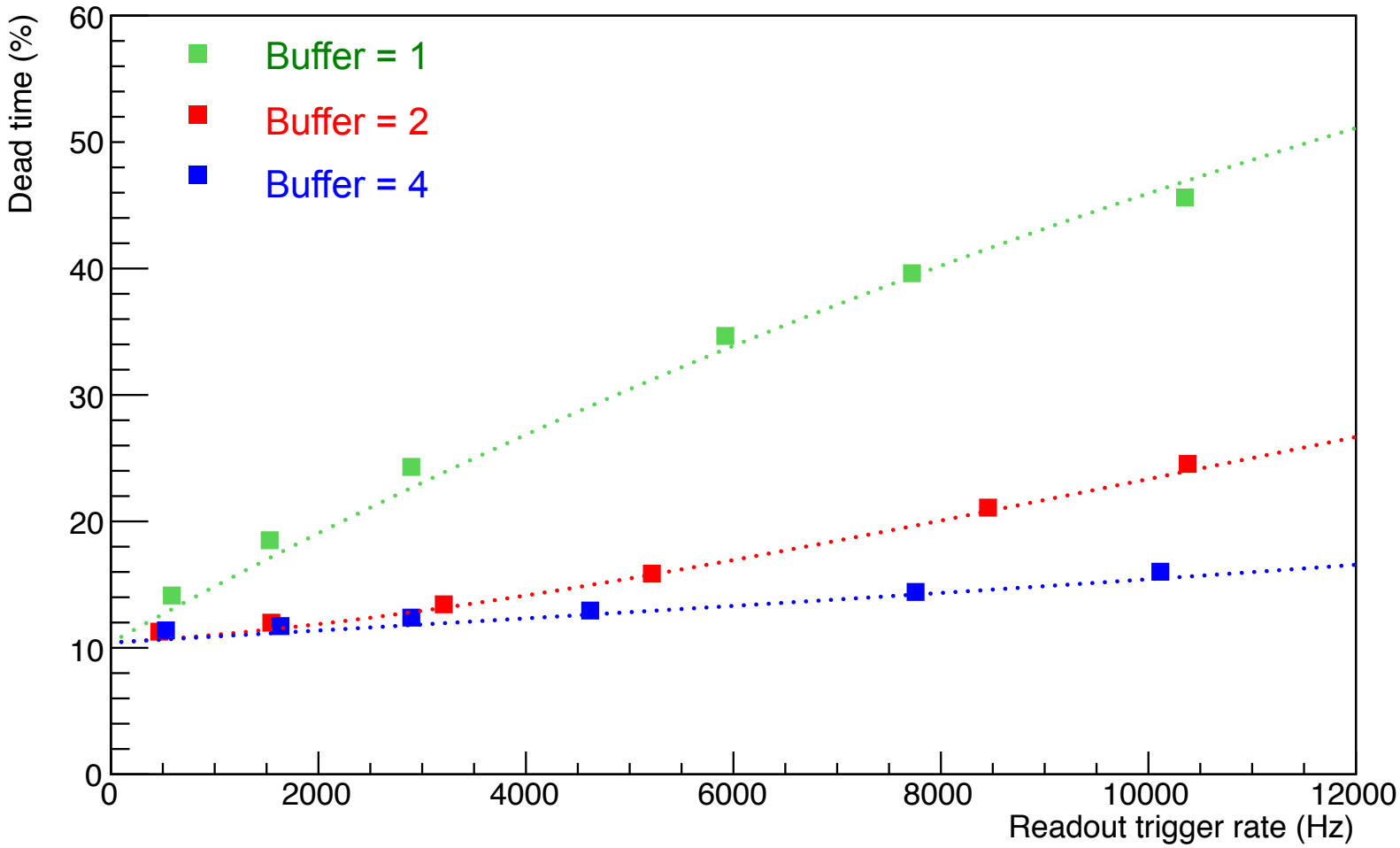
Dead time due to front-end busy,

$$DT_{FE} = \frac{\mathrm{L2}dt_{FE}}{\mathrm{L2}dt_{FE} + 1}$$

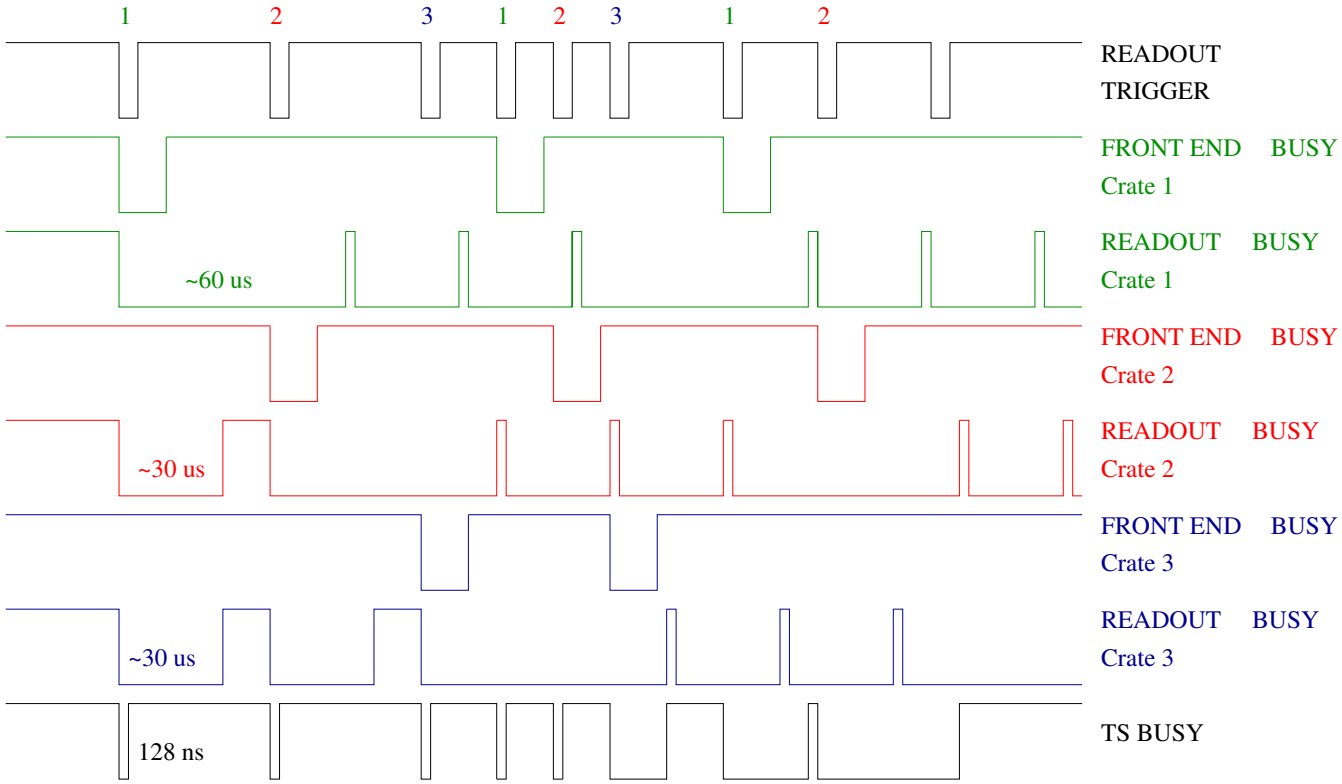
Note that the readout dead time is now contribute to the system only when the buffer is full.

Buffered Mode – Single Crate

Local trigger rate = 50 KHz, Reading 6 channels in each ADCs



Buffered Mode – Event Switching



Dead time due to the readout busy time in the FB crate which processes the readout

$$DT_{R1} = \sum_{n=b}^{\infty} \frac{\mu_{R1}^{n} e^{-\mu_{R1}}}{n\ !}$$

$$\mu_{R1} = L2.dt_R$$

$$dt_R \sim 60\mu s$$

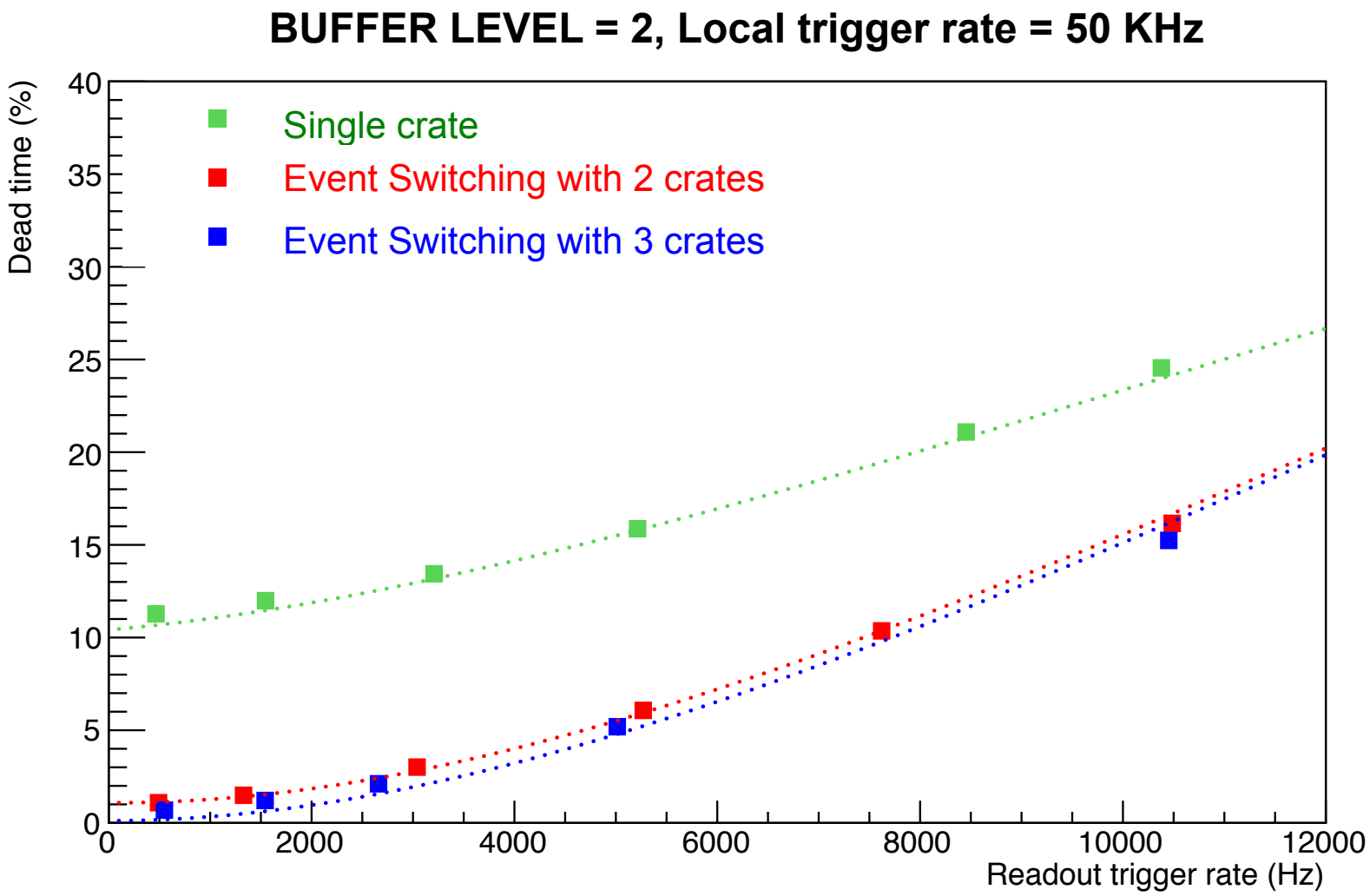
Dead time due to the additional readout busy time occurs in the other crates

$$DT_{R2} = \sum_{n=b}^{\infty} \frac{\mu_{R2}^{n} e^{-\mu_{R2}}}{n\ !}$$

$$\mu_{R2} = L2.dt_{R2}$$

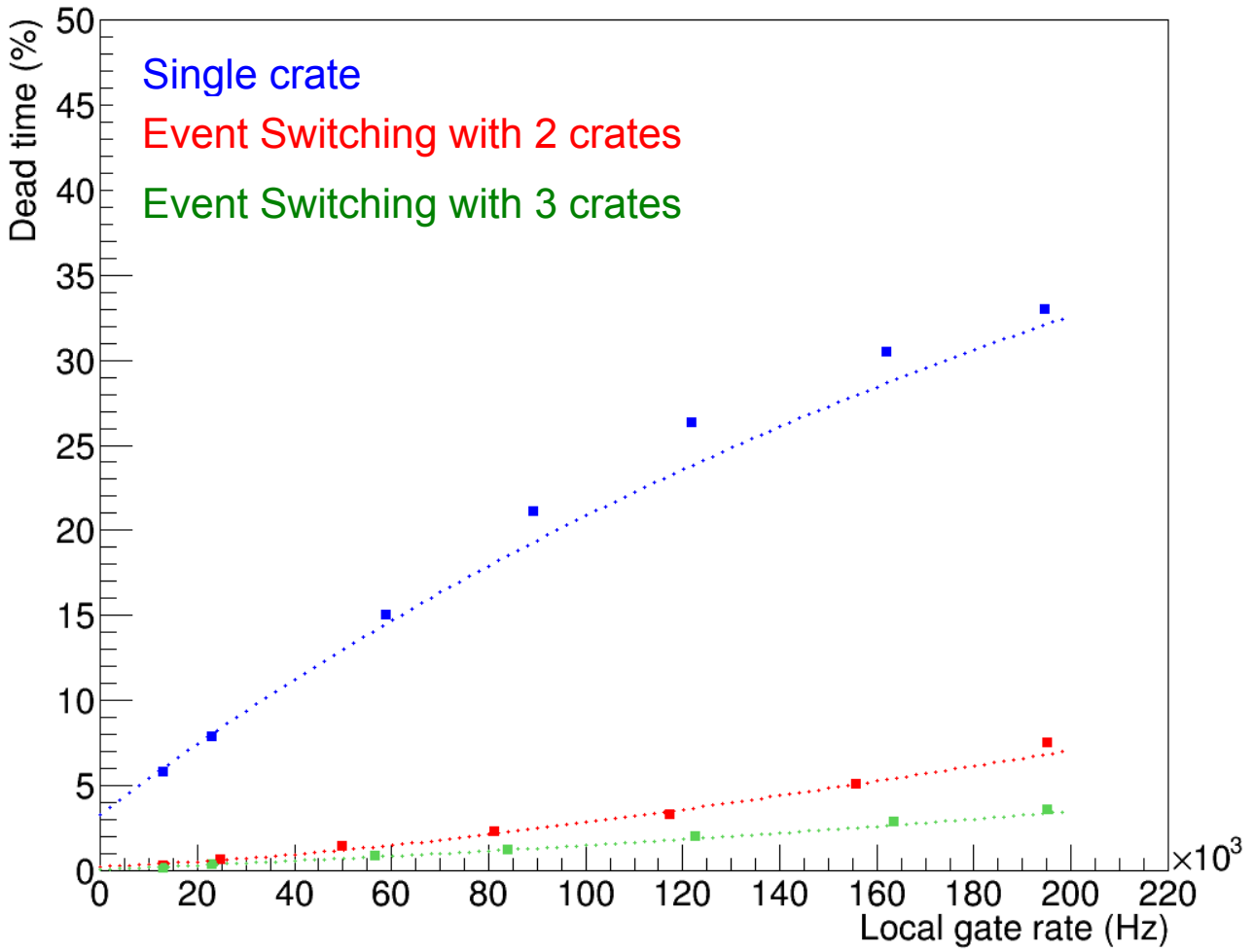
$$dt_{R2} \sim 30\mu s$$

Buffered Mode – Event Switching



Buffered Mode – Event Switching

BUFFER LEVEL = 4, Readout trigger rate = 5 KHz



Current Status

- Event switching:
  - Dead times study with event switching is completed.
  - Dead time model is developed and it is in good agreement with data. Details are documented.
  - Another test, along with GEM/HCal DAQ, is in progress to check the performance of event switching.
- FB crates:
  - ECal: 9 out of 12 crates have been tested with all the modules.
  - CDet: 2 crates have been tested.
- Installing Linux and other drivers to new Intel vme CPUs.
  - Completed installation - 3 CPUs. Instructions are documented.
  - Need to setup CODA.
- Need to work on the decoder we are using for ECal DAQ and add the modifications to the Hall A analyzer.

Thanks Alexander Camsonne, Robert Michaels, William Gu and Bryan Moffit for support and guidance.