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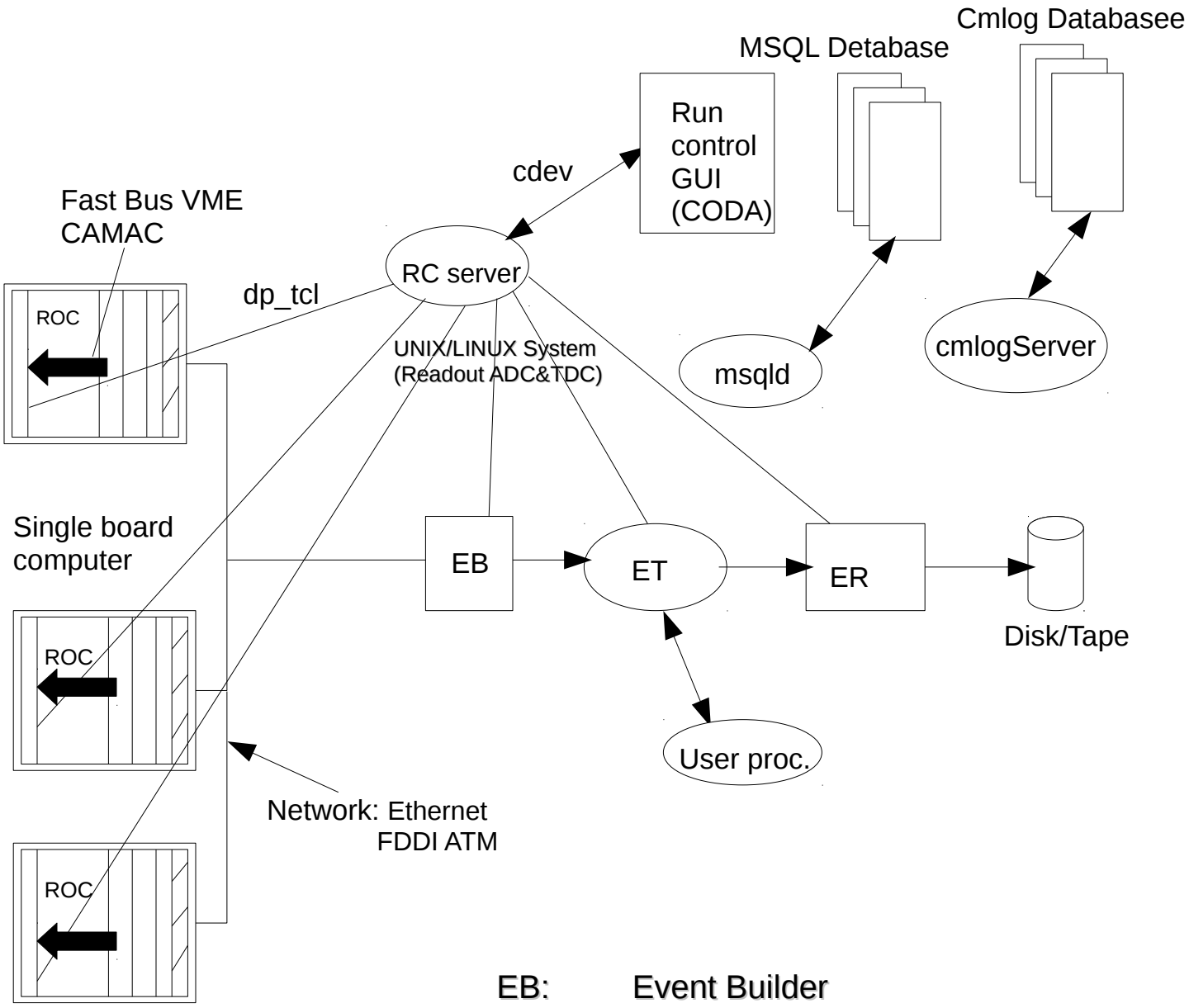
Schematic Diagram of DAQ



EB: Event Builder
ET: Event Transfer
ER: Event Reader
ROC: Readout controller
(Filled with ADC&TDC)
GUI: Graphical Interface

Note: This whole process takes one event at time.

Fig1: Hall A DAQ

Schematic for Trigger System

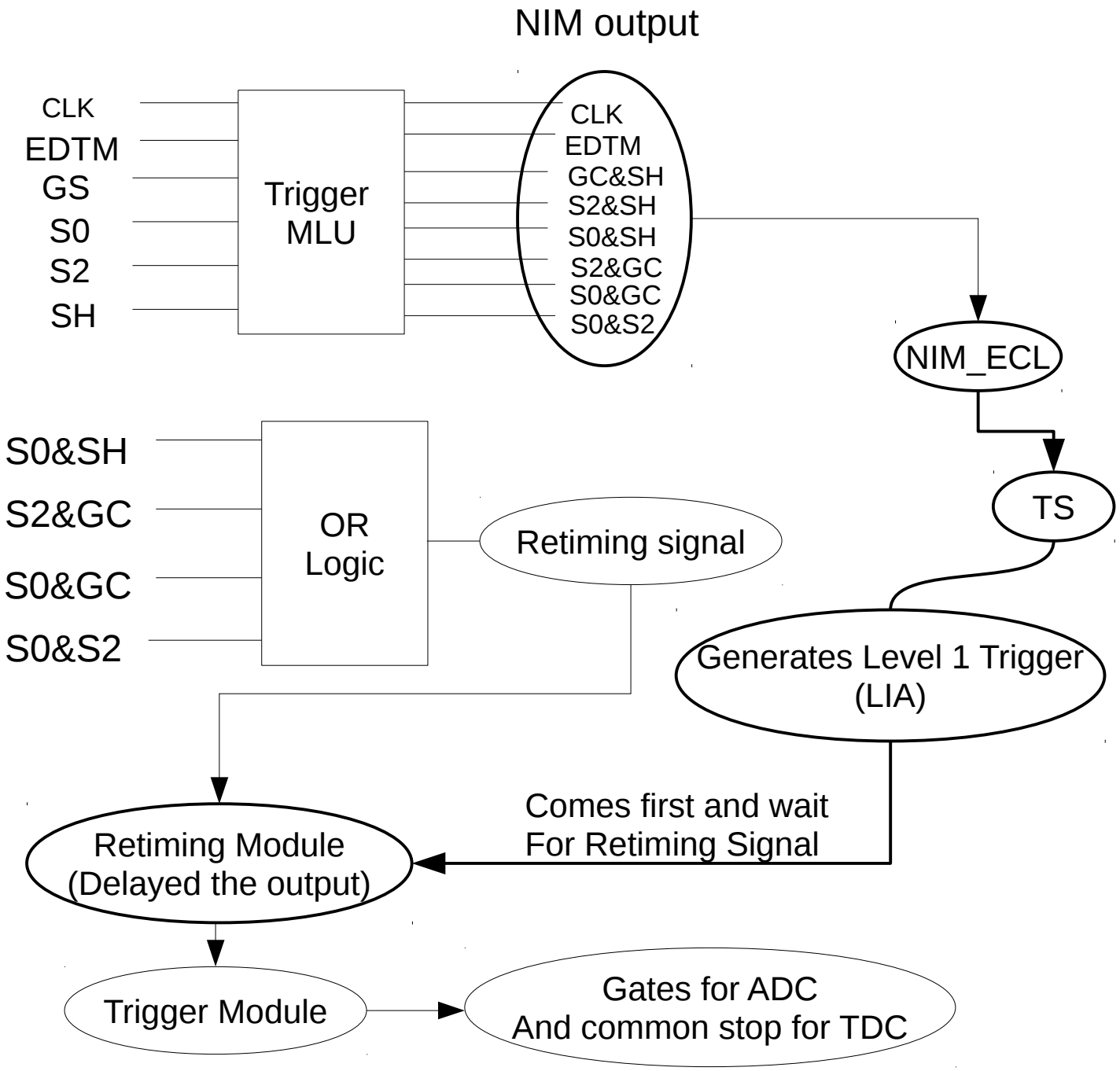


Fig 2: Hall A Trigger System

DAQ: A block diagram of Hall A DAQ(data acquisition) system is shown in fig. 1. The DAQ software is based on CODA(CEBAF online data acquisition) package developed by the Jlab CODA group. Hardware components includes Trigger Supervisor(TS) module, Analog to digital converters(ADCs), Time to digital converters(TDCs) and scalar modules. The TDC, ADC and scalar modules are either Fastbus or VME-type. After entering hits from the detectors, the crates are read out by read out controllers(ROC's), which are CODA routines running under the VxWorks operating system . The information's from ROC's are then passed over to event builder(EB). The EB is a routine that wait for the connection requested from ROC's, collect their fragments, order and merge the piece in to a single data structure in CODA format. The events are then passes to the ER(Event recorder), Which is a coda routine that write a event on disk and are finally transferred to the central data server.

Trigger design: Triggers are the electronic signals that assist the DAQ to start read out of the detectors information. The trigger design for the halla DAQ is shown in fig.2. Signals from four detectors -S0 scintillator, S2m scintillator, gas Cherenkov and calorimeter are sent to the front-end electronics. Logical pulses from each of these detectors is then sent to a trigger module based on VME programmable logic(MLU module). This allows various combination of detectors in the trigger. Here the input to MLU also includes EDTM and clock. The outputs of MLU can be adjusted to either from coincidence between different inputs or simply copy inputs. NIM outputs are then fed to the Trigger Supervisor (TS) via NIM_ECL. TS located in the electronic hut on the second floor. When a trigger is accepted by the TS, a level one-accept (L1A) signal is generated. L1A and the retiming signals are then send to retiming module where they form a coincidence. Then the coincidence signal fed to the trigger module(TM) where an ADC gate, and TDC start/stop are generated. These are then distributed to the front end of the electronics on the fast bus crate and VME crates where ADC's, TDC's and scalars start to record data when these signals arrive.