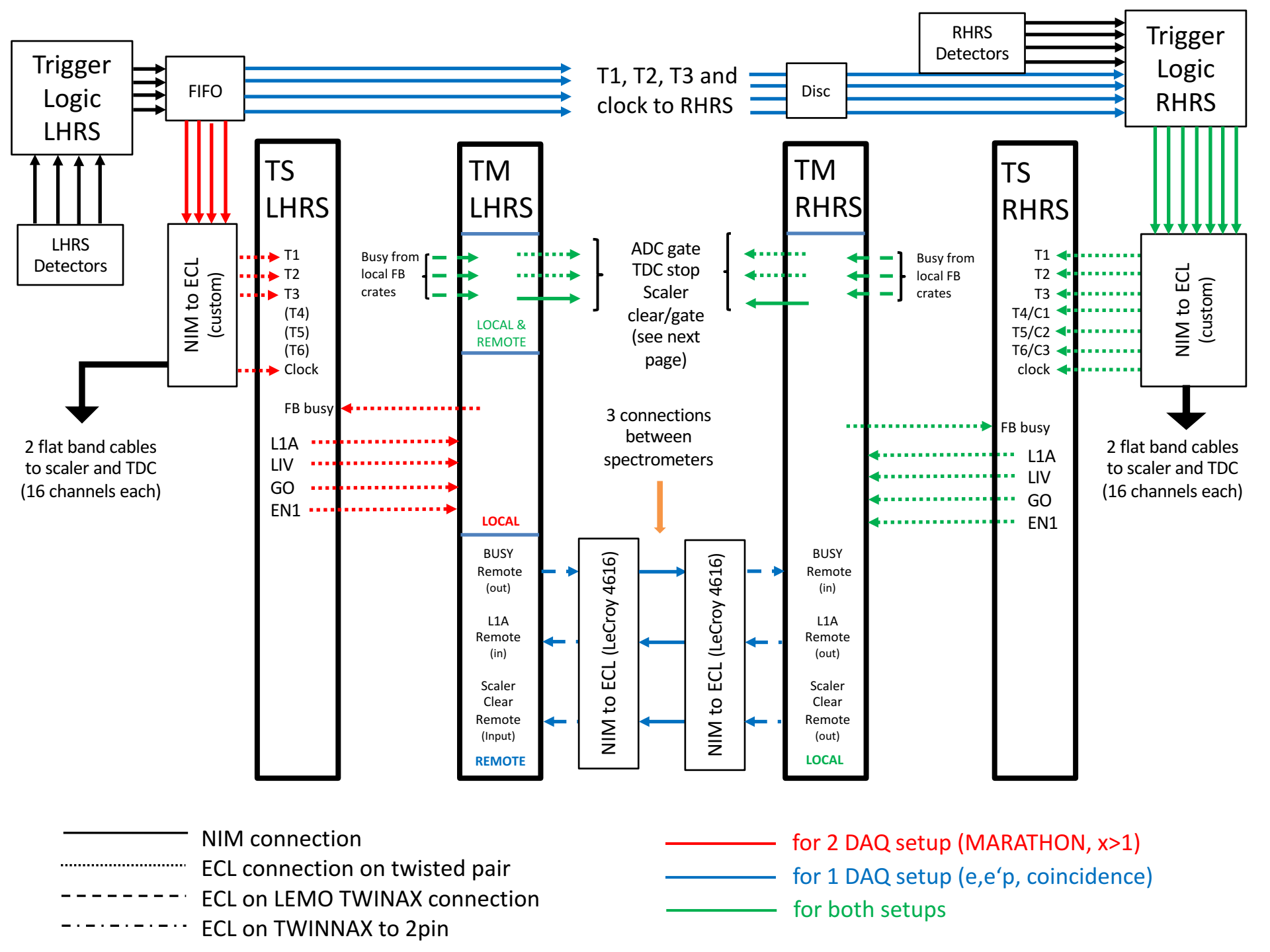
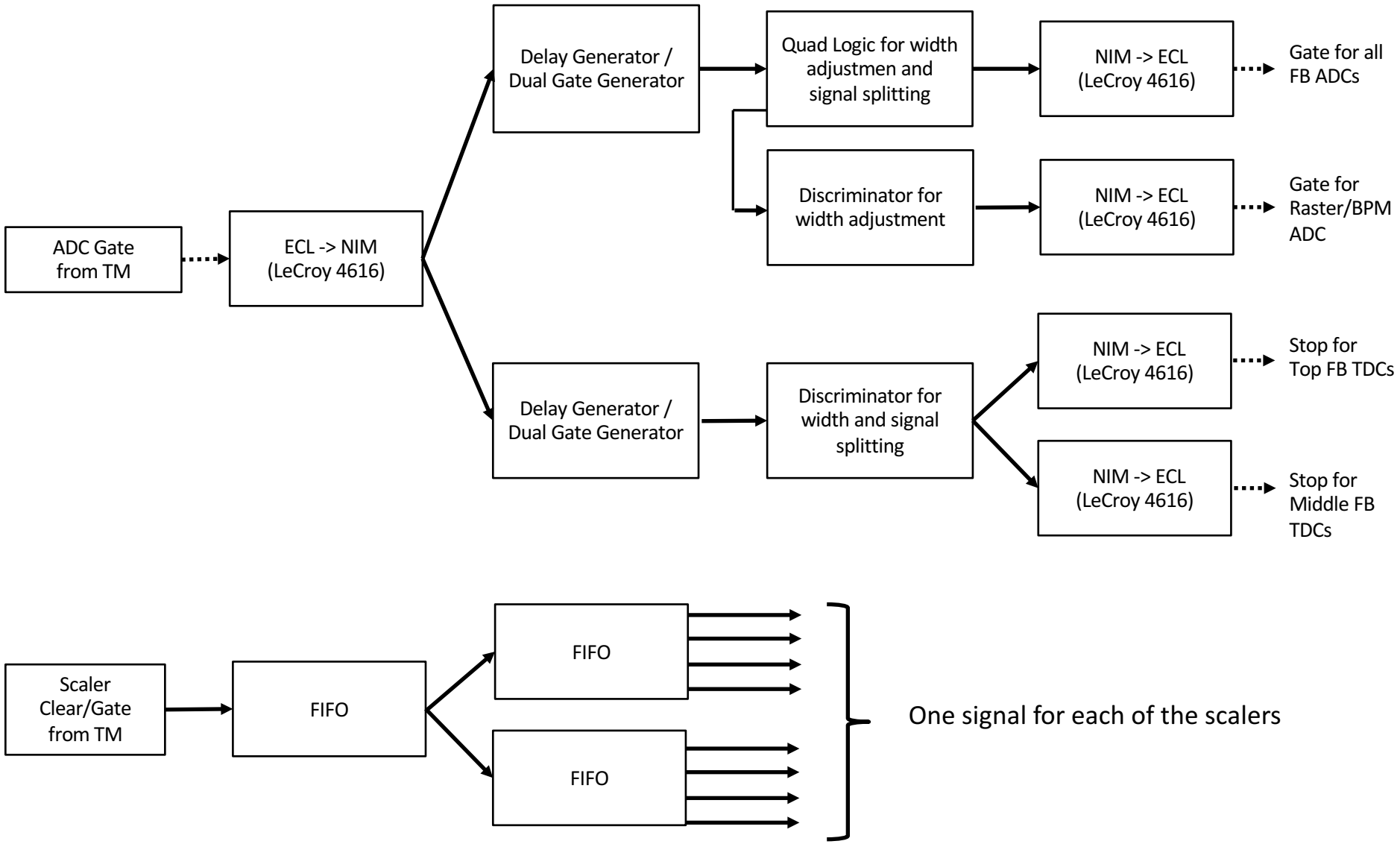
Trigger Considerations

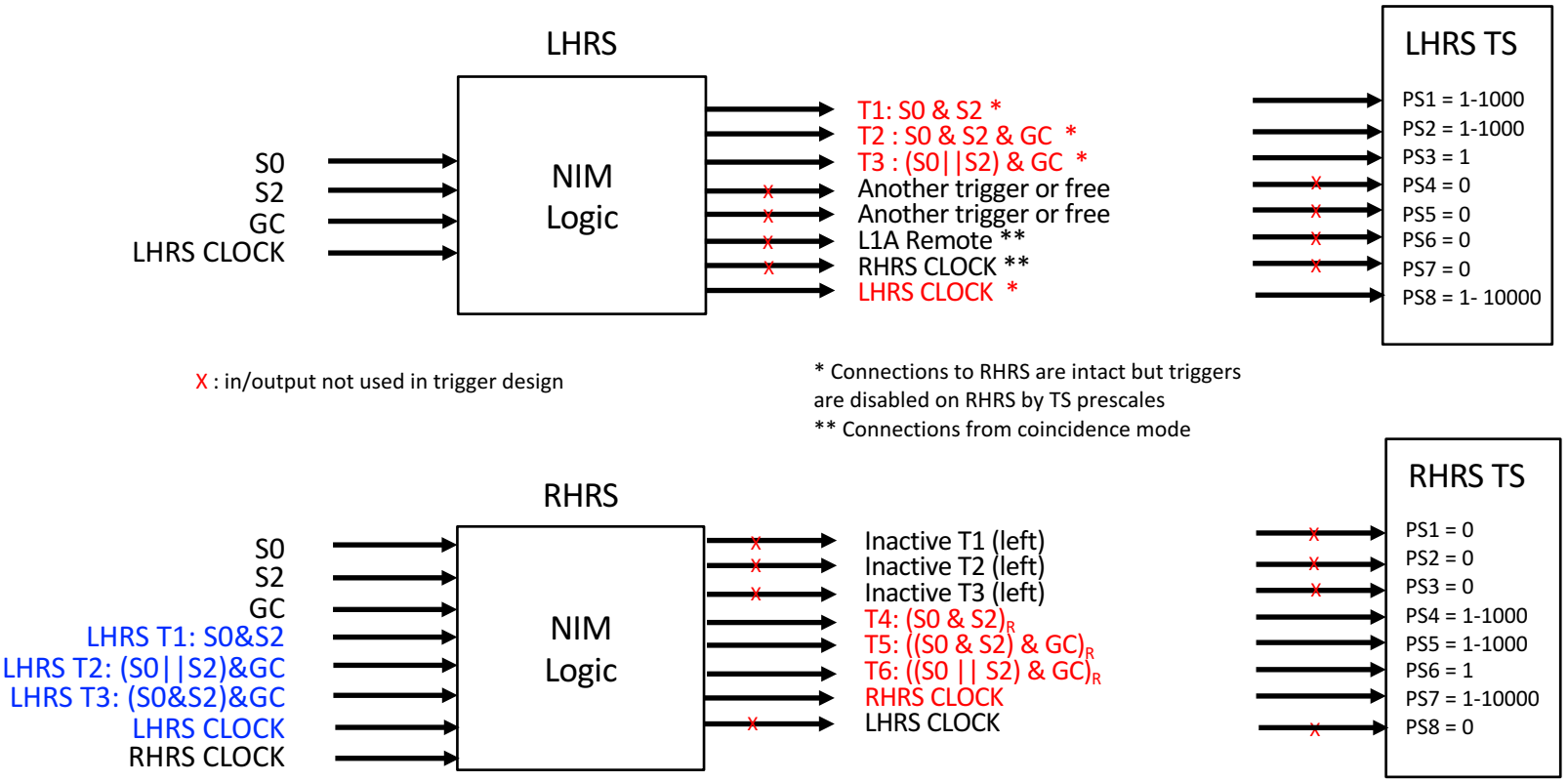
- Switching between single arm and coincidence mode fast, easy and as little hardware changes as possible
- Implementation of triggers in NIM logic
- No “cheating“ in coincidence mode as during Argon run
- No Retiming of signals (no RT module)
- RHRS TS is controlling DAQ in coincidence mode


Trigger Logic LHRS
FIFO
T1, T2, T3 and clock to RHRS
Disc
RHRS Detectors
Trigger Logic RHRS
LHRS Detectors
NIM to ECL (custom)
TS LHRS
TM LHRS
TM RHRS
TS RHRS
T1
T2
T3
(T4)
(T5)
(T6)
Clock
Busy from local FB crates
LOCAL & REMOTE
ADC gate
TDC stop
Scaler clear/gate
(see next page)
T4/C1
T5/C2
T6/C3
clock
NIM to ECL (custom)
2 flat band cables to scaler and TDC (16 channels each)
FB busy
L1A
LIV
GO
EN1
3 connections between spectrometers
LOCAL
BUSY Remote (out)
L1A Remote (in)
Scaler Clear Remote (Input)
REMOTE
NIM to ECL (LeCroy 4616)
NIM to ECL (LeCroy 4616)
BUSY Remote (in)
L1A Remote (out)
Scaler Clear Remote (out)
LOCAL
NIM connection
ECL connection on twisted pair
ECL on LEMO TWINAX connection
ECL on TWINNAX to 2pin
for 2 DAQ setup (MARATHON, x>1)
for 1 DAQ setup (e,e‘p, coincidence)
for both setups

Flow of ADC gate, TDC stop and scaler signals for both arms

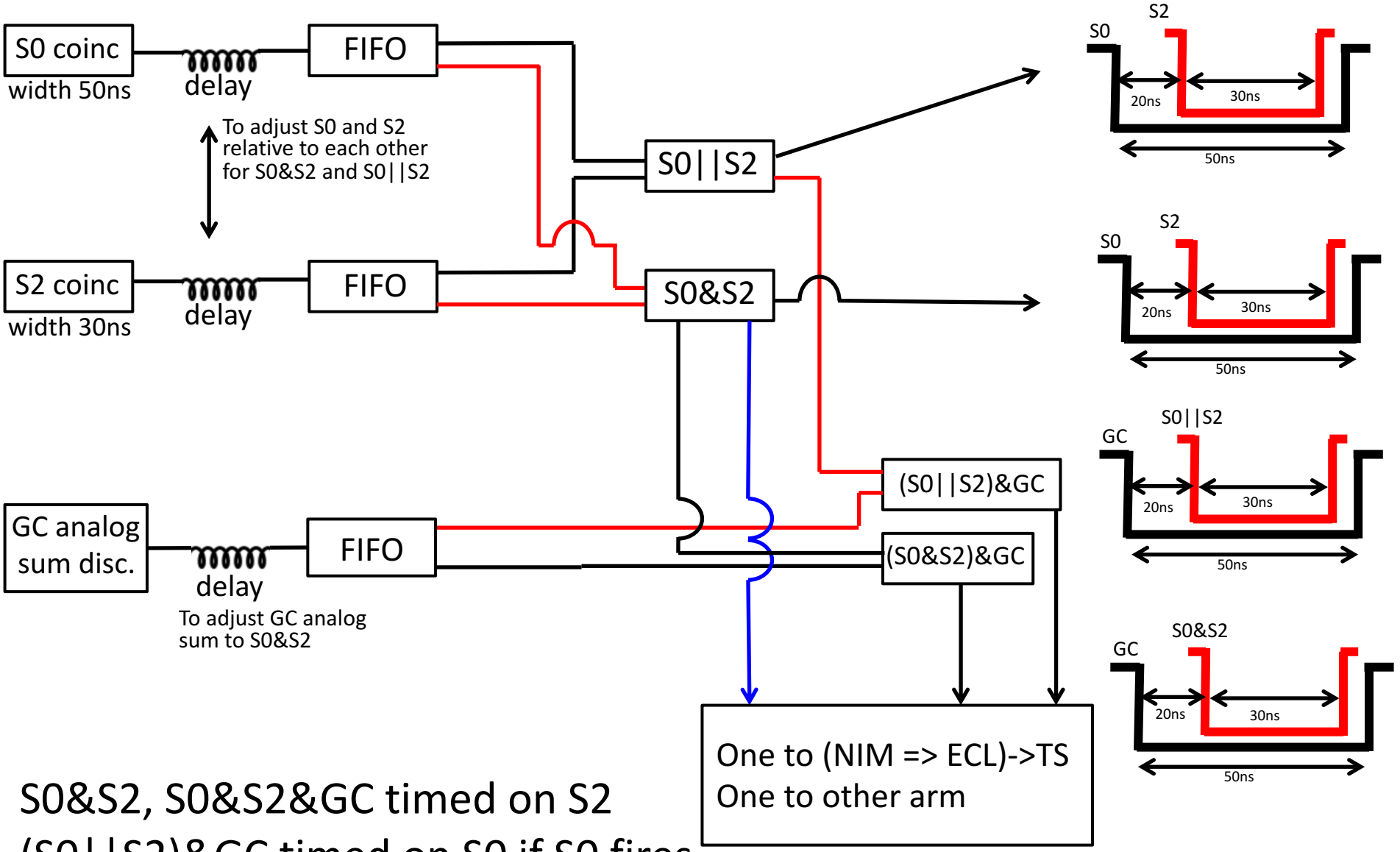


Trigger Logic for 2 DAQ mode (single arm configuration)



- Some of the signals on the RHRS have to be delayed to be in time with LHRS triggers
- T1 – T3 LHRS single triggers - similar for all experiments
- T4 – T6 RHRS single triggers

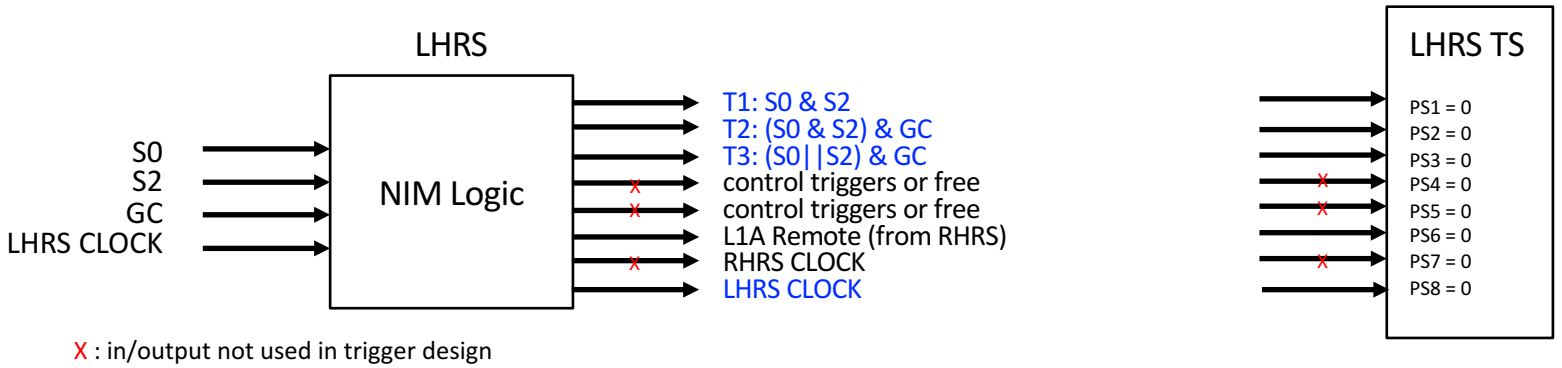
Single Arm Triggers (S0&S2); (S0&S2)&GC; (S0||S2)&GC



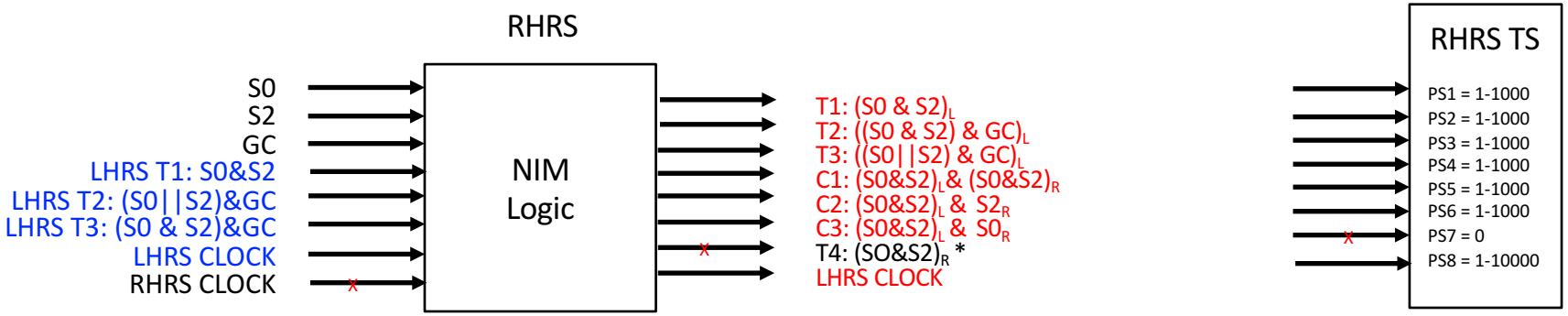
S0&S2, S0&S2&GC timed on S2

(S0||S2)&GC timed on S0 if S0 fires

Trigger Logic for 1 DAQ mode (concidence configuration)



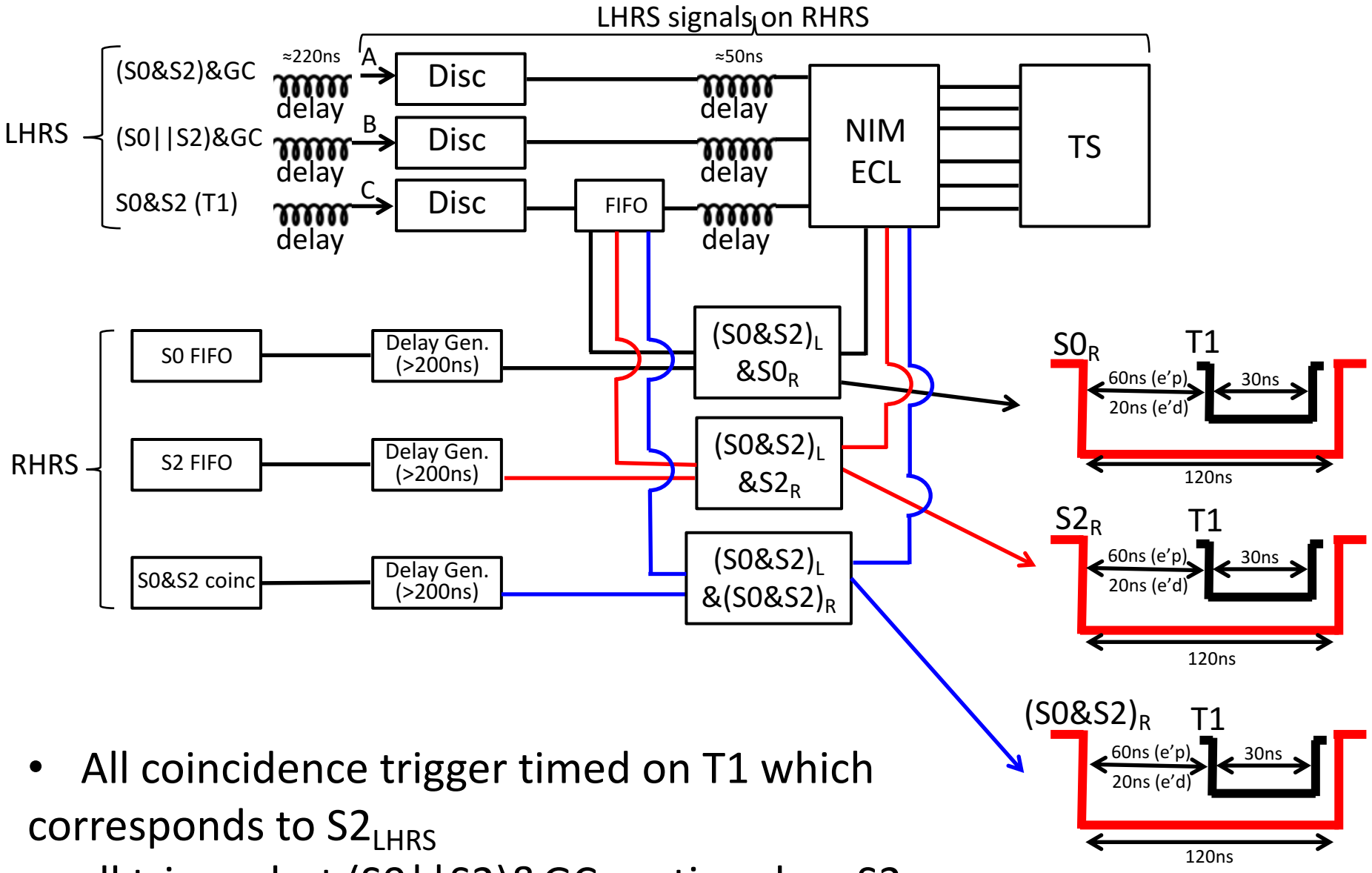
X : in/output not used in trigger design



* Usually disabled, necessary for right arm cosmics or right arm calibration

- Some of the signals on the RHRS have to be delayed to be in time with LHRS triggers
- T1 – T3 LHRS single triggers
- C1 – C3 Coincidence triggers

Coincidence triggers



- All coincidence trigger timed on T1 which corresponds to $S2_{LHRS}$

-> all trigger but $(S0||S2)\&GC_{LHRS}$ timed on $S2_{LHRS}$

- $(S0||S2)\&GC_{LHRS}$ timed on $S0_{LHRS}$ if S0 fires

Signals Exchange LHRS and RHRS

Necessary signal exchange:

- T1: NIM, fast timing
- T2: NIM, fast timing
- T3: NIM, fast timing
- LHRS clock: NIM, could be slow timing
- RHRS clock: NIM, could be slow timing
- Retiming signal: NIM, fast timing
- Scaler: ECL with LEMO TWINNAX connectors, could be slow timing
- Busy: ECL with LEMO TWINNAX connectors, could be slow timing
- L1A: ECL with LEMO TWINNAX connectors, fast timing
- Flatband RS485 connection TS to LHRS Fastbus crates

Available cables (found):

- 6 fast coax cables (222ns, Lemo connectors)
- 3 slower cables (240ns, Lemo connectors)
- 1 Flatband RS485 cable (not fully operational -> has to be tested)

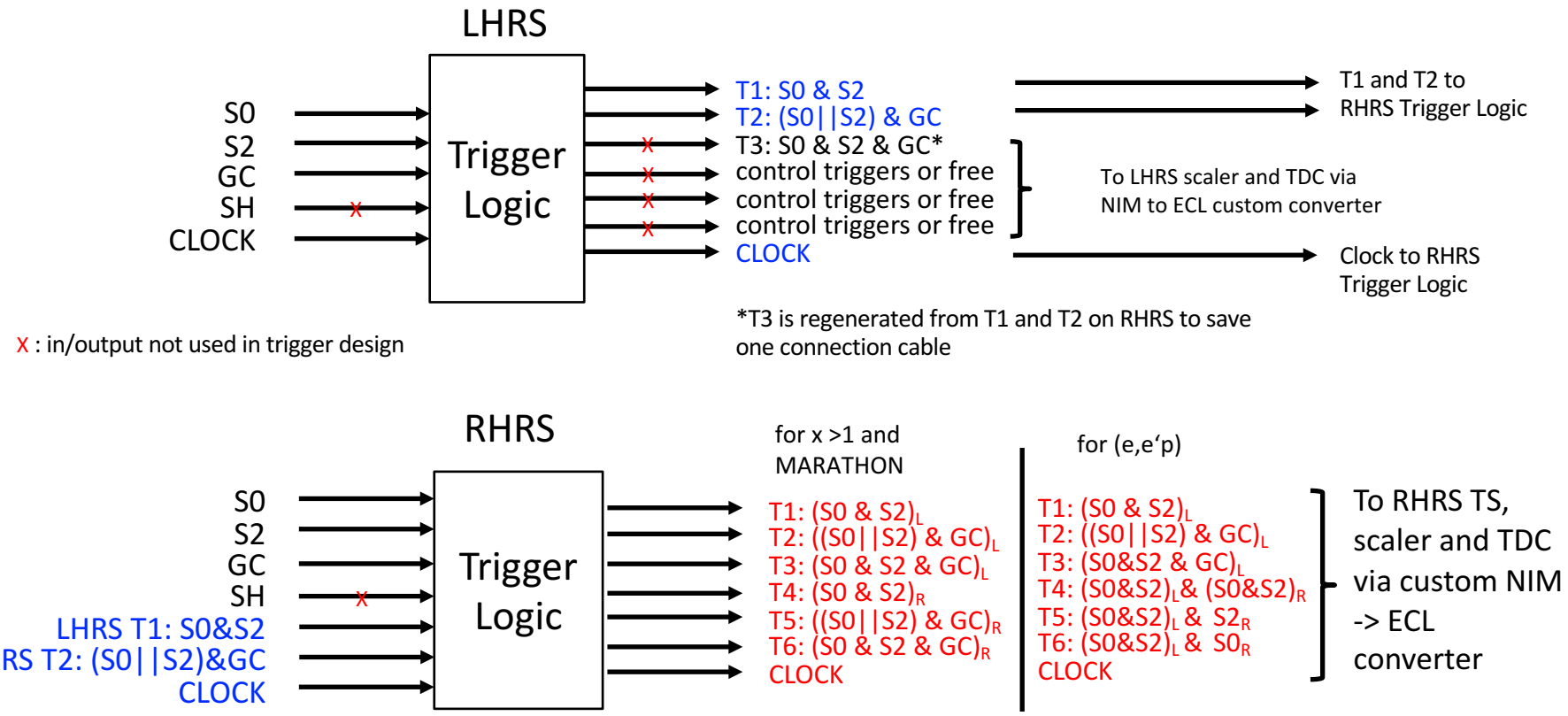
Not Available:

- 2 cables with LEMO TWINNAX connectors

Status at 09/13/17

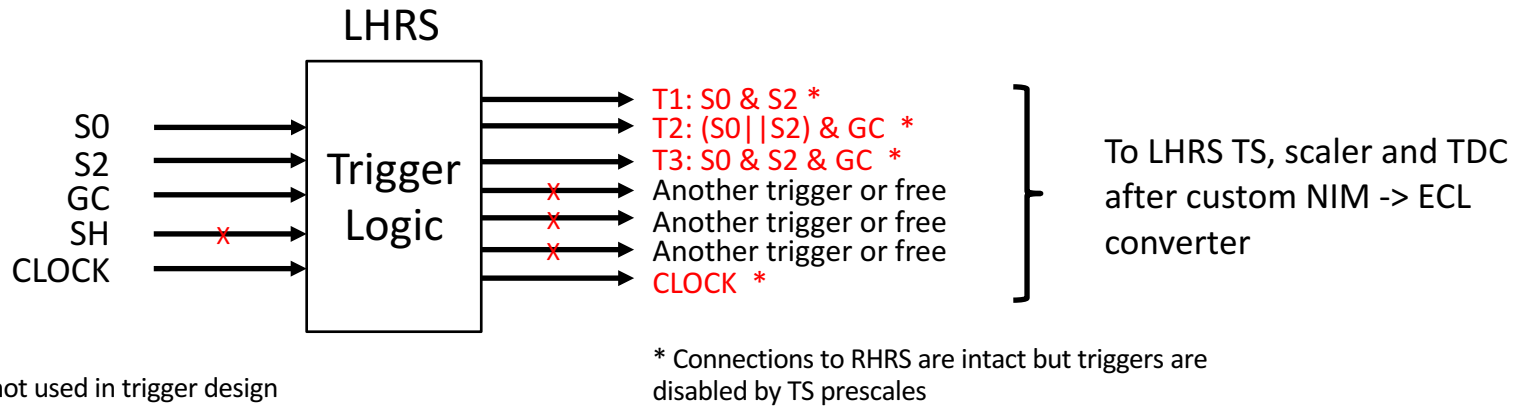
- Done:
  - Single arm trigger setup (connections and timing)
  - Coincidence trigger connections
- Current work:
  - Coincidence trigger timing with physics simulation using the clock
  - Connection of TM remote signals
- Next steps:
  - Coincidence simulation with additional randoms
  - Timing of trigger inputs in TS

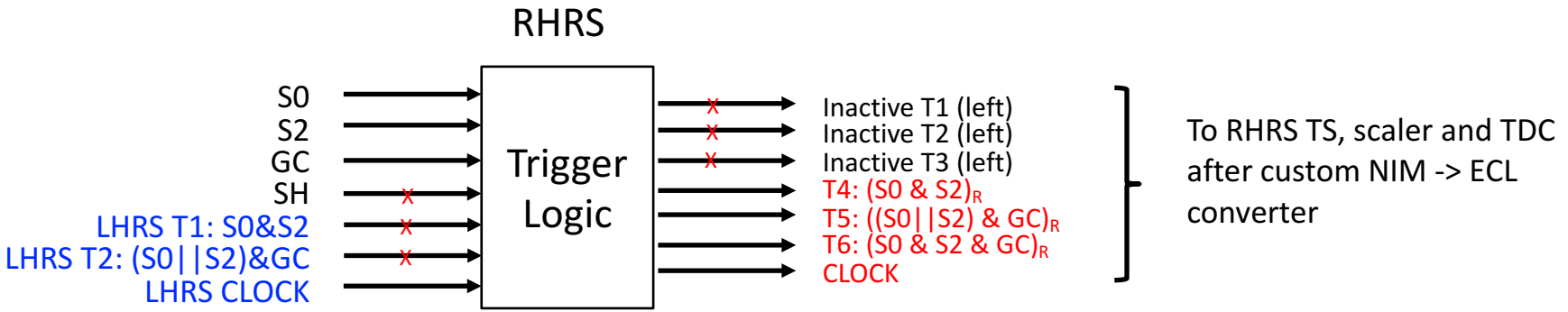
Trigger Logic for 1 DAQ mode



- Trigger logic can be either NIM or MLU or both with one output as control in scaler and TDC
- Some of the signals on the RHRS have to be delayed to be in time with LHRS triggers
- T1 – T3 LHRS triggers - similar for all experiments
- T4 – T6 RHRS triggers (single or concidence triggers)

Trigger Logic for 2 DAQ mode

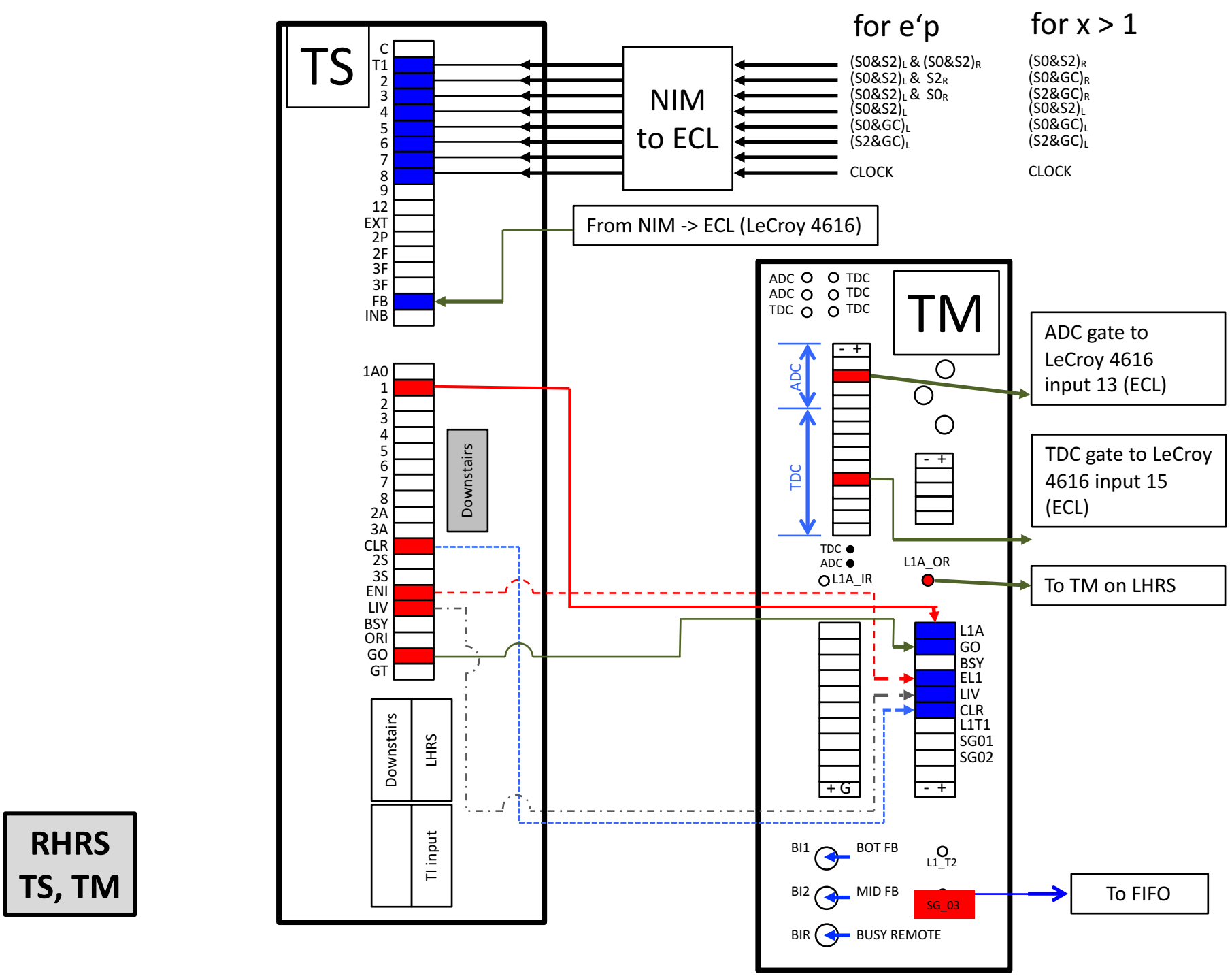


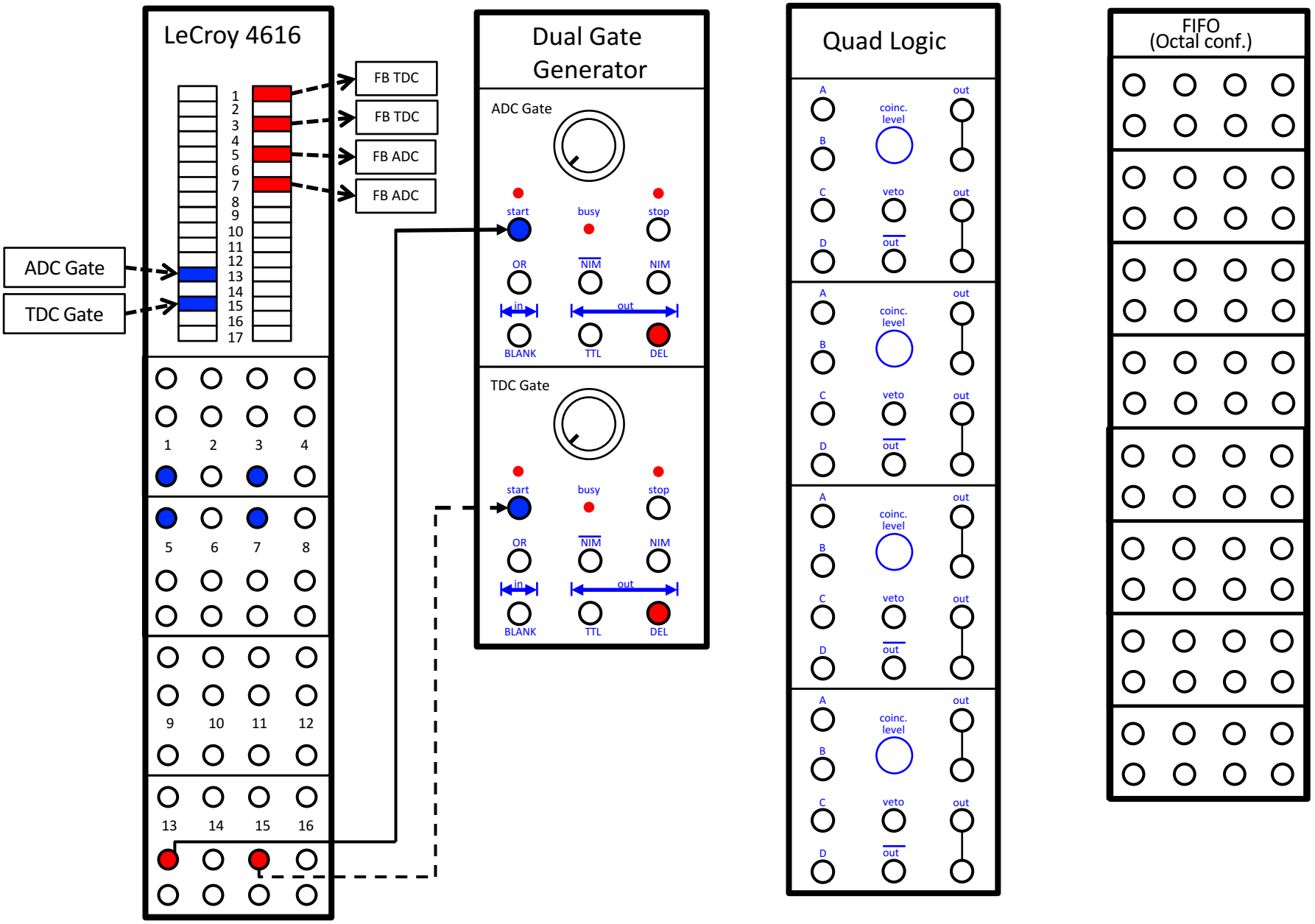


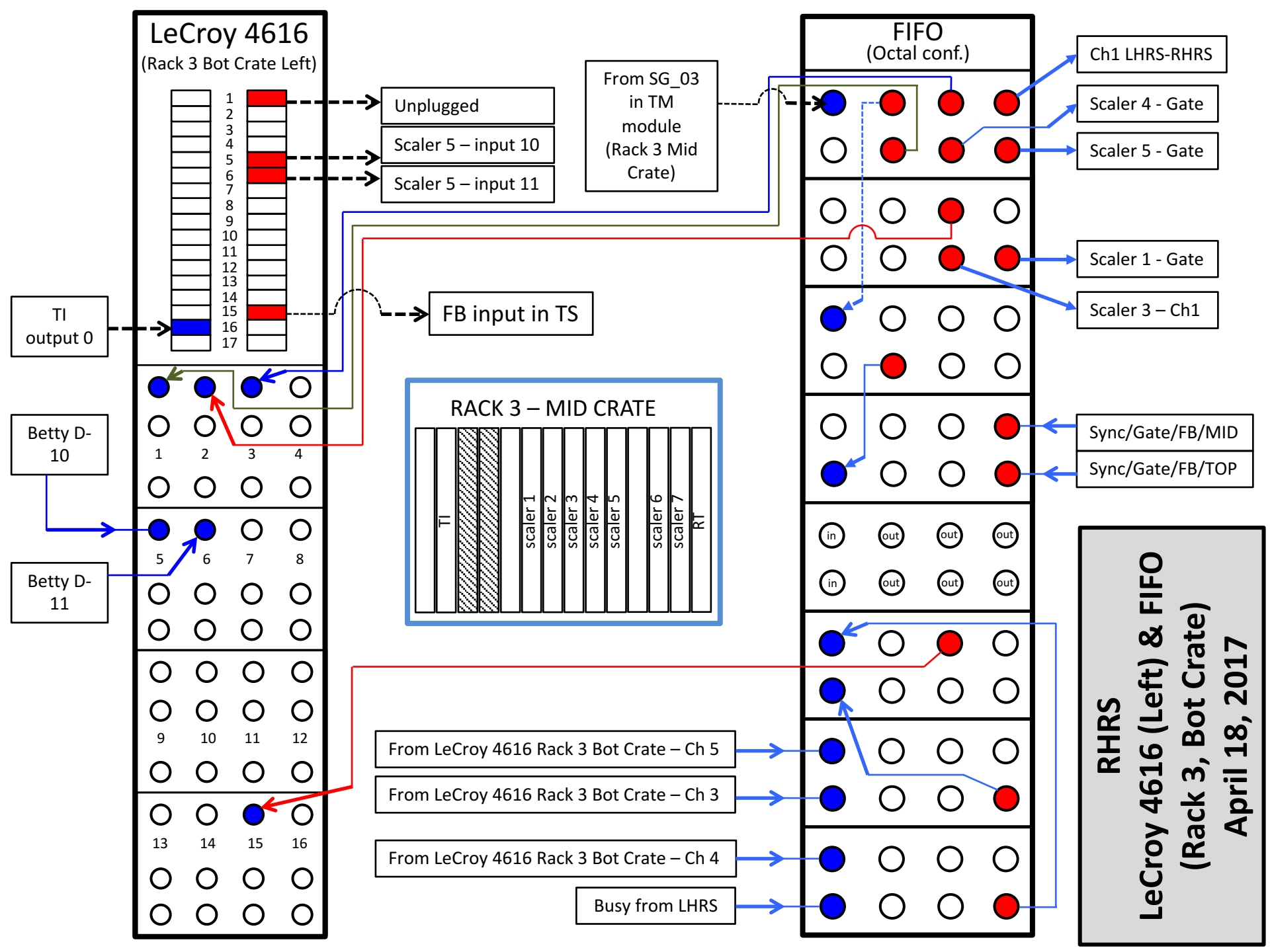
- Trigger logic can be either NIM or MLU or both with one output as control in scaler and TDC
- T1 – T3 LHRS single triggers
- T4 – T6 RHRS single triggers
- Single triggers are fed to the indivual TS of the corresponding sides
- Using more triggers on the RHRS involves changing cables

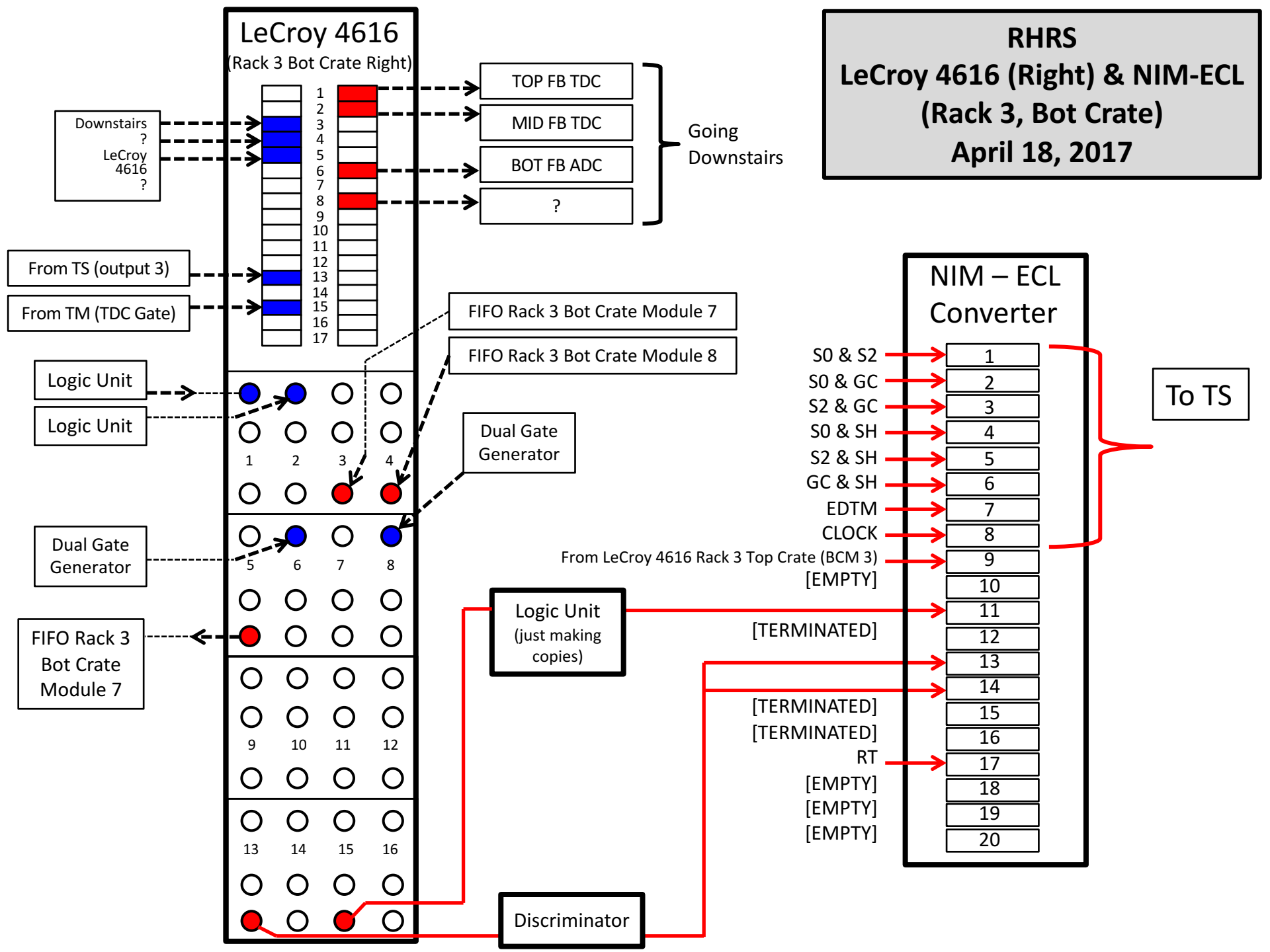
Next slides are not up to date!!!
27 June 2017

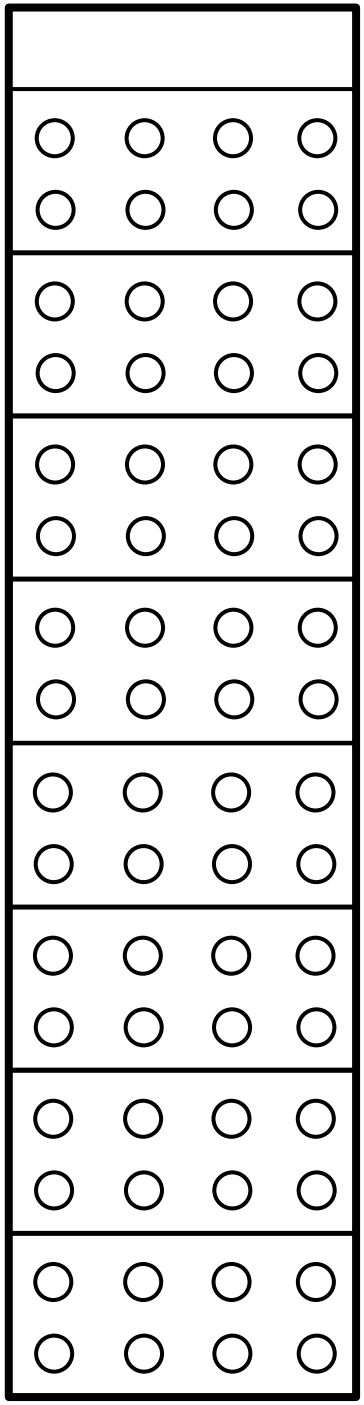
have to be modified for correct setup

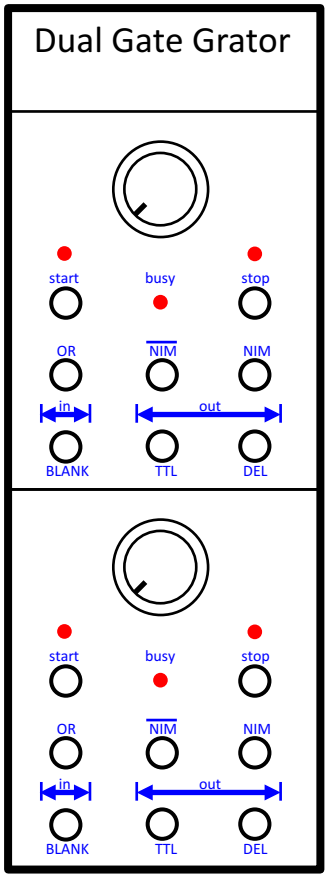

RHRS
TS, TM
TS
C
T1
2
3
4
5
6
7
8
9
12
EXT
2P
2F
3F
3F
FB
INB
NIM
to ECL
for e'p
(S0&S2)L & (S0&S2)R
(S0&S2)L & S2R
(S0&S2)L & S0R
(S0&S2)L
(S0&GC)L
(S2&GC)L
CLOCK
for x > 1
(S0&S2)R
(S0&GC)R
(S2&GC)R
(S0&S2)L
(S0&GC)L
(S2&GC)L
CLOCK
From NIM -> ECL (LeCroy 4616)
1A0
1
2
3
4
5
6
7
8
2A
3A
CLR
2S
3S
ENI
LIV
BSY
ORI
GO
GT
Downstairs
Downstairs
LHRS
TI input
TM
ADC
ADC
TDC
TDC
TDC
TDC
ADC
TDC
TDC
ADC
L1A_IR
L1A_OR
+ G
L1A
GO
BSY
EL1
LIV
CLR
L1T1
SG01
SG02
BI1
BOT FB
L1_T2
BI2
MID FB
SG_03
BIR
BUSY REMOTE
ADC gate to LeCroy 4616 input 13 (ECL)
TDC gate to LeCroy 4616 input 15 (ECL)
To TM on LHRS
To FIFO

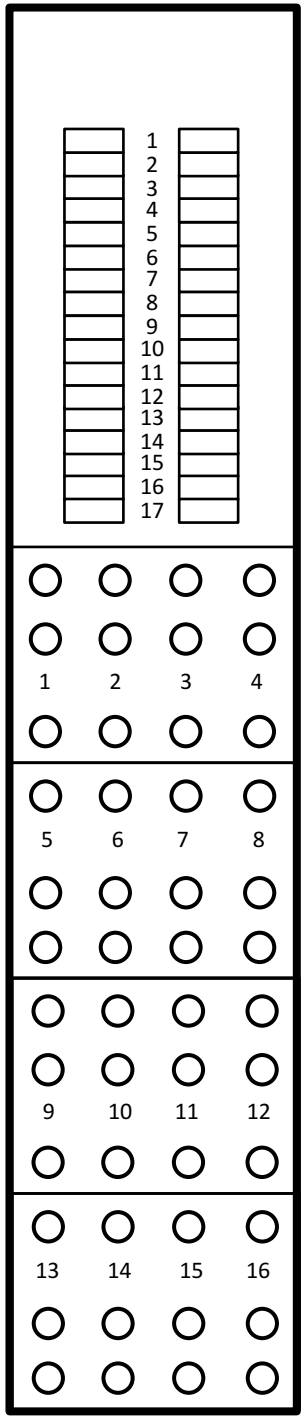

LeCroy 4616
FB TDC
FB TDC
FB ADC
FB ADC
ADC Gate
TDC Gate
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
1 2 3 4
5 6 7 8
9 10 11 12
13 14 15 16
Dual Gate Generator
ADC Gate
start
busy
stop
OR
NIM
NIM
in
out
BLANK
TTL
DEL
TDC Gate
start
busy
stop
OR
NIM
NIM
in
out
BLANK
TTL
DEL
Quad Logic
A
B
C
D
coinc. level
veto
out
FIFO (Octal conf.)

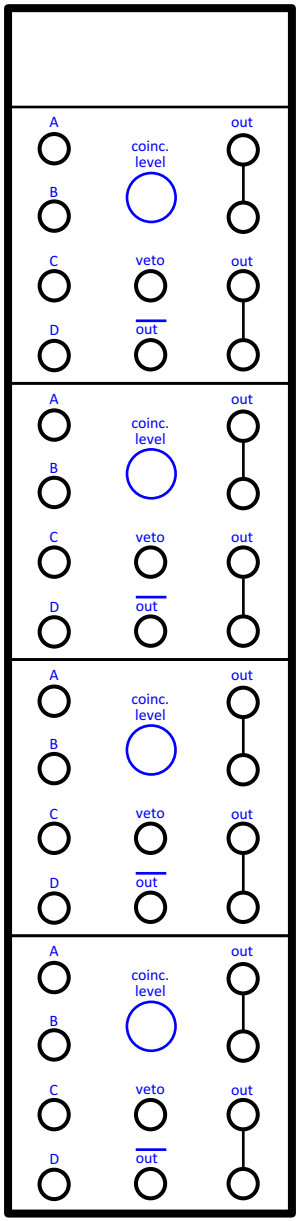

LeCroy 4616
(Rack 3 Bot Crate Left)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
Unplugged
Scaler 5 – input 10
Scaler 5 – input 11
From SG_03 in TM module (Rack 3 Mid Crate)
FB input in TS
TI output 0
Betty D-10
Betty D-11
RACK 3 – MID CRATE
TI
scaler 1
scaler 2
scaler 3
scaler 4
scaler 5
scaler 6
scaler 7
RT
FIFO
(Octal conf.)
Ch1 LHRS-RHRS
Scaler 4 - Gate
Scaler 5 - Gate
Scaler 1 - Gate
Scaler 3 – Ch1
Sync/Gate/FB/MID
Sync/Gate/FB/TOP
in
out
From LeCroy 4616 Rack 3 Bot Crate – Ch 5
From LeCroy 4616 Rack 3 Bot Crate – Ch 3
From LeCroy 4616 Rack 3 Bot Crate – Ch 4
Busy from LHRS
RHRS
LeCroy 4616 (Left) & FIFO
(Rack 3, Bot Crate)
April 18, 2017


RHRS
LeCroy 4616 (Right) & NIM-ECL
(Rack 3, Bot Crate)
April 18, 2017
LeCroy 4616
(Rack 3 Bot Crate Right)
Downstairs
?
LeCroy
4616
?
TOP FB TDC
MID FB TDC
BOT FB ADC
?
Going
Downstairs
From TS (output 3)
From TM (TDC Gate)
FIFO Rack 3 Bot Crate Module 7
FIFO Rack 3 Bot Crate Module 8
Logic Unit
Logic Unit
Dual Gate
Generator
Dual Gate
Generator
FIFO Rack 3
Bot Crate
Module 7
Logic Unit
(just making
copies)
Discriminator
NIM – ECL
Converter
S0 & S2
S0 & GC
S2 & GC
S0 & SH
S2 & SH
GC & SH
EDTM
CLOCK
From LeCroy 4616 Rack 3 Top Crate (BCM 3)
[EMPTY]
[TERMINATED]
[TERMINATED]
[TERMINATED]
RT
[EMPTY]
[EMPTY]
[EMPTY]
To TS




Dual Gate Grator
start
busy
stop
OR
NIM
NIM
in
out
BLANK
TTL
DEL
start
busy
stop
OR
NIM
NIM
in
out
BLANK
TTL
DEL


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16


A
coinc. level
out
B
C
veto
out
D
out
A
coinc. level
out
B
C
veto
out
D
out
A
coinc. level
out
B
C
veto
out
D
out
A
coinc. level
out
B
C
veto
out
D
out