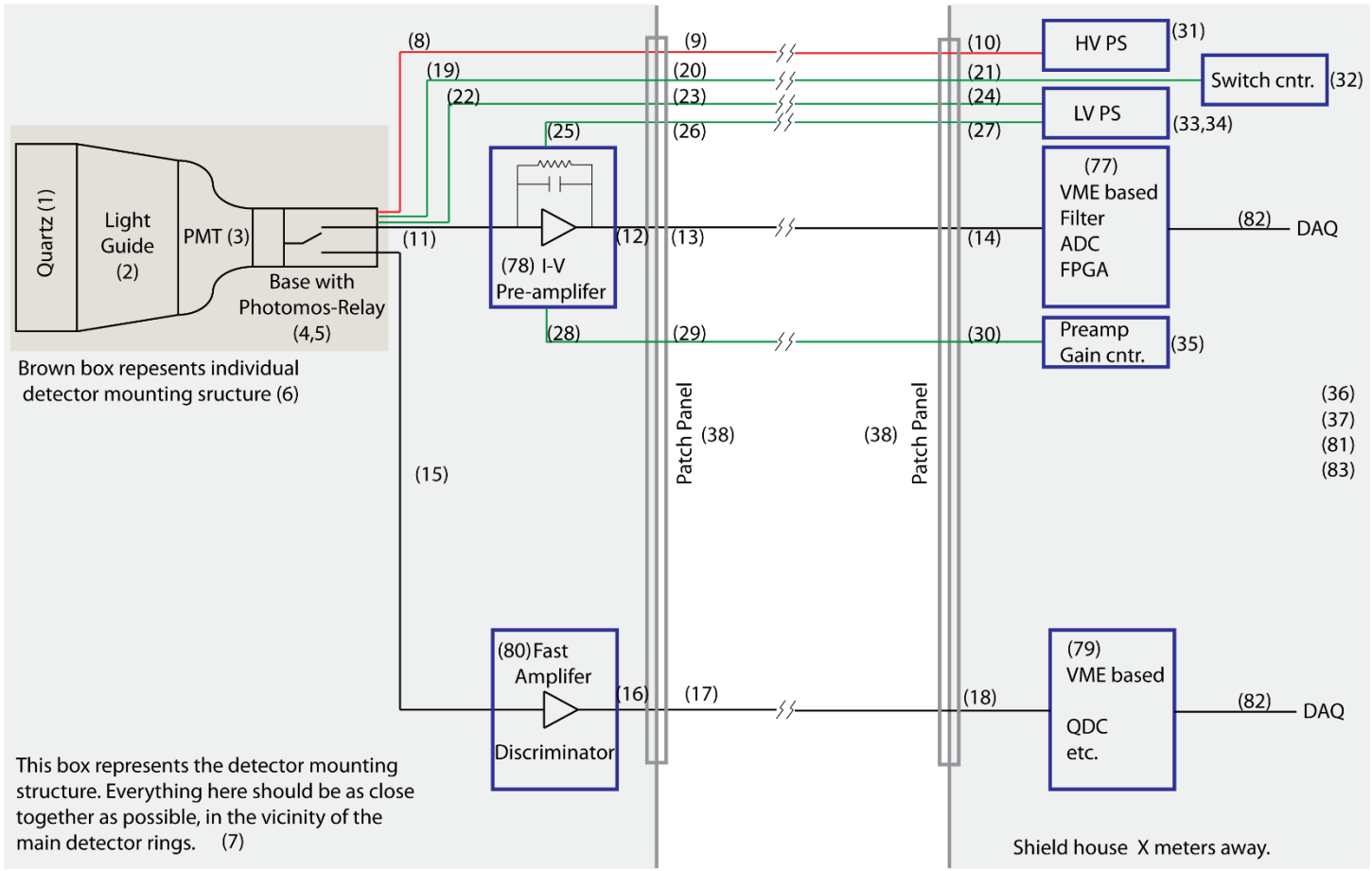
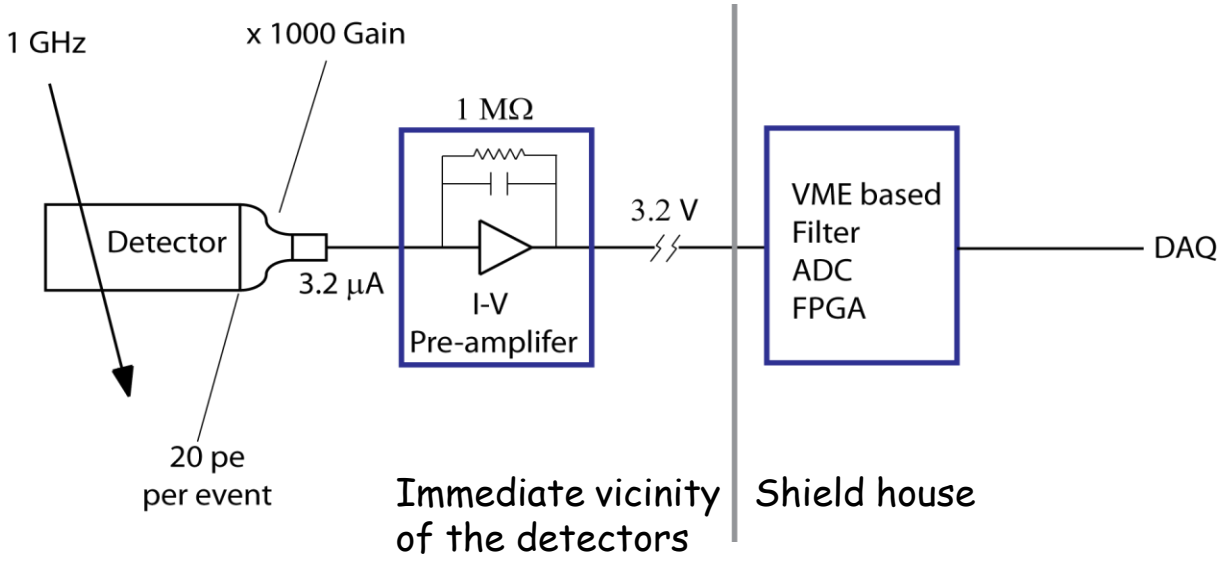
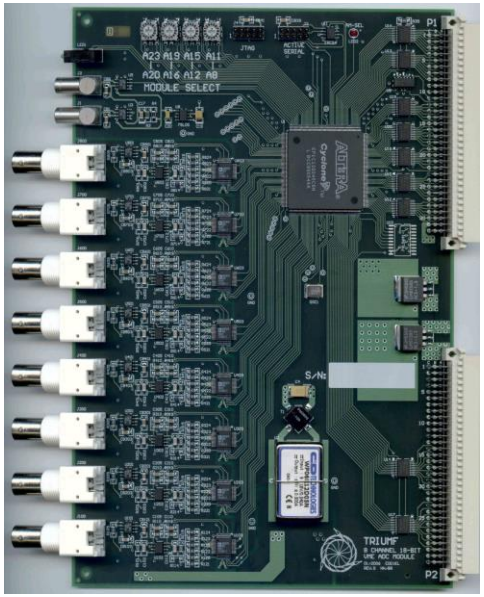
Integrating Electronics Re-Design
Initial Discussion

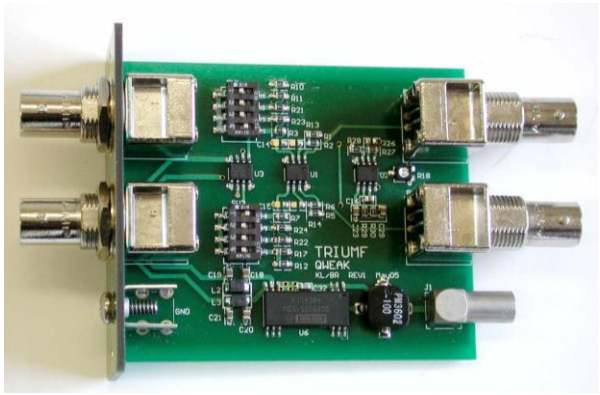
Integrating Detector Work Package Diagram



Integrating Electronics Re-Design
Initial Discussion







These two components correspond to the items for which TRIUMF support is requested.

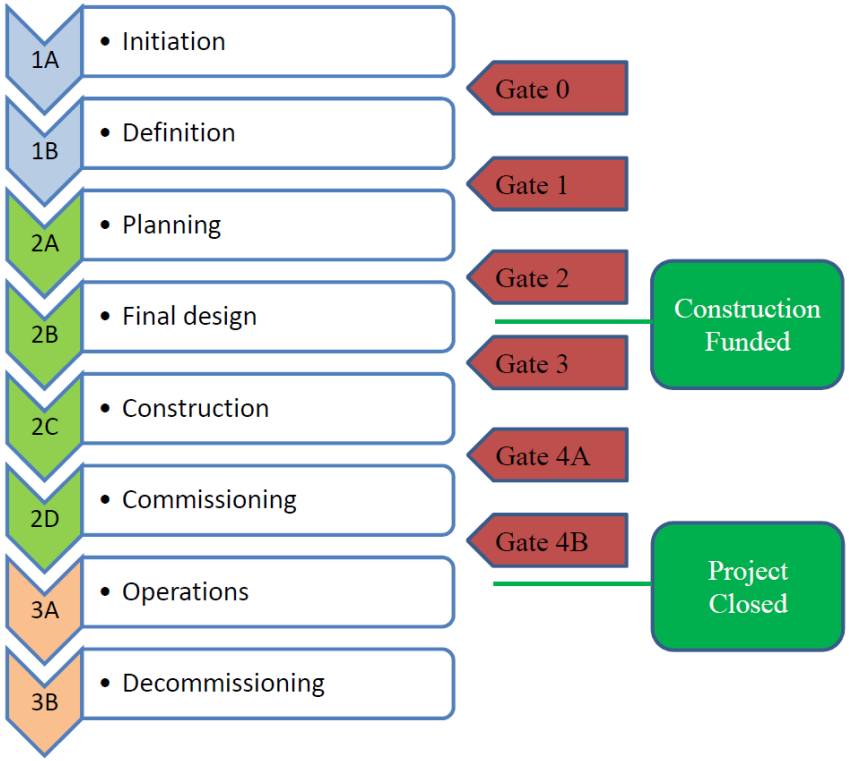
Integrating Electronics Re-Design
Initial Discussion

Project status at TRIUMF:

- Gate 0 (done March 2016)
- Gate 1 (done July 2016)
- Gate 2 (sometime this Fall ? …)

Gate 2 review documents:

- Initial technical design
- Detailed initial project plan
- Resource loaded schedule (WBS) for two scenarios (w/wo CFI)
- Specify requirements (for TRIUMF) for commissioning and operation
- Specify future FW support needs



Integrating Electronics Re-Design Initial Discussion

Stage	Phase	Phase UID	Table Process	Phase Description	Key Deliverable	TSOP
Pre-Project Stage	Initiation	1A	Table 5.1 1-3	Initiate Project	Project Initiation Sheet.	
	Definition	1B	Table 5.2 2,3	Define Project	Conceptual Design.	TSOP-01
Project Stage	Planning	2A	Table 5.2 4,5	Develop design and project plan	Initial technical design. Initial project plan with WBS & schedule.	TSOP-01 TSOP-06
	Final Design	2B	Table 5.3 2,3	Complete design and project plan	Final technical design. Final project plan with WBS & schedule.	TSOP-01 TSOP-06
	Construction	2C	Table 5.3 4,5	Construct the device or facility	As built drawings. Commissioning plan.	TSOP-01 TSOP-06 TSOP-13
	Commissioning	2D	Table 5.3 6,7	Commission the device or facility	Commissioning Report. Operating procedures.	TSOP-01 TSOP-04 TSOP-12 TSOP-13
Post Project Stage	Operating	3A		Operate the device or facility	Science, beam or other output.	TSOP-01 TSOP-04 TSOP-11 TSOP-12
	Decommissioning	3B		Decommission the device or facility	Decommissioning Report.	TSOP-01

Integrating Electronics Re-Design
Initial Discussion

Information presented to TRIUMF for Gate 1 (DocDB 214-v1):

- Explanation of existing QWeak modules
- MOLLER experimental setup and measurement technique
- Desired changes for MOLLER module:
  - Higher bandwidth (~500 kHz)
  - Higher sampling rate (≥ 2 Msps)
  - ADC resolution (same at 18 bit)
  - High ADC linearity
  - Small signal delay
  - FPGA capability:
    - Read out additional information (RMS, min, max, etc.)
    - Block readout phase shift
    - "Waveform Digitization"
    - Accumulation start-stop times readout
  - Improve data readout speed (crate format, protocol, etc.)

Integrating Electronics Re-Design
Initial Discussion

TRIUMF Gate 1 review questions / results:

- We have a TRIUMF team:
  - Fabrice Retiere (contact and project manager)
  - Daryl Bishop (lead engineer)
  - Additional (Leonid Kuchaninov, Doug Bryman)

- Requires a full work breakdown structure (WBS) and resource estimate
- Requires project management
- Specific technical questions/suggestions that came up:
  - Do we need BNC format at input
  - FPGA supported data preformatting or direct streaming of ADC data
  - Move away from readout via VME bus – use gigabit Ethernet
  - If FPGA is used, do we require frequent changes of FW – can we do it ourselves?
  - Suggesting new 18 bit, 15 Msps ADC – facilitates some form of waveform digitization if quartz detectors are slow …
  - Full or semi differential signal

Integrating Electronics Re-Design
Initial Discussion

My questions / assessment of the situation:

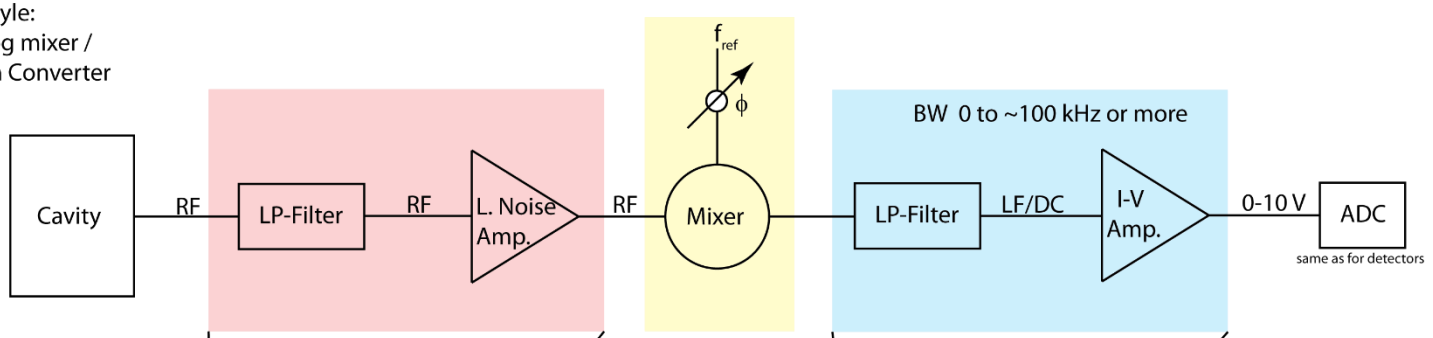
- TRIUMF is committed to the electronics development (with or without the CFI success)
- Engineers seem to strongly prefer to move away from VME bus readout
- We can easily go to higher sampling rate and keep or increase resolution without technical drawbacks
- Does streaming readout and/or gigabit Ethernet work with CODA ; is it too much data to handle during online analysis ?
- We have to develop an initial design or determine specific design changes in the next few months …
- I think we would want to implement the possibility to install new FPGA firmware ourselves … early training for expertise should happen at TRIUMF and if CFI successful hire technician to support this at Jlab.

Integrating Electronics Re-Design
Initial Discussion

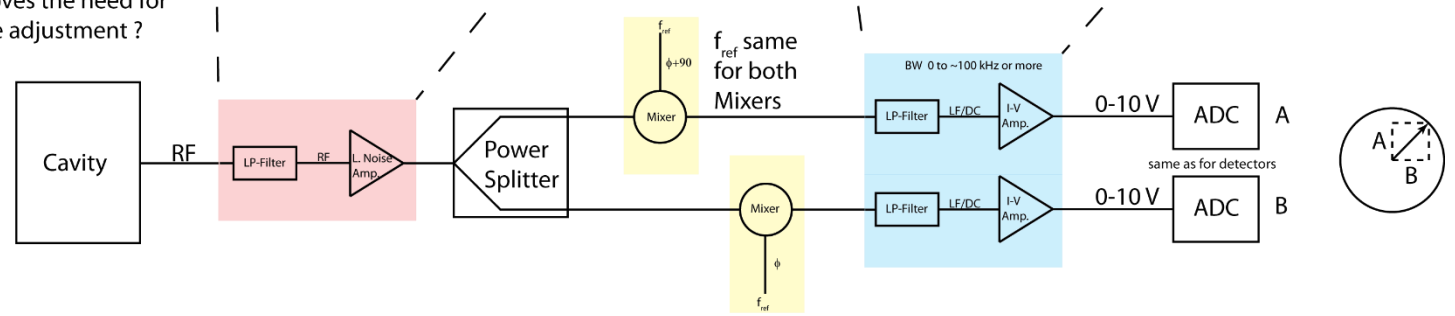
Some of the slides presented at the Gate 1 review are attached after this …

Aside: Beam Monitor Signal Chain (options)

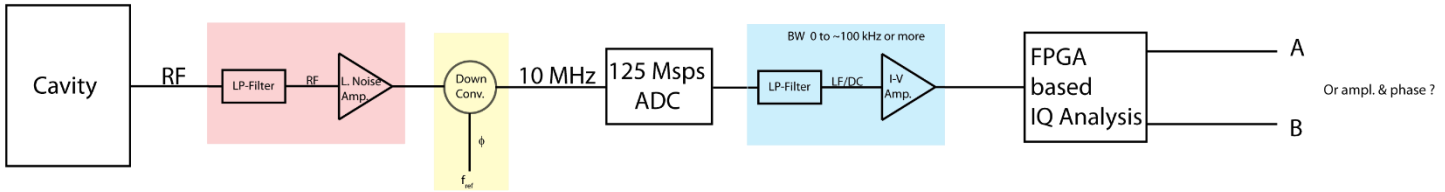
1) Old style:
Analog mixer /
Down Converter



2) New IQ style:
Removes the need for
phase adjustment ?



3) New IQ style - Digitized:
Removes possible pathologies
from having to use two separate
ADC channels.



Signal Levels at the ADC Input

Example Detector Signal:

$$G_{PMT} = 400 \qquad G_{AMP} = 0.5\ M\Omega \qquad R_e = 5\ GHz$$

$$N_{pe} \approx 40 \quad \Rightarrow \quad q_{cath} \approx 64 \times 10^{-19}\ C\ /\ track$$

$$i_C = 1.6 R_e N_{pe} \times 10^{-10}\ nA \simeq 32\ nA$$

$$i_A = i_C G_{PMT} \simeq 13\ \mu A$$

$$S = i_A G_{AMP} = 6.5\ V$$

at the ADC input

$$B = 500\ kHz$$

equivalent noise bandwidth

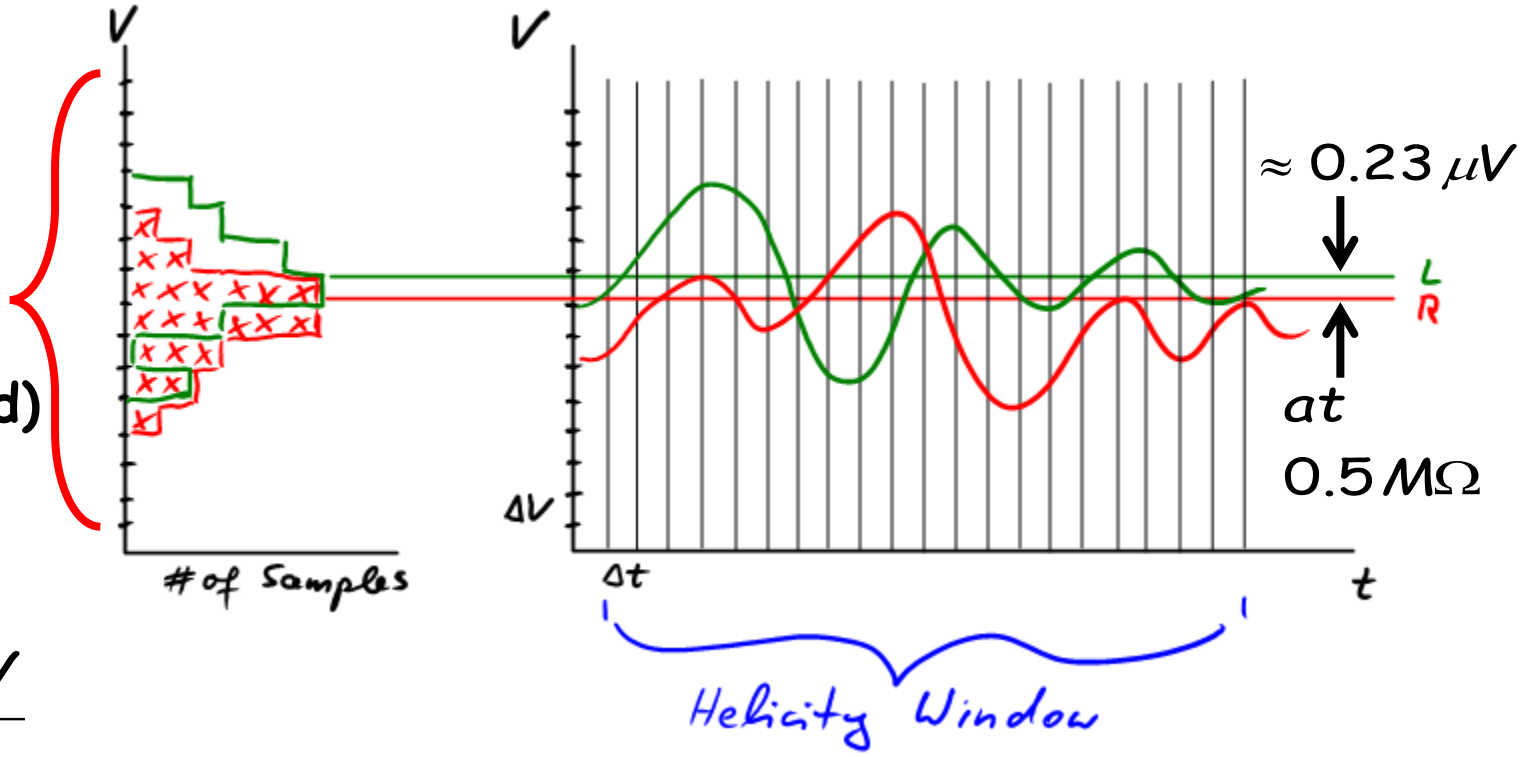
$$\sigma_{Shot} = \sqrt{2 q_{cath} G_{PMT}\, i_A} \cdot \sqrt{B} \approx 180\ nA \quad \Rightarrow \quad \approx 90\ mV$$

Noise is usually 15-30% higher due to dynode gain fluctuations.

Signal Levels at the ADC Input

Digitization:

ADC range and resolution (0 suppressed)



18 bit Resolution:

$$\Delta V = \frac{10V}{2^{17}}$$

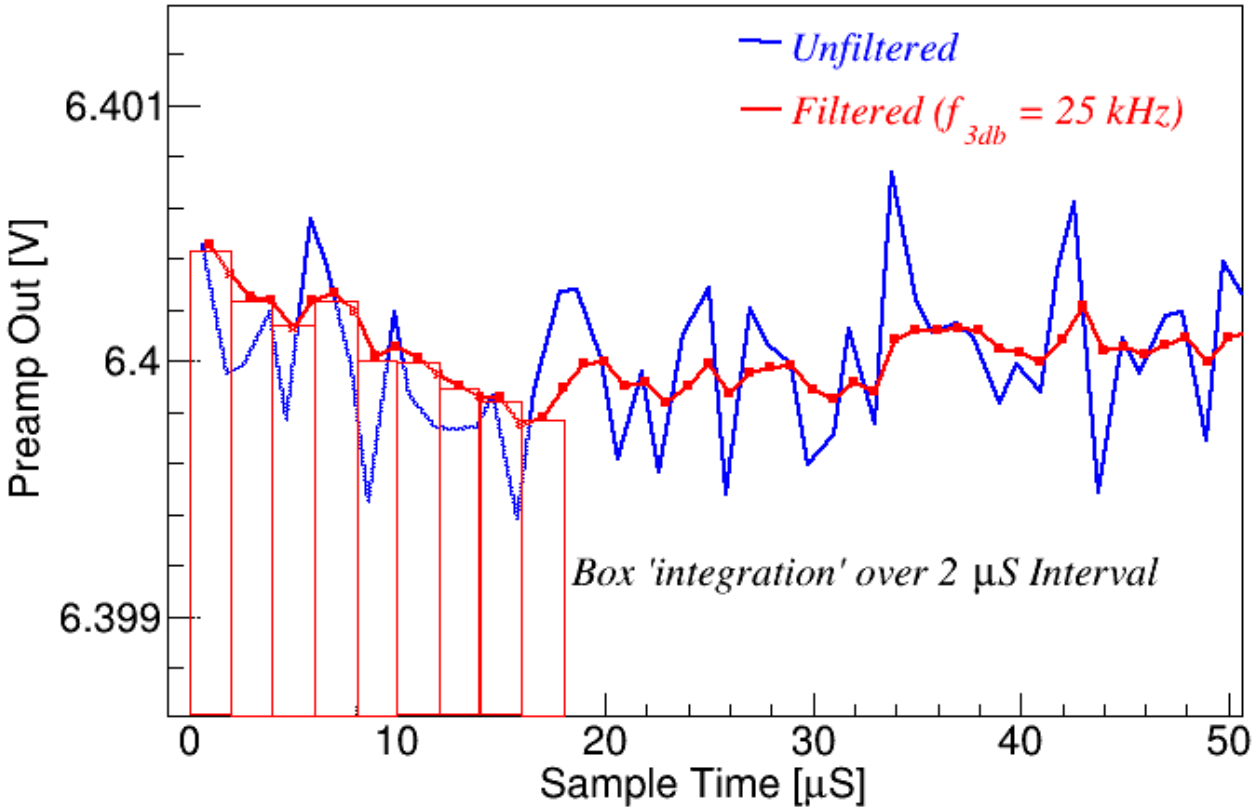
$$\approx 76\mu V$$

➡ **Signal RMS is spread over ~1200 ADC channels**

ADC Integration Scheme

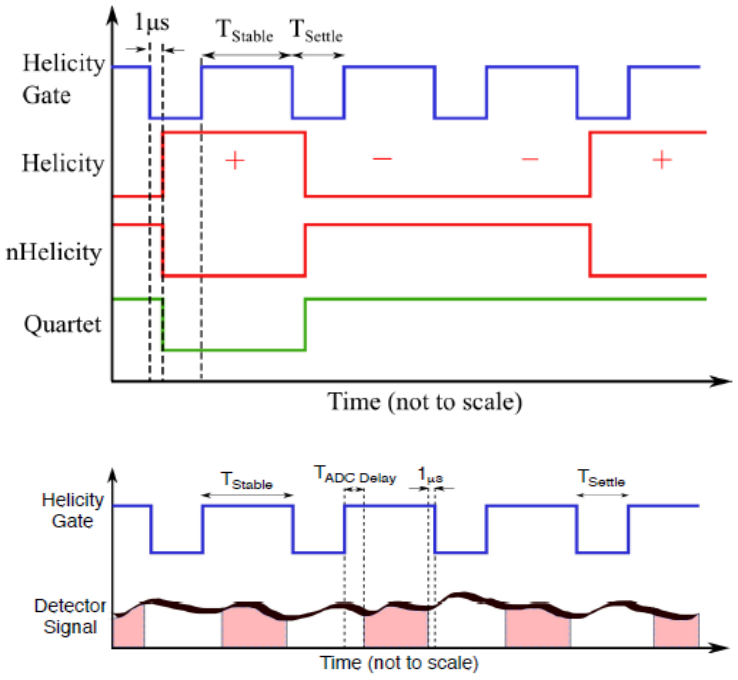
QWeak ADC integration scheme:

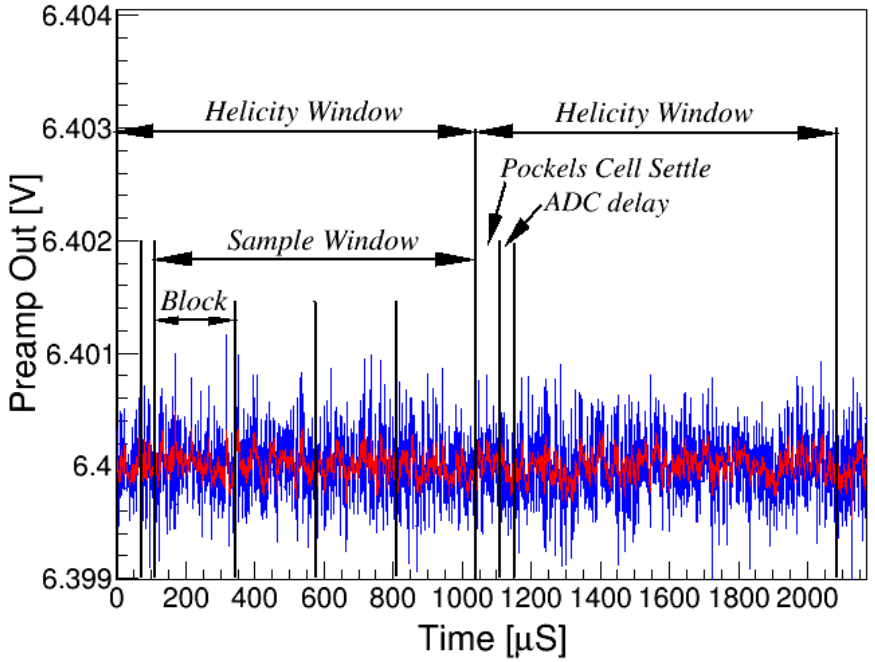
- **at highest rate samples every 2 μs**
- **filtering should be consistent with sampling rate, bit noise, and ADC non-linearity**
- **higher helicity reversal would mean smaller number of samples per window**
- **unless we increase the sampling rate**



ADC Integration Scheme

- Detector yields are integrated (summed) over each helicity state
- Raw asymmetries are formed from differences between positive and negative helicity states within a quartet
- Quartet asymmetries are histogrammed





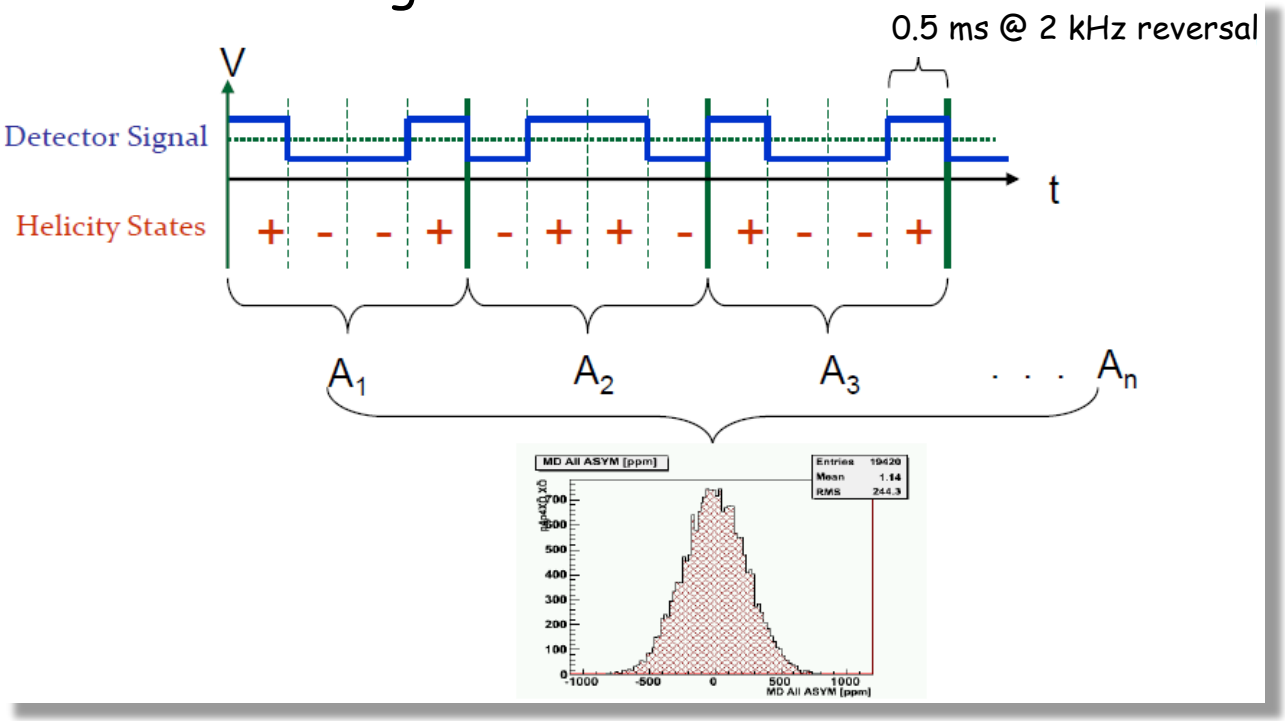
Asymmetry Formation

- Detector yields are integrated (summed) over each helicity state
- Normalize detector signal by beam current

$$Y = \frac{S_{det}}{S_{mon}}$$

- Raw asymmetries are formed from differences between positive and negative helicity states within a quartet
- Quartet asymmetries are histogrammed

$$A_{msr} = \frac{\sum_{+} Y_{+} - \sum_{-} Y_{-}}{\sum_{+} Y_{+} + \sum_{-} Y_{-}}$$



Signal Levels in the Data Stream

The helicity integration scheme is effectively another filter:

$$G_{PMT} = 400 \qquad G_{AMP} = 0.5\ M\Omega \qquad R_e = 5\ GHz$$

$$N_{pe} \approx 40 \quad \Rightarrow \quad q_{cath} = 64 \times 10^{-19}\ C\ /\ track$$

$$i_A = 1.6 R_e N_{pe} G_{PMT} \times 10^{-10}\ nA = 13\ \mu A$$

$$B = \frac{1}{2} \cdot 2000\ Hz \quad \textbf{equivalent noise bandwidth}$$

$$\sigma_{Shot} = \sqrt{2 q_{cath} G_{PMT} i_A} \cdot \sqrt{B} \approx 8\ nA \ \Rightarrow \approx 4\ mV$$

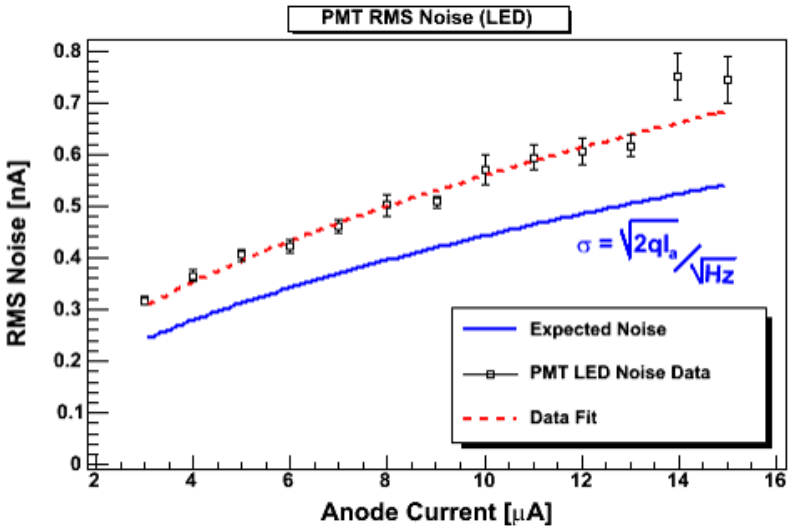
Note that: $\dfrac{1}{\sqrt{N}} = \sqrt{\dfrac{2000\ Hz}{R_e}} \approx 632\ ppm$

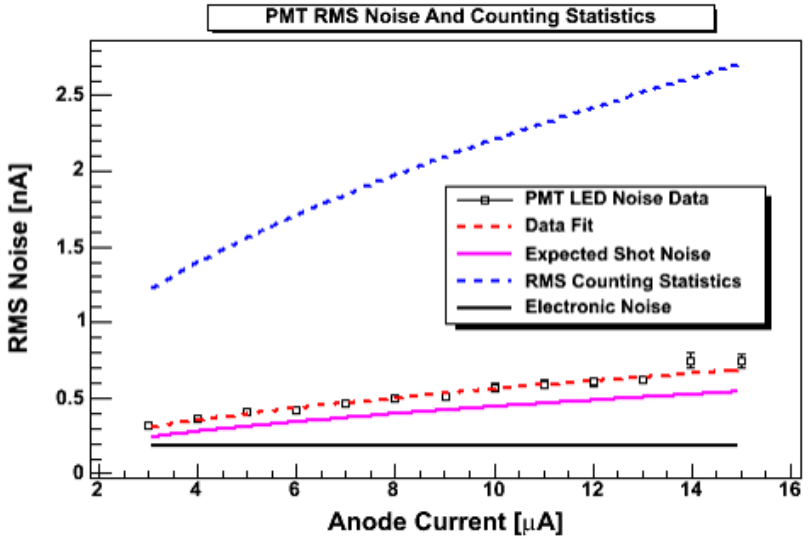
and $\dfrac{\sigma_{Shot}}{i_A} = \dfrac{0.008\ \mu A}{13\ \mu A} \approx 615\ ppm$

Uncertainties

Electronic noise needs to be small compared to the RMS noise in the yield, so that it gets averaged away quickely

Some single photo-electron bench test examples from Qweak:



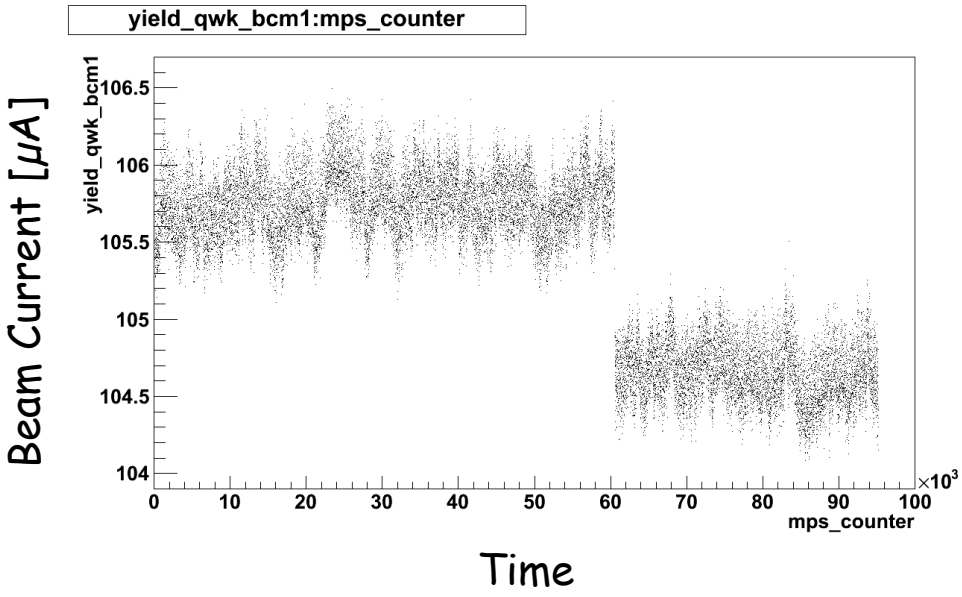


Uncertainties

Due to changes in the beam conditions, the detector signal must be normalized to the beam current monitors

Linear regression is used to correct for beam position, angle and energy

- Measure beam current using beam monitors all along the beam line upstream of the target



- Normalized detector signal $y = \frac{S_{det}}{S_{mon}}$

Uncertainties

The faster the helicity reversal the better the approximation of the signal as a linear drift for many experimental effects.

Lots of large scale slow drifts present in the experiment

Locally the signal "looks like" a linear function of time:

$$y_{\pm}(t) \approx \left(a + \left.\frac{dy}{dt}\right|_{t_i} t \right)\left(1 + A_{msr}\right)$$

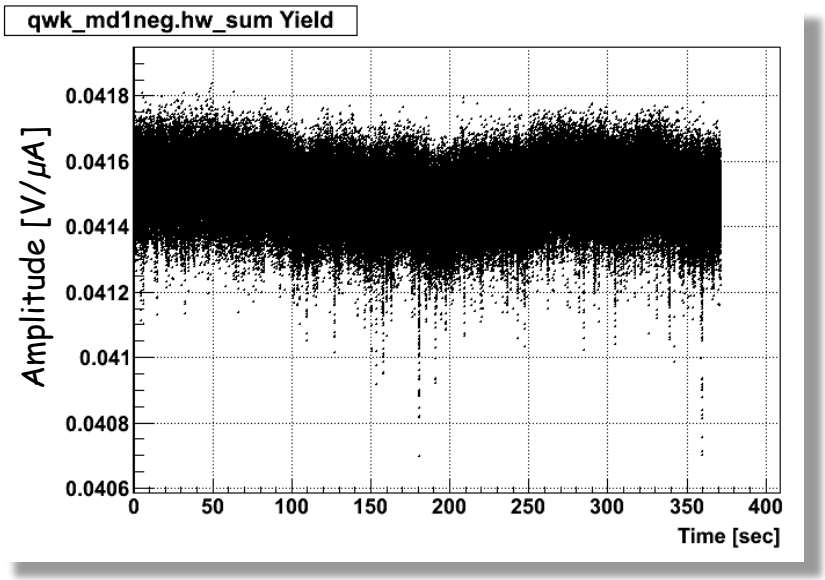
The quartet helicity pattern removes linear drifts:

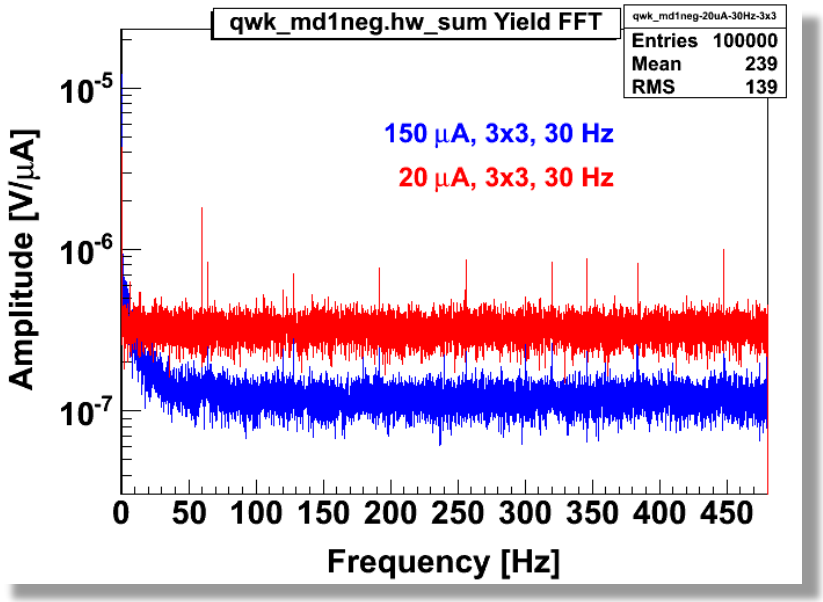
$$A_{msr} = \frac{\sum_{+} y_{+} - \sum_{-} y_{-}}{\sum_{+} y_{+} + \sum_{-} y_{-}}$$

Uncertainties

Target boiling:

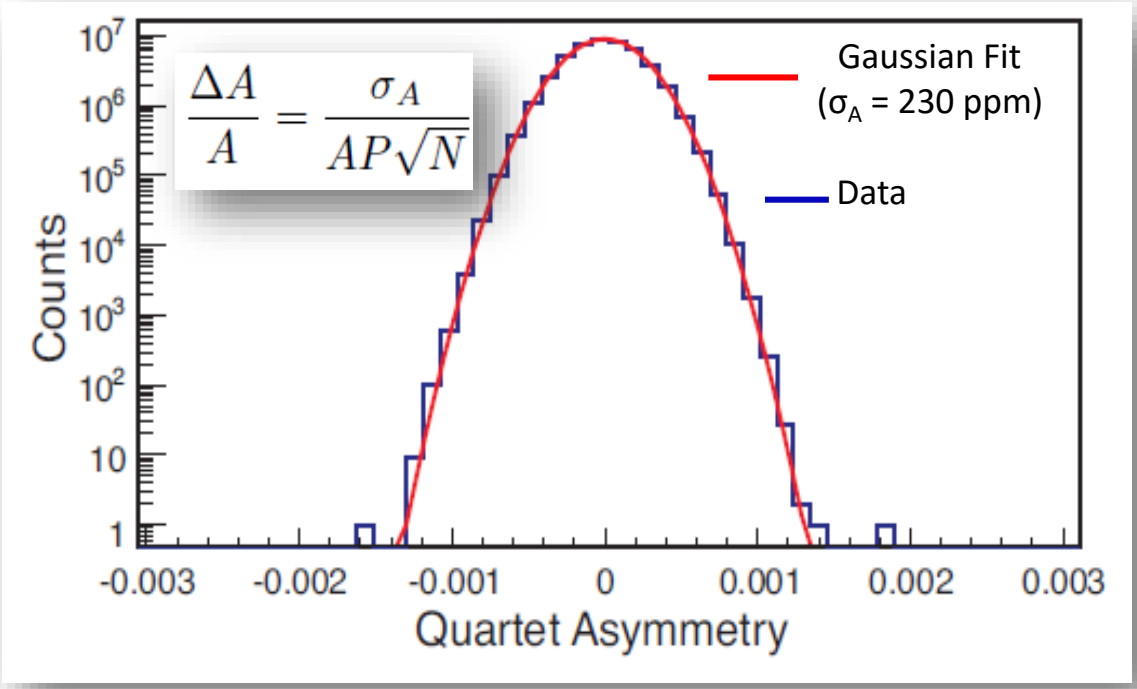
- With high beam power target boiling is inevitable
- Starts around 100 μA
- But this has a 1/f frequency dependence which dominates at low frequency
- Fast helicity reversal reduces this effect.





Measurement Methodology and Uncertainties

Histogram of asymmetries formed from quartets:



Typical observed RMS width in main detector yield: ~ 240 ppm

Pure counting statistics:	≈	200 ppm
Detector Resolution:	+	90 ppm
Current monitor resolution	+	50 ppm
Target boiling	+	57 ppm
Total	≈	233 ppm ≈ observed

Qweak example!

Numbers will be smaller for MOLLER …

Uncertainties and Electronics Design Choices

- Higher frequency helicity reversal leads to more data (higher statistics)
- Higher frequency helicity reversal reduces systematic effects
- Higher frequency helicity reversal requires a higher ADC sampling rate
- Higher frequency helicity reversal requires a shorter Pockels cell transition
- Electronics must see helicity transition, requiring higher sampling rate and larger bandwidth

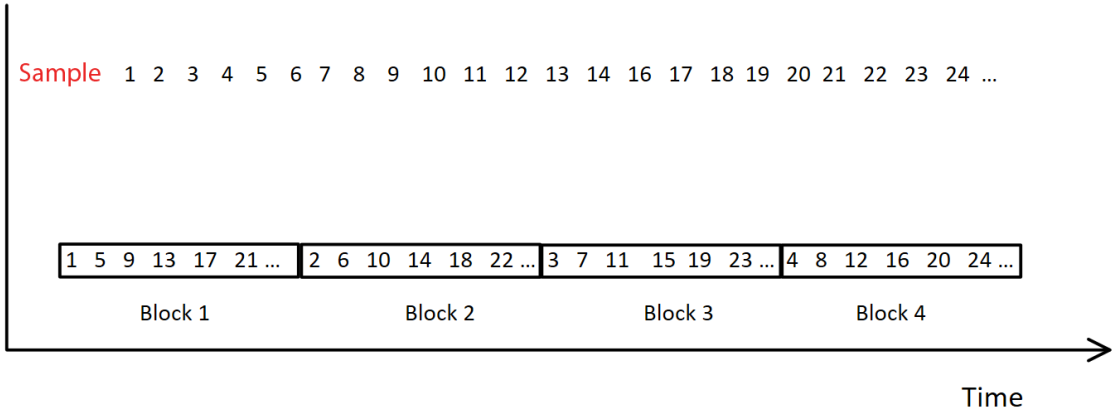
  - Goal transition time: $t_{set} = 10\,\mu s$
  - Settle to 0.01% of final value corresponds to 9 time constants or a 1.1 μs time constant
  - Minimum bandwidth is then $f_{3db} = 0.35 / \left(2.2 \times 1.1\ \mu S\right) \simeq 150\,kHz$
  - The noise equivalent bandwidth is $\frac{\pi}{2} f_{3db} \simeq 240\,kHz$ → $B = 500\,kHz$

- Helicity correlated and uncorrelated changes in beam position, angle, energy and current require the detector signal to be normalized to the beam monitors, so the beam monitors must be read out with the same electronics, at the same sampling rate. RF down-conversion and monitor analysis is practical down to certain bandwidths – so we need to accommodate those bandwidths.

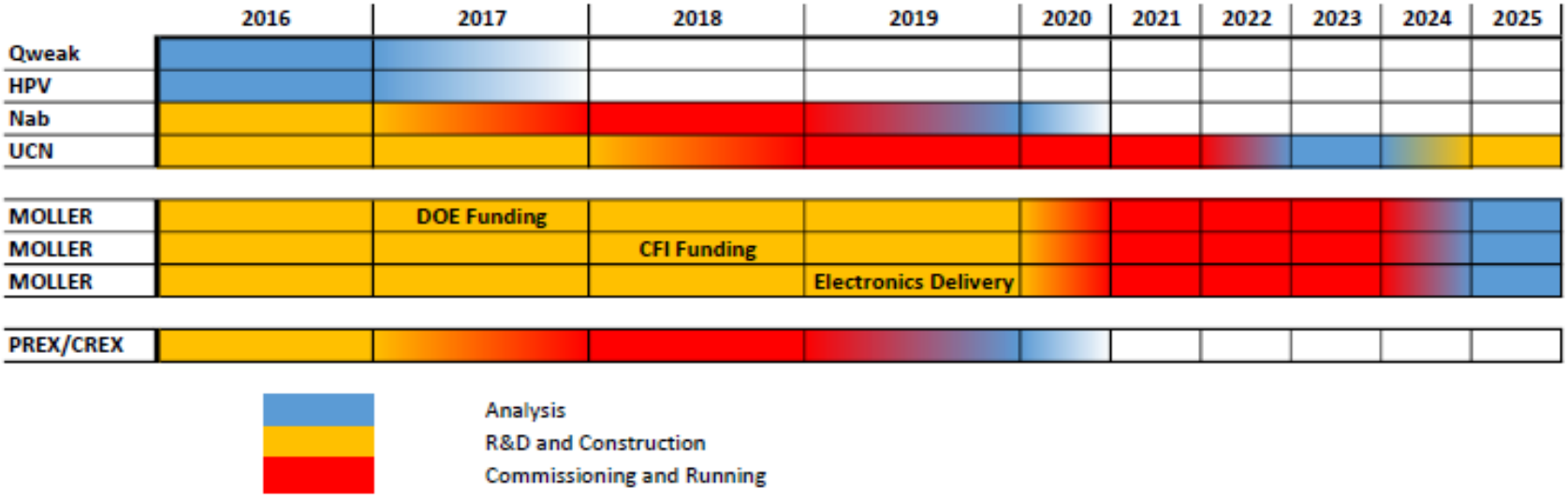
Uncertainties and Electronics Design Choices

- Higher frequency helicity reversal requires higher ADC sampling rate
  - Helicity window at 2 kHz reversal : $\Delta t = 500\,\mu s$
  - Subtract Pockels cell settle and electronics delays : $\Delta t = 460\,\mu s$ (?)
  - Divide window into 4 blocks to do systematic analysis : $\Delta t_B = 115\,\mu s$
  - To get a reasonable number of samples per block take a sample every μs

    ≥ 1 *Msps*
  - Already more or less dictated by Pockels cell settle anyway.



Eletronics WBS, Timeline, Manpower & Resources

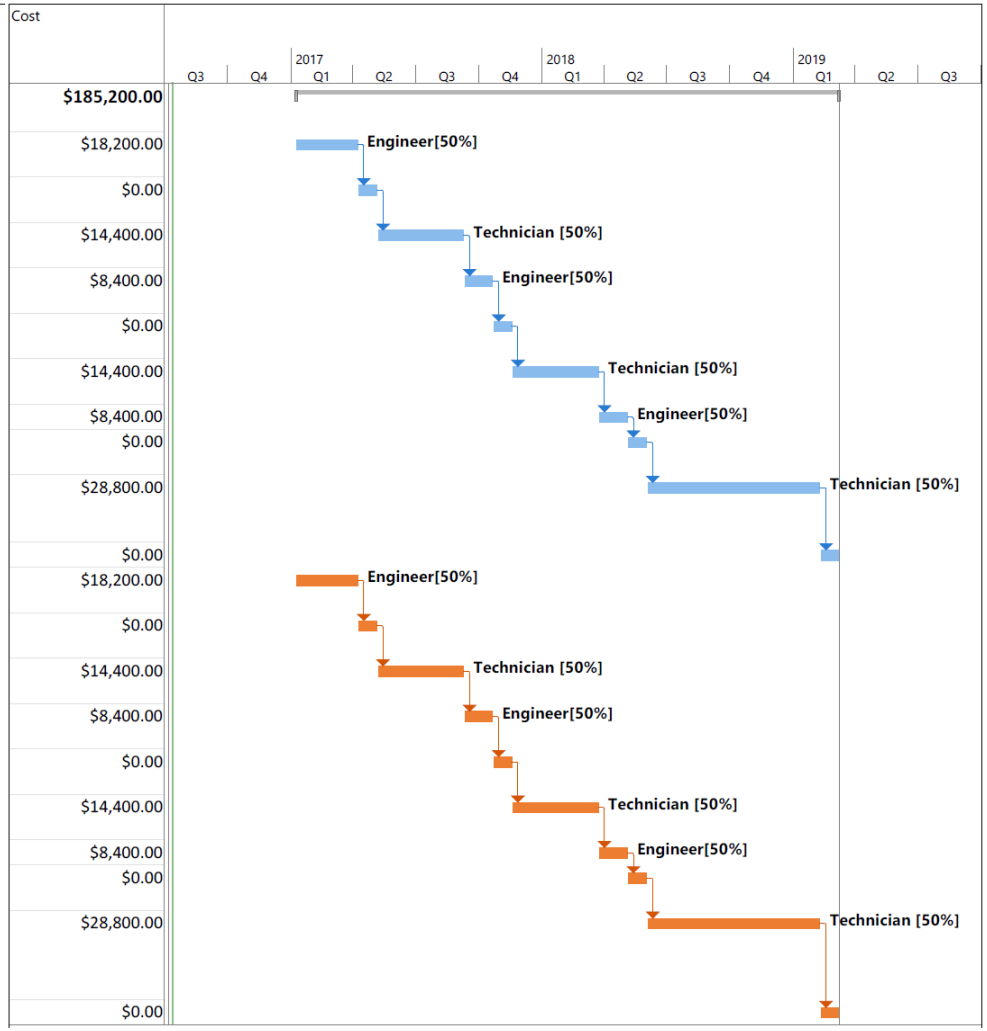


Total CFI project consists of part of integrating detector package and associated integrating electronics for the detectors and the beam monitors.

Only resources associated with electronics development are requested from TRIUMF.

Eletronics WBS, Timeline, Manpower & Resources

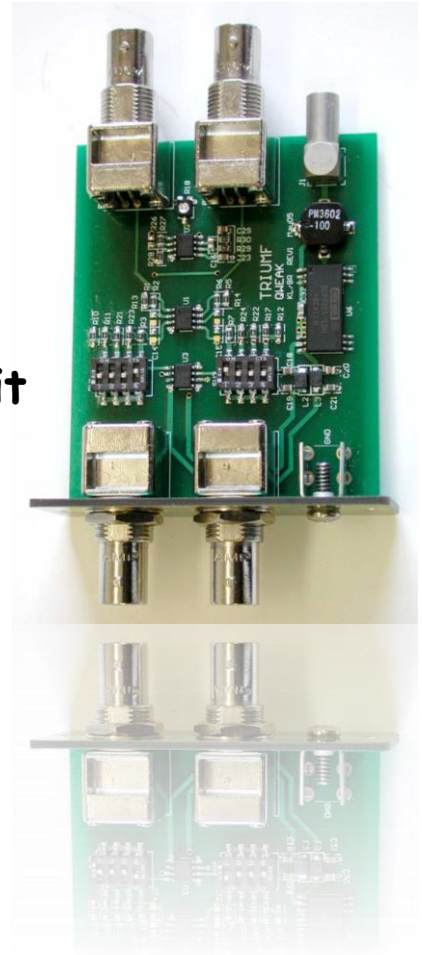
ID	Task Mode	Task Name	Duration	Start	Finish	Pr	Resource Names	Regular Work	Cost
0		**MOLLER Integrating**	**565 days?**	**Mon 17-01-09**	**Fri 19-03-08**			**3,880 hrs**	**$185,200.00**
1		Preamp prototype development	65 days	Mon 17-01-09	Fri 17-04-07		Engineer[50%]	260 hrs	$18,200.00
2		Preamp Prototype Procurement	20 days	Mon 17-04-10	Fri 17-05-05	1		0 hrs	$0.00
3		Preamp assembly & testing	90 days	Mon 17-05-08	Fri 17-09-08	2	Technician [50%]	360 hrs	$14,400.00
4		Preamp Design Changes	30 days	Mon 17-09-11	Fri 17-10-20	3	Engineer[50%]	120 hrs	$8,400.00
5		Preamp Prototype 2 procurement	20 days	Mon 17-10-23	Fri 17-11-17	4		0 hrs	$0.00
6		Preamp prototype 2 assembly and	90 days	Mon 17-11-20	Fri 18-03-23	5	Technician [50%]	360 hrs	$14,400.00
7		Preamp final design	30 days	Mon 18-03-2	Fri 18-05-04	6	Engineer[50%]	120 hrs	$8,400.00
8		Preamp parts procurement	20 days	Mon 18-05-07	Fri 18-06-01	7		0 hrs	$0.00
9		Preamp final assembly of all channels and QA	180 days	Mon 18-06-04	Fri 19-02-08	8	Technician [50%]	720 hrs	$28,800.00
10		Preamp delivery	20 days	Mon 19-02-1	Fri 19-03-08	9		0 hrs	$0.00
11		ADC board prototype	65 days	Mon 17-01-09	Fri 17-04-07		Engineer[50%]	260 hrs	$18,200.00
12		ADC board prototype	20 days	Mon 17-04-10	Fri 17-05-05	11		0 hrs	$0.00
13		ADC board assembly & testing	90 days	Mon 17-05-08	Fri 17-09-08	12	Technician [50%]	360 hrs	$14,400.00
14		ADC board design changes	30 days?	Mon 17-09-11	Fri 17-10-20	13	Engineer[50%]	120 hrs	$8,400.00
15		ADC board prototype 2	20 days	Mon 17-10-23	Fri 17-11-17	14		0 hrs	$0.00
16		ADC board prototype 2	90 days	Mon 17-11-20	Fri 18-03-23	15	Technician [50%]	360 hrs	$14,400.00
17		ADC board final de	30 days	Mon 18-03-2	Fri 18-05-04	16	Engineer[50%]	120 hrs	$8,400.00
18		ADC board parts procurement	20 days	Mon 18-05-07	Fri 18-06-01	17		0 hrs	$0.00
19		ADC board final assembly of all channels and QA testing	180 days	Mon 18-06-04	Fri 19-02-08	18	Technician [50%]	720 hrs	$28,800.00
20		ADC board delivery	20 days	Mon 19-02-1	Fri 19-03-08	19		0 hrs	$0.00



Hardware

Preamplifer

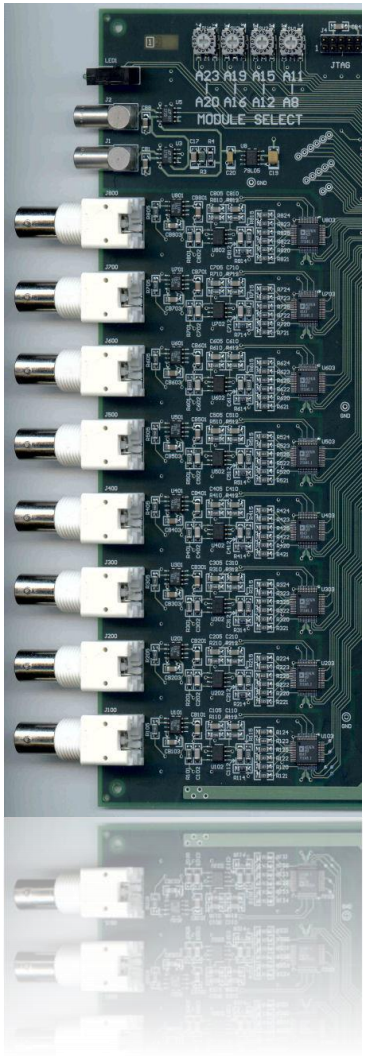
- **Gain: V_{out} / V_{in} = 0.5, 1, 2, 4 MW switch selectable**
- **Output ±10 V. Adjustable ±2 V offset**
- **Input: current limit set by gain and 10 volt output limit**
- **Power: +5 VDC on Lemo connector**
- **Bandwidth: f3db = 26 kHz**
- **Noise: 0.5 mV/√(Hz) referred to output with 1MΩ gain setting (Amplifier noise specification assumes the input capacitance of 5 m of RG-62.)**



Hardware

TRIUMF VME Integrating ADC

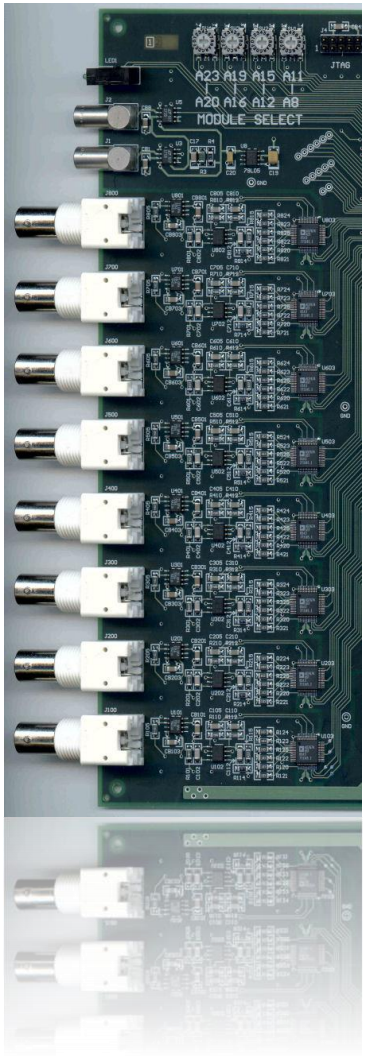
- **Trigger: external NIM signal or internal trigger**
- **Integration time: selected as a number of samples, up to 1/30 second**
- **Sample rate: selectable up to 500 ksps. 18-bit ADCs.**
- **Clock: internal 20 MHz or external NIM selectable.**
- **Input: ±10 volts. High impedance differential.**
- **Output: 32 bit sum**
- **The integration period may be sub-divided into up to four blocks. Buffering - no dead time.**
- **Uses FPGA for ADC data handling**



Hardware

TRIUMF VME Integrating ADC

- **50 kHz, 5-pole anti-aliasing filter**
- **Full differential input provides common mode noise rejection**
- **Buffered output permits reading previous integral during integration**
- **Eight integrators per single width VME**
- **The 18 bit ADCs have ~0.5 LSB RMS noise per sample**



VME registers
- ExternalClock prescale/sample clock generator
- Number of Samples/gate
- Gate Source (test mode)
- Gate Length (test mode)
- Gate Delay (in external clock ticks)

Data Readout
- Channel number/identifier
- 32-bit sums
- subsample 1-4
- valid data flag

Sampling and Integration in the Time Domain

Competing Bandwidth Considerations:

Favoring Large Bandwidth :

- **provides ADC sample distribution large enough to average out the bit noise**

- **allows the sampling to follow the signal during helicity state transitions**

- **Since the asymmetry is much smaller than the ADC resolution, filtering away the "high" frequency components leads to random loss of helicity information.**

- **If the helicity reversal rate goes up, then the analog bandwidth has to go up as well: need a large enough spread to determine the helicity variation for each window**

Sampling and Integration in the Time Domain

Competing Bandwidth Considerations:

Why filter at all ?

Favoring "Smaller" Bandwidth :

- the analog bandwidth one can handle is limited by the maximum sampling rate in the module
  - Satisfying the Nyquist rule up to the frequencies we care about means increasing the sampling rate if the bandwidth goes up
- large bandwidths pick up high frequency, large amplitude signals and increase the data RMS and/or introduce systematic effects (non-Gaussian)

Sampling and Integration in the Time Domain

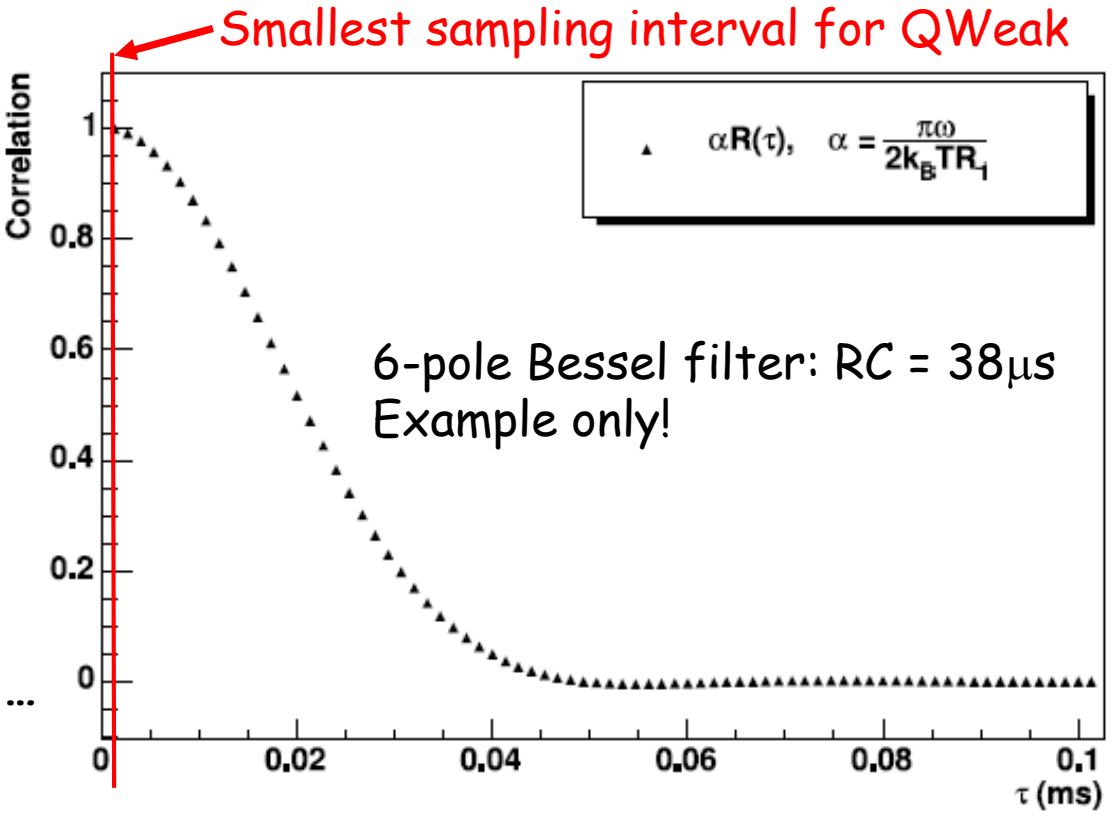
Low bandwidth and oversampling leads to high correlation between samples …

But we don't care:

In the end we get a single yield for each helicity window which is uncorrelated with neighboring helicity measurements.

But we get to use this to deal with ADC systematics …

Statistical precision goes as $\frac{1}{\sqrt{N}}$ **for N helicity windows.**



$$\mathcal{R}_{I_J}(\tau) = \int_0^\infty |\mathcal{H}(i\omega)|^2 \; \mathcal{S}_{V_J}(f) \; e^{2\pi i f \tau} \; df = K_o \int_0^\infty \frac{4\mathrm{k_B} T R_1 \; e^{2\pi i f \tau} \; df}{|B_6(i2\pi f)|^2}$$