Super BigBite DAQ & Trigger

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Hall A Collaboration Meeting

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SBS DAQ Requirements

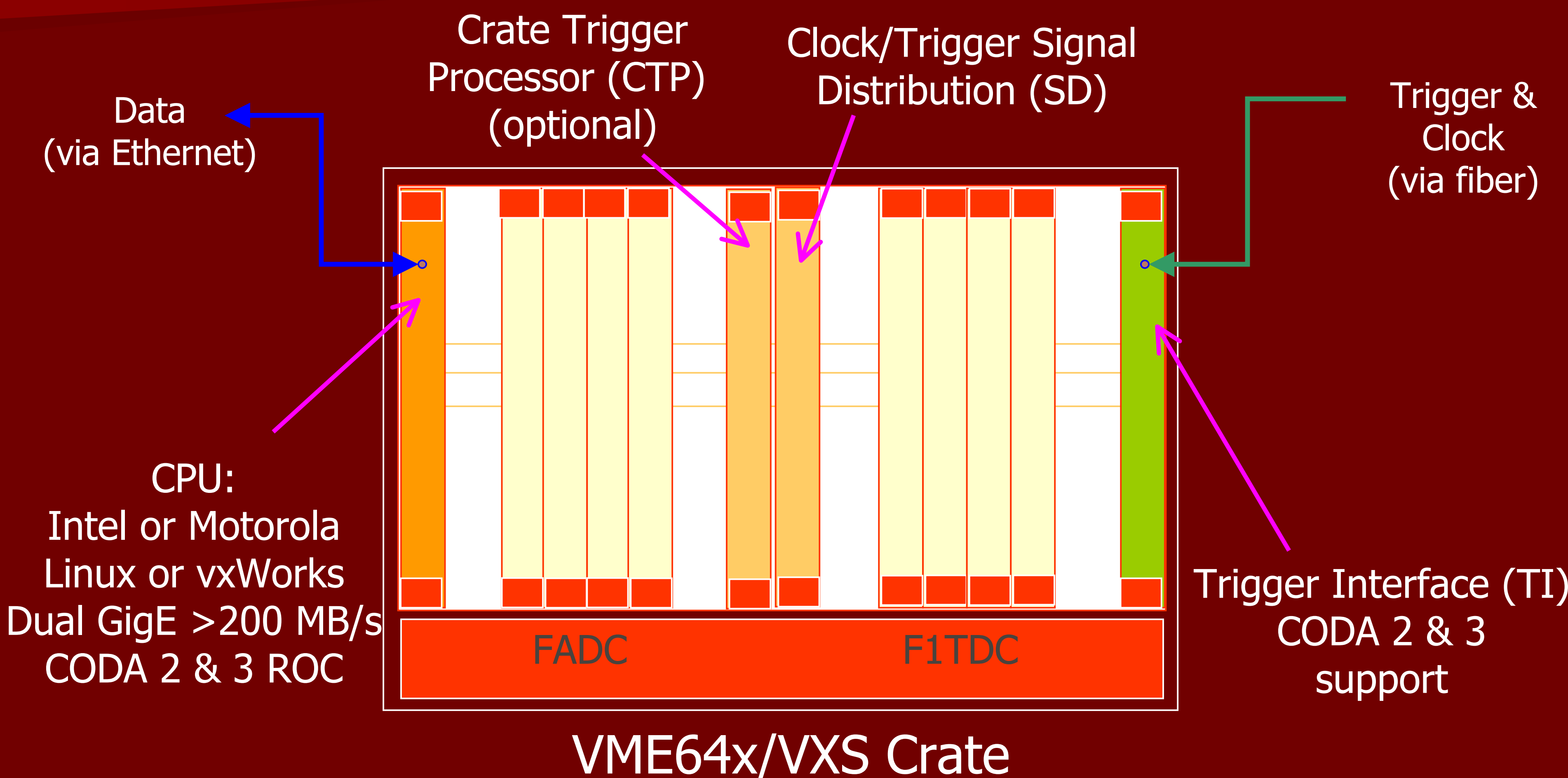
- Data rate driven by GEMs & Coordinate Detector
  - ≈90,000 channels, 4-8% occupancy, 2 bytes/channel
  - ≈15 kB event size @ 5 kHz = 75 MB/s
- Add other detectors, allow for higher rates, …
  ⇒ must handle ≈100 MB/s
- Far exceeds current Hall A capabilities
- Need 12 GeV DAQ upgrade to meet the requirements
  - Plan exists for Hall A
  - http://hallaweb.jlab.org/equipment/daq/daq_12gev.pdf

12 GeV Upgrade DAQ Electronics

- Fully pipelined
- 200 kHz L1 trigger rate capability
- VME64x front-end crates with support for
  - High-speed readout modes (2eVME, 2eSST) up to 200 MB/s
  - Event "blocking" (buffering, caching) - up to 200 events
  - Custom serial (VXS) backplane bus:
    - Bi-directional trigger path
    - Optional data path
  - (Trunked) Gigabit Ethernet or fiber uplinks to event builder
- Synchronous trigger distribution, 250 MHz ref. Clock
- SBS will use some of this technology + custom modules

Future Front Ends

(graphics from Dave Abbott)



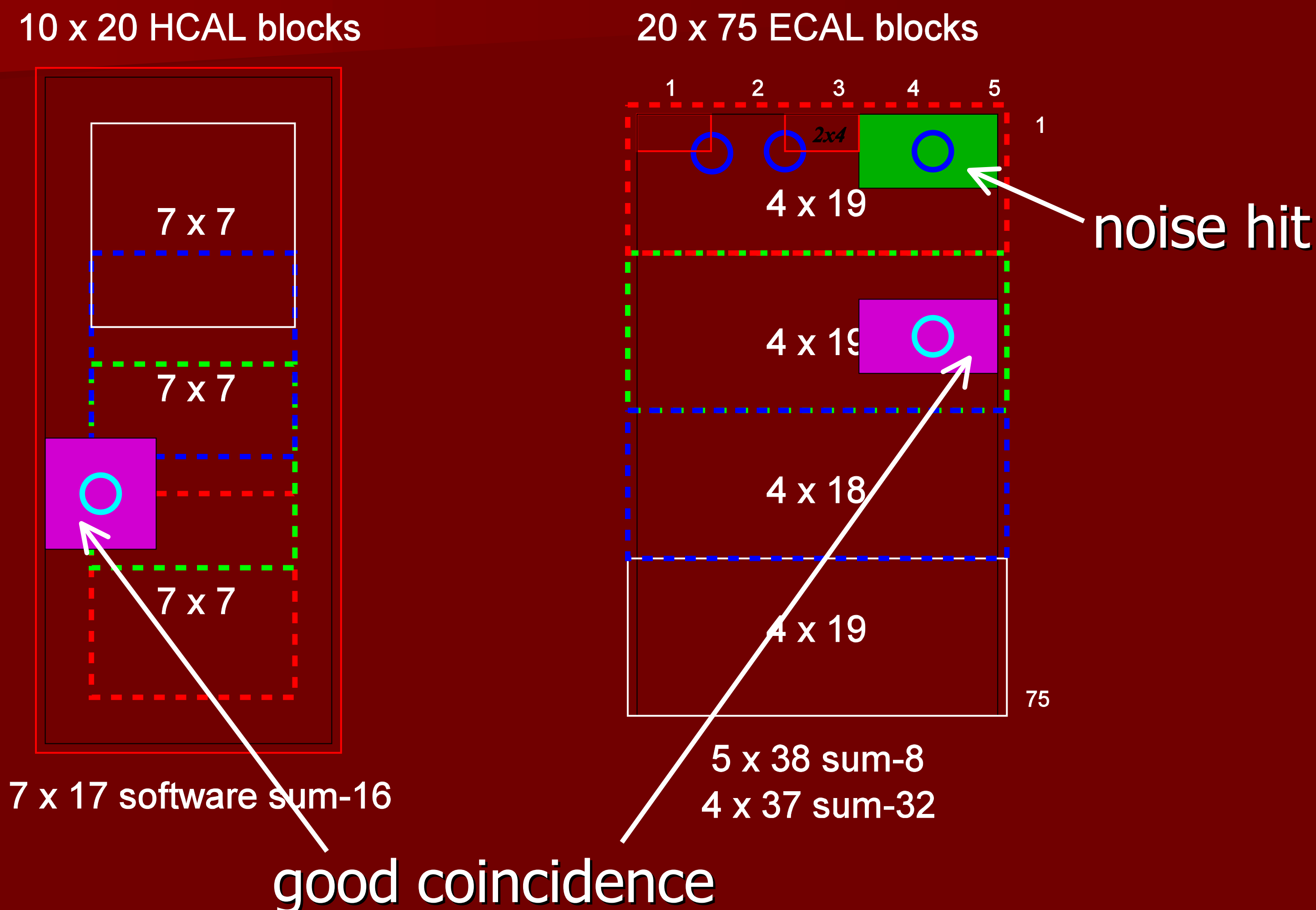
SBS Trigger Considerations

- GMn and GEn(2)
  - BigBite with gas Cherenkov and shower: ≤ 3 kHz singles. Use as is (for both arms). No need for hardware coincidence.
- GEp(5): elastic $H(\vec{e},e'\vec{p})$
  - ≈60 kHz singles in electron arm (BigCal)
  - ≈1.5 MHz singles in proton arm (SBS)
  - $\Rightarrow$ ≥ 5 kHz raw coincidence rate. Too high.
  - $\Rightarrow$ take advantage of spatial correlations in elastic scattering to build intelligent coincidence logic

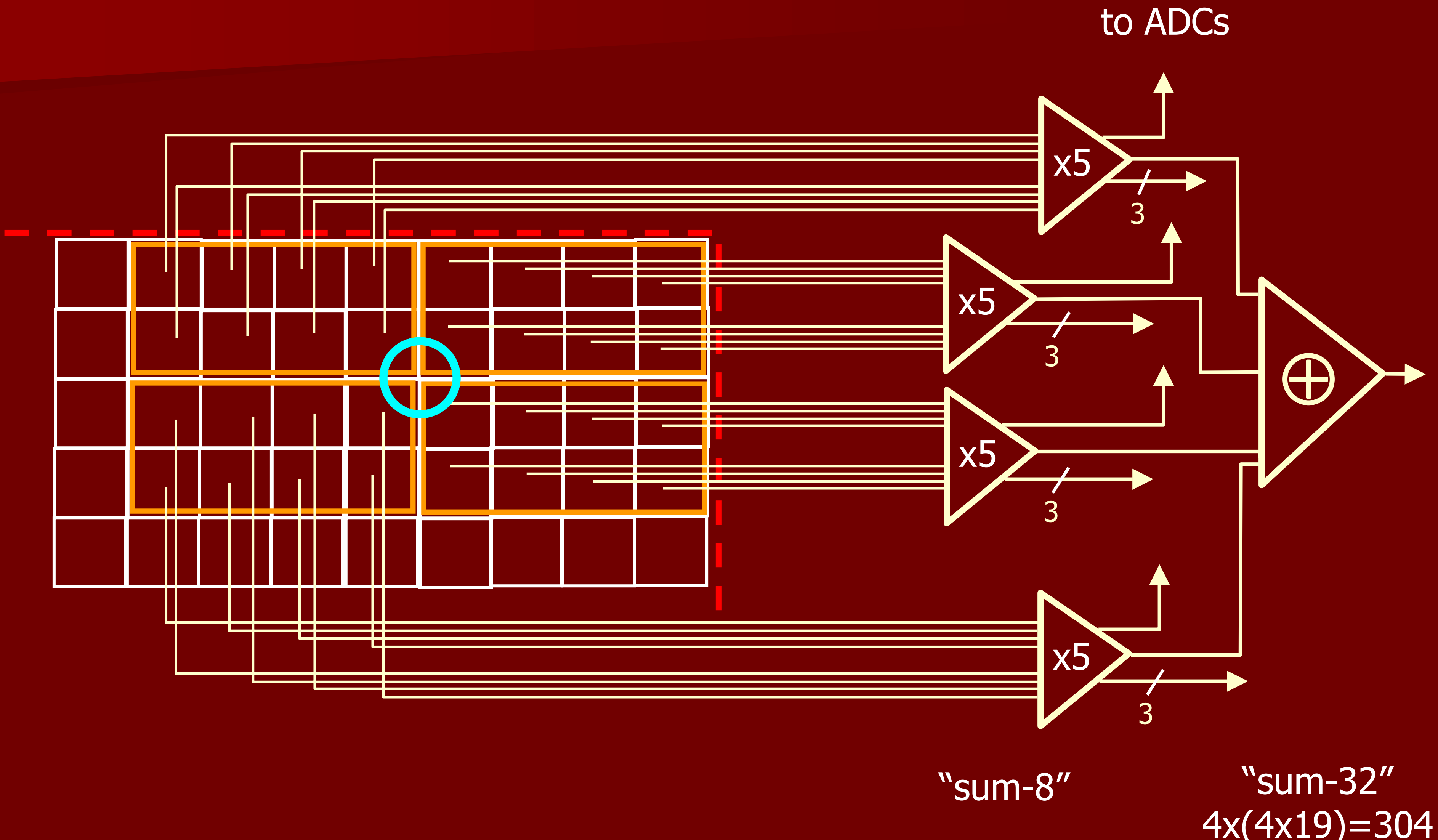
GEp(5) Spatial-Correlations Trigger

- Level 1
  - ≈100 ns
  - "Mark" samples in APV-25 GEM readouts
  - Gate Fastbus & VME
  - Generated by electron arm (≈60 kHz rate)
- Level 2
  - ≈3 μs
  - Use FPGAs to detect spatial correlations between ECAL and HCAL calorimeters
  - Reduces rate by factor of 5
  - Fast Clear FB & VME after L2 timeout $\Rightarrow$ < 20% DT

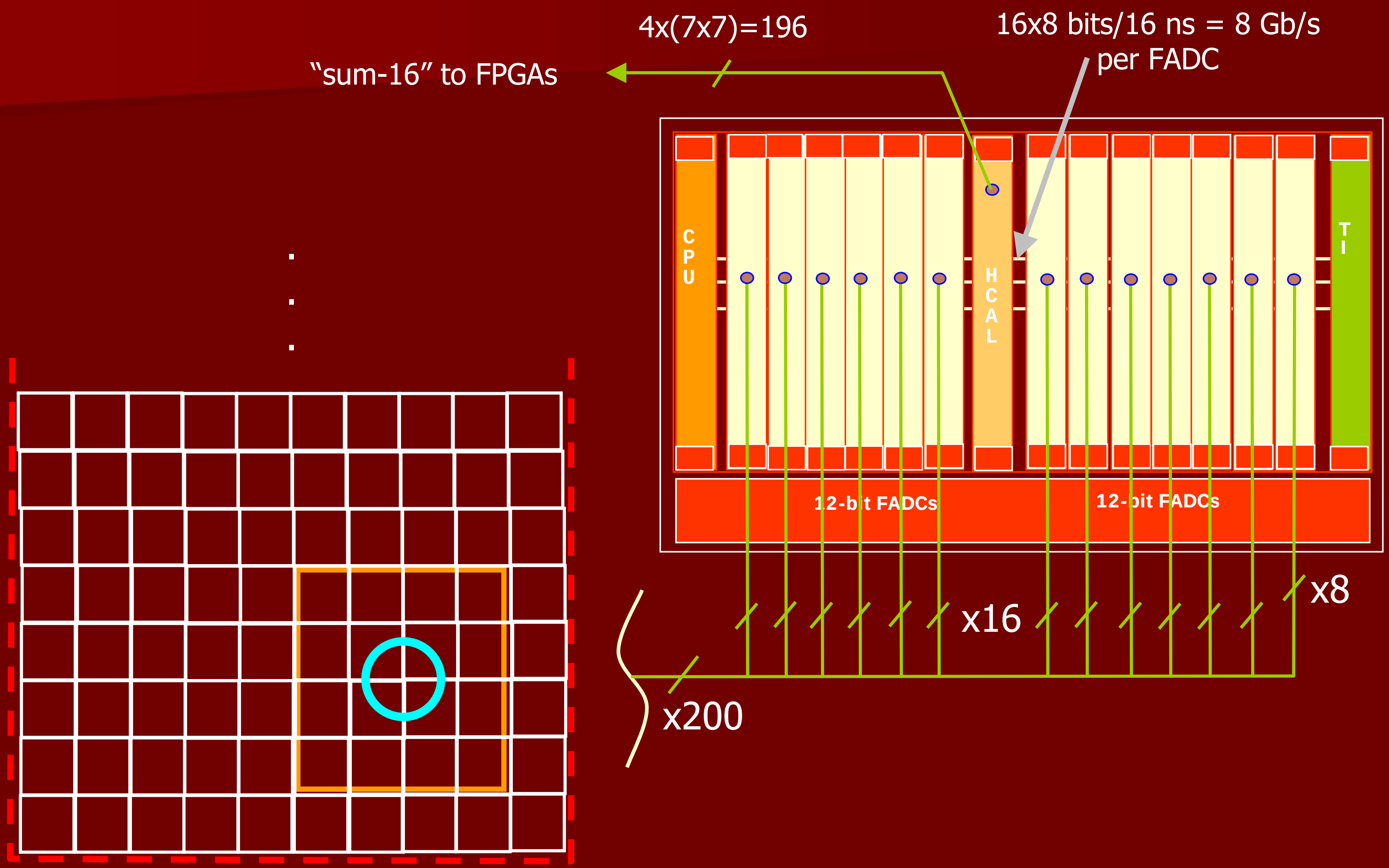
GEp(5) Calorimeter Sums



ECAL Sums



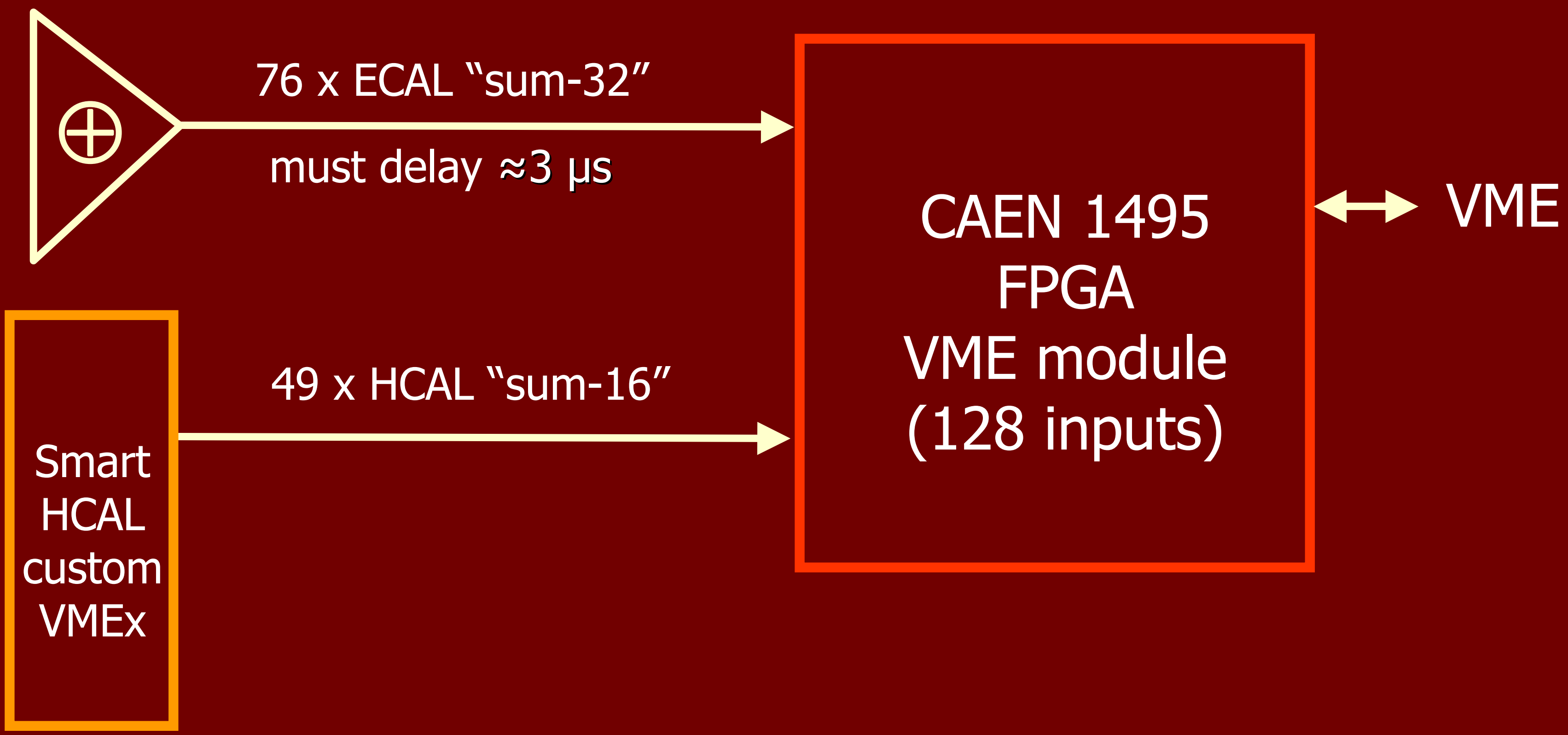
HCAL Sums



4x(7x7)=196
"sum-16" to FPGAs
16x8 bits/16 ns = 8 Gb/s
per FADC
CPU
HCAL
TI
12-bit FADCs
12-bit FADCs
x16
x8
x200

FPGA Coincidence Logic

For each calorimeter section (4x):



Conclusions

- SBS Data Acquisition rather challenging
  - Up to 100 MB/s data rate
  - Pipelined electronics
  - Custom modules
- GEp(5) Trigger similarly challenging
  - Digital summing logic for HCAL
  - FPGA coincidence logic
- Need experience, R&D