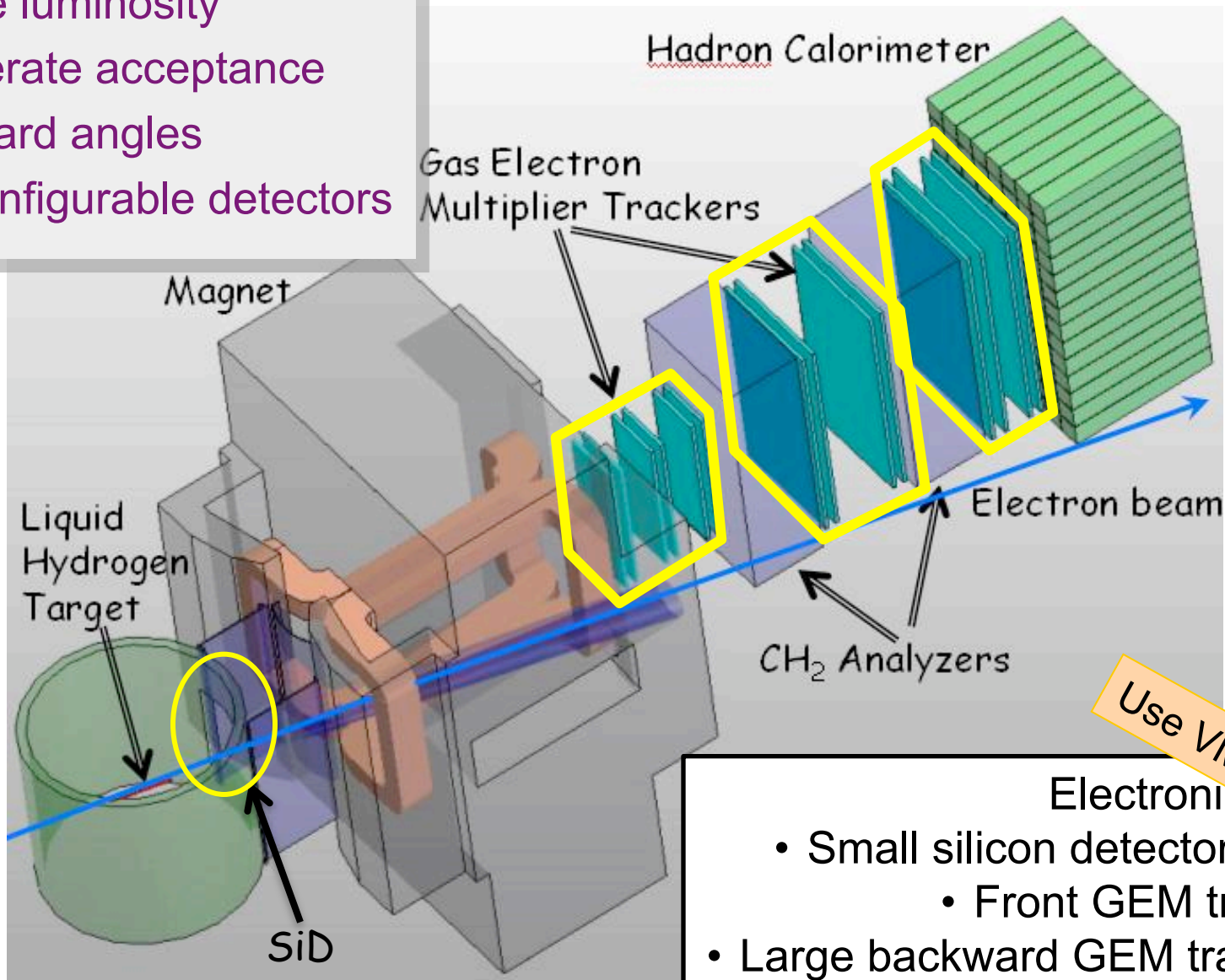
An aerial photograph of a large industrial or research facility, likely the Jefferson Lab. The image shows several large, light-colored buildings with flat roofs, interspersed with parking lots and green spaces. The facility is surrounded by dense green trees and vegetation. The overall scene is captured from a high angle, providing a comprehensive view of the complex's layout.

Status of the APV25 electronics for the GEM tracker at JLab

SBS Spectrometer in Hall A

- Large luminosity
- Moderate acceptance
- Forward angles
- Reconfigurable detectors



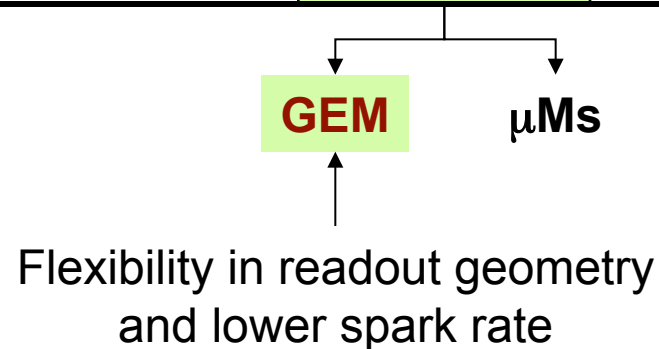
Use VME64x

- Electronics
- Small silicon detector (SiD)
 - Front GEM tracker
 - Large backward GEM trackers
- ⇒ **>100k channels**

Choice of the technology

System Requirements	Tracking Technology		
	Drift	MPGD	Silicon
High Background Rate (up to): (low energy γ and e) 1 MHz/cm²	NO	MHz/mm²	MHz/mm²
High Resolution (down to): 70 μm	Achievable	50 μm	30 μm
Large Area: from 40×150 to 80×300 cm ²	YES	Doable	Very Expensive

... and modular: reuse in different geometrical configurations



Approach: 40x50 cm² 3xGEM Module

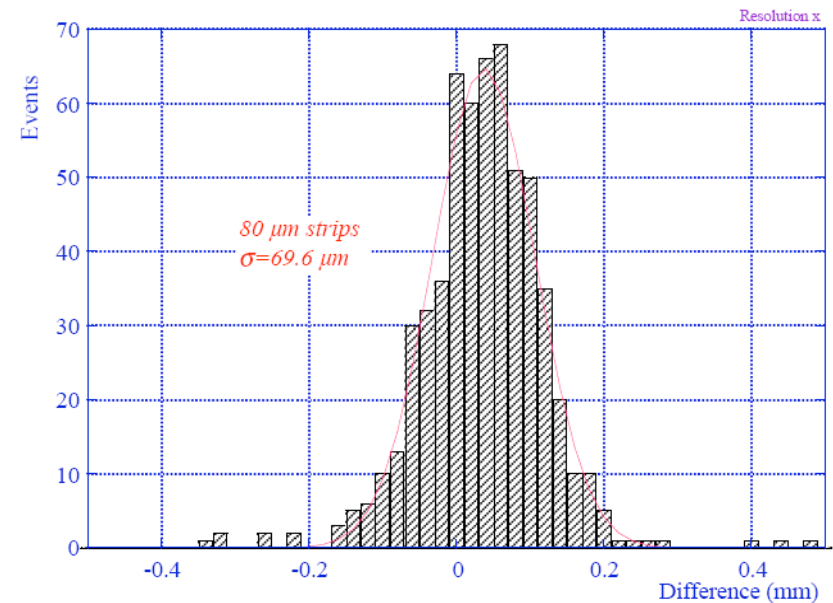
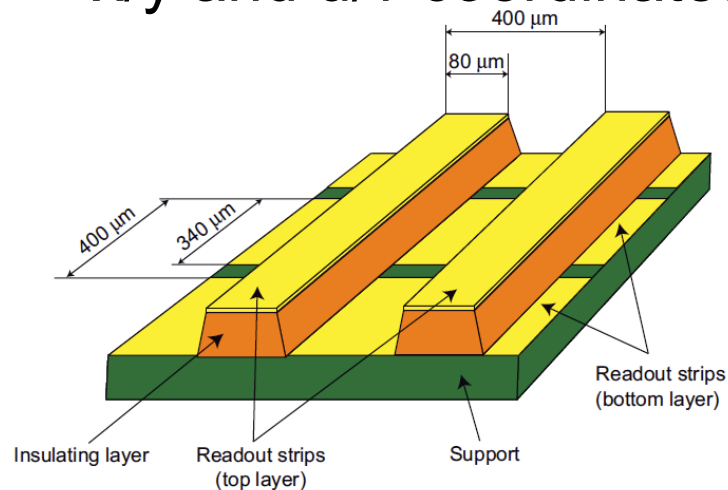
Use the same “basic” module for all trackers types

- Size: 40x50 cm² active area + 8 mm frame width

- FEM study:

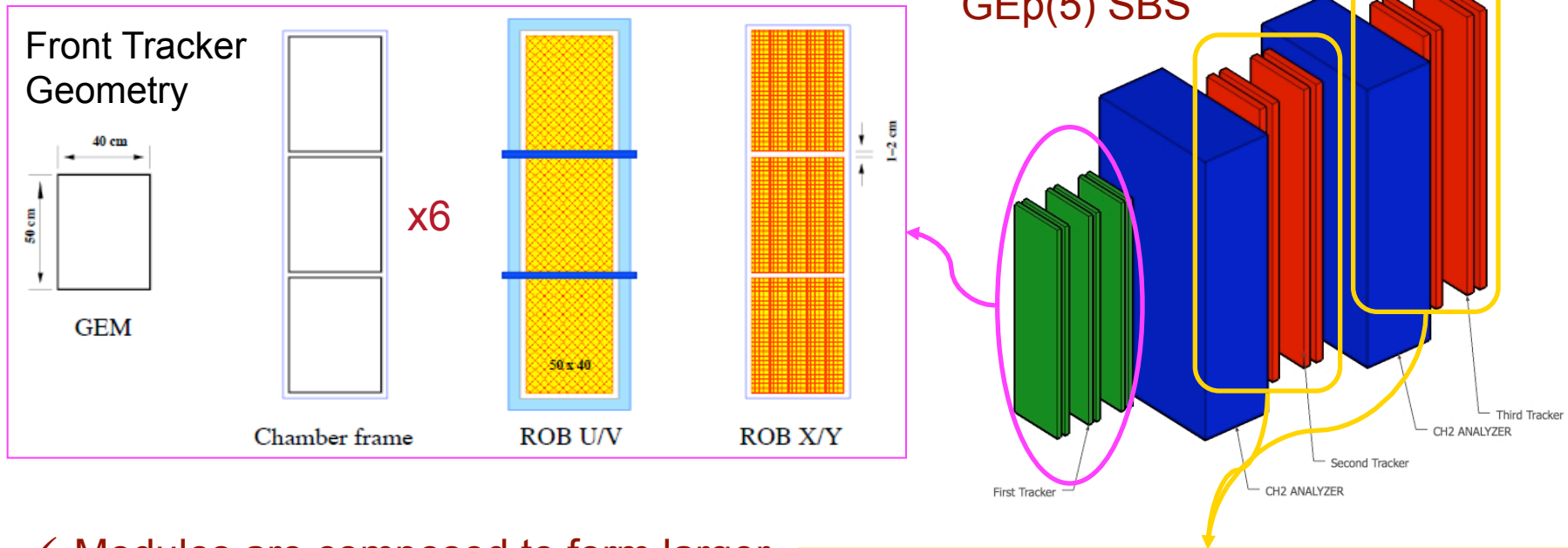
Frame width (mm)	5	6	7	8	9	10
Maximum Sag (μm)	180	24	21	19	16	12

- 3 x GEM foils (double mask) technology
- 2D strip readout (a la COMPASS) - 0.4 mm pitch
- x/y and u/v coordinates

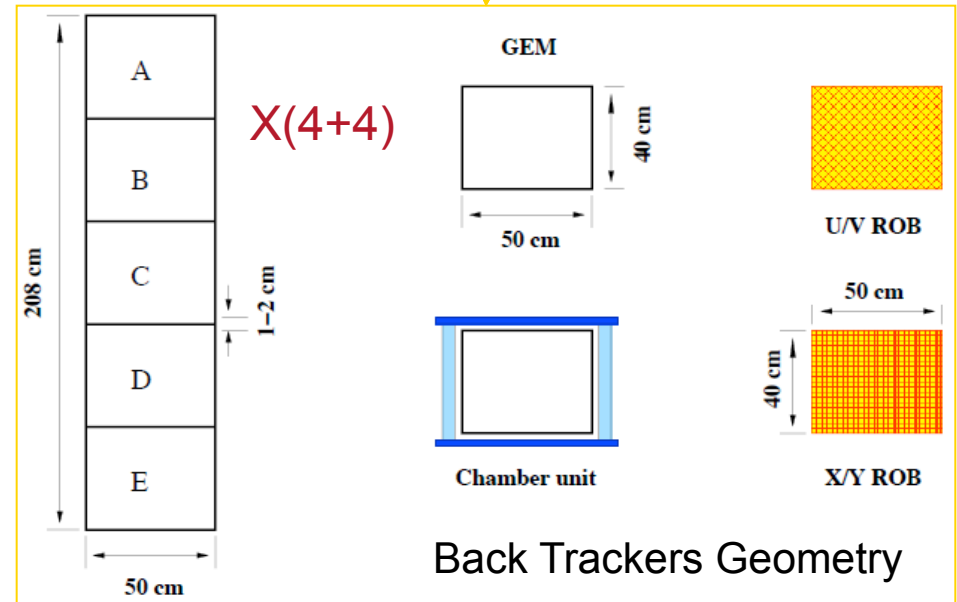


Performances proven in real experiment such as COMPASS and PREX!

SBS Tracker Chambers configuration



- ✓ Modules are composed to form larger chambers with different sizes
- ✓ Electronics along the borders and behind the frame (at 90°) – cyan and blue in drawing
- ✓ Carbon fiber support frame around the chamber (cyan in drawing); dedicated to each chamber configuration

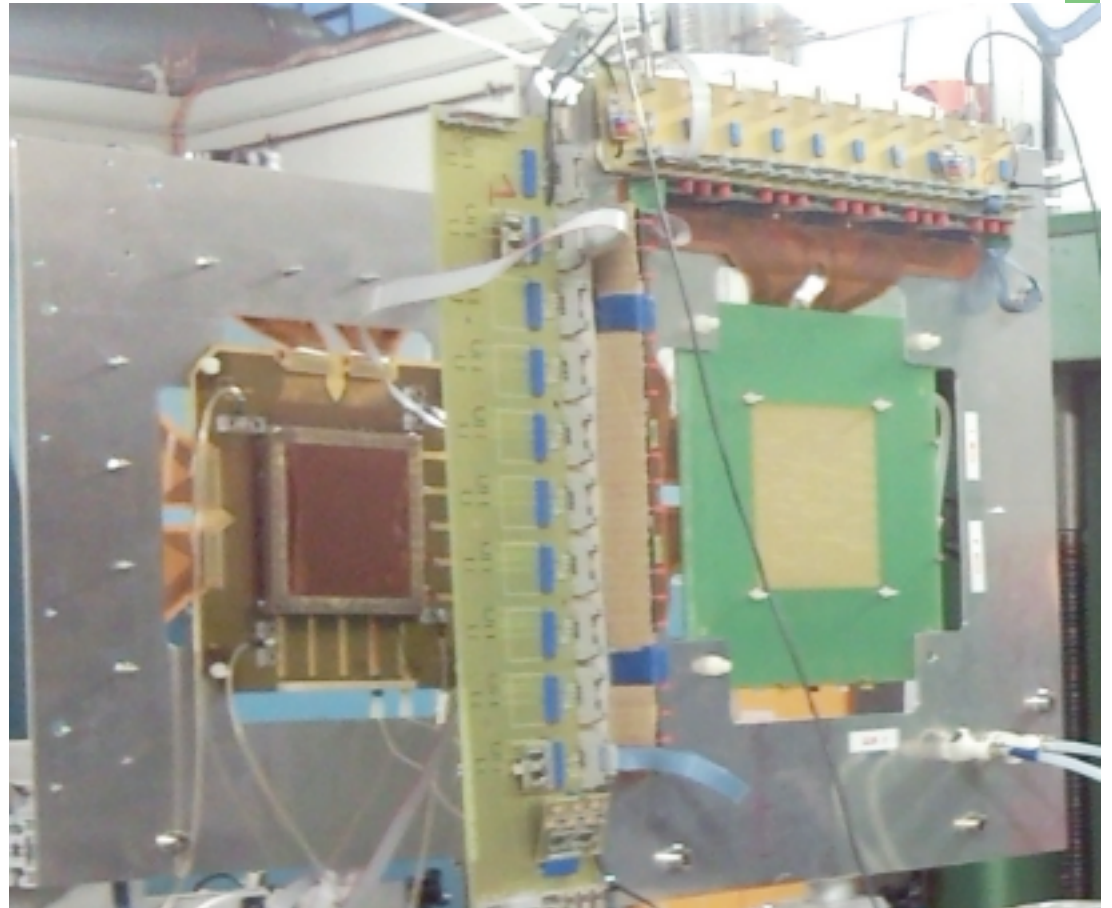


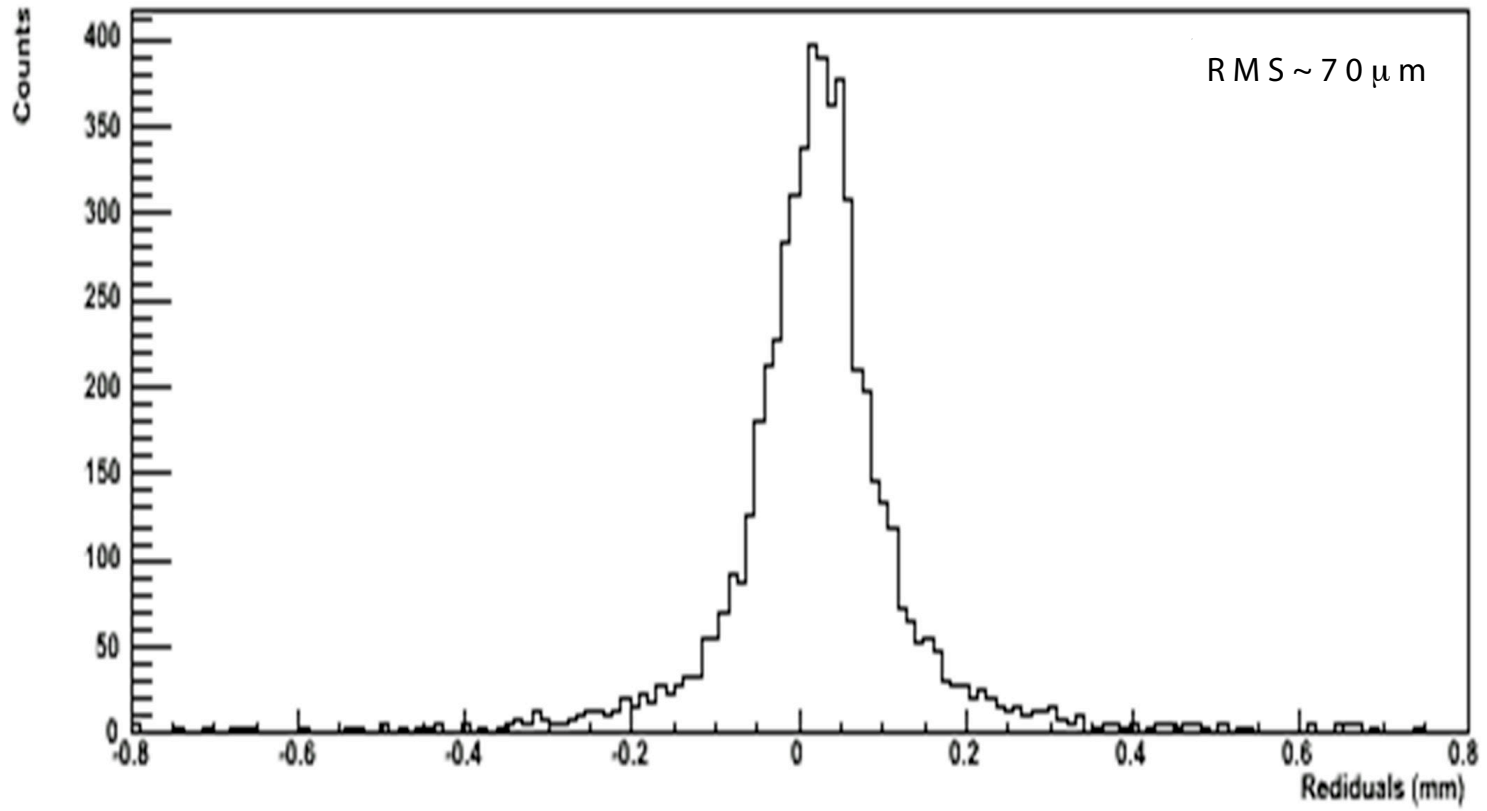
SBS GEM chamber prototyping

- Prototype GEM tracker consisting of five 10 cm x 10 cm chambers built.
- Already tested in high rate conditions during hall A PREX experiment. Data being analyzed now
- More extensive test with APV-25 electronics and under high background rates planned for this Autumn.
- A 40 cm x 40 cm prototype and APV-25 electronics under construction at INFN.

Topics to study

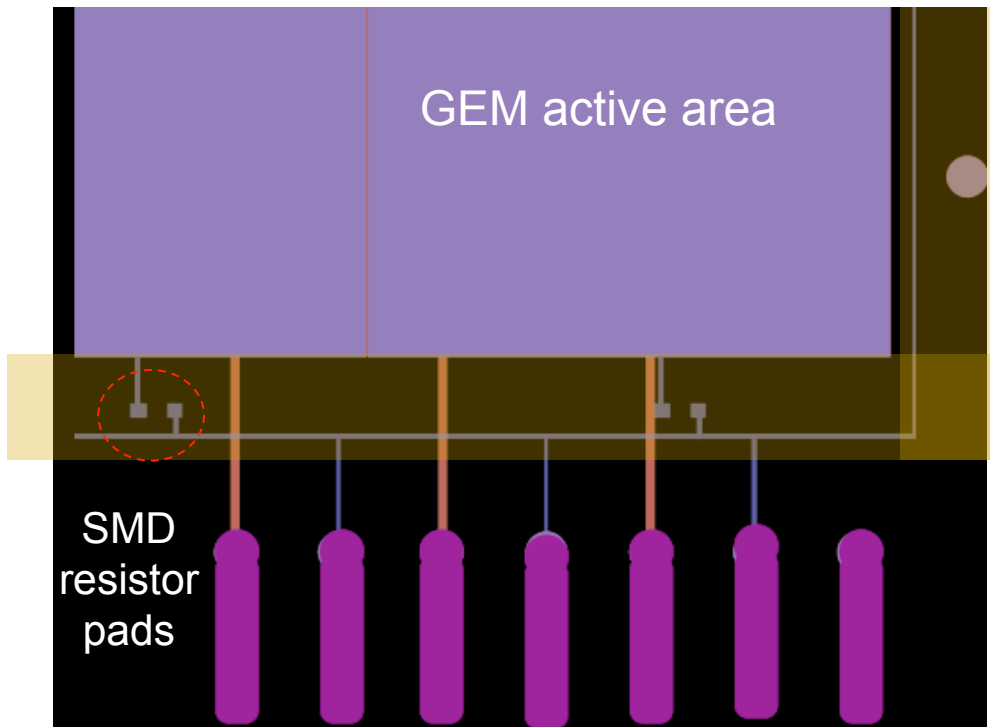
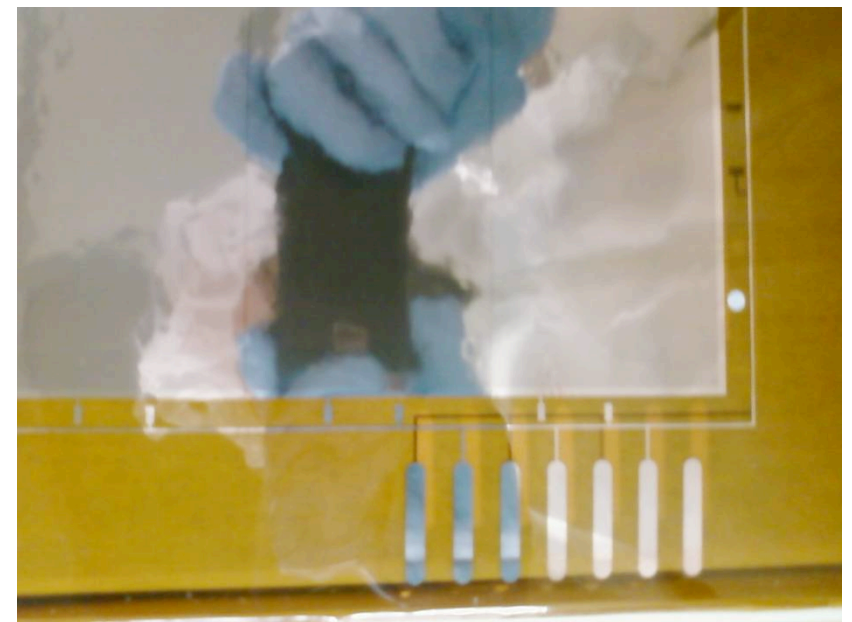
- Tracking under high rates
- Response to low energy photons
- Readout plane size limitations (noise pickup, capacitance etc.)
- Combining readout strips



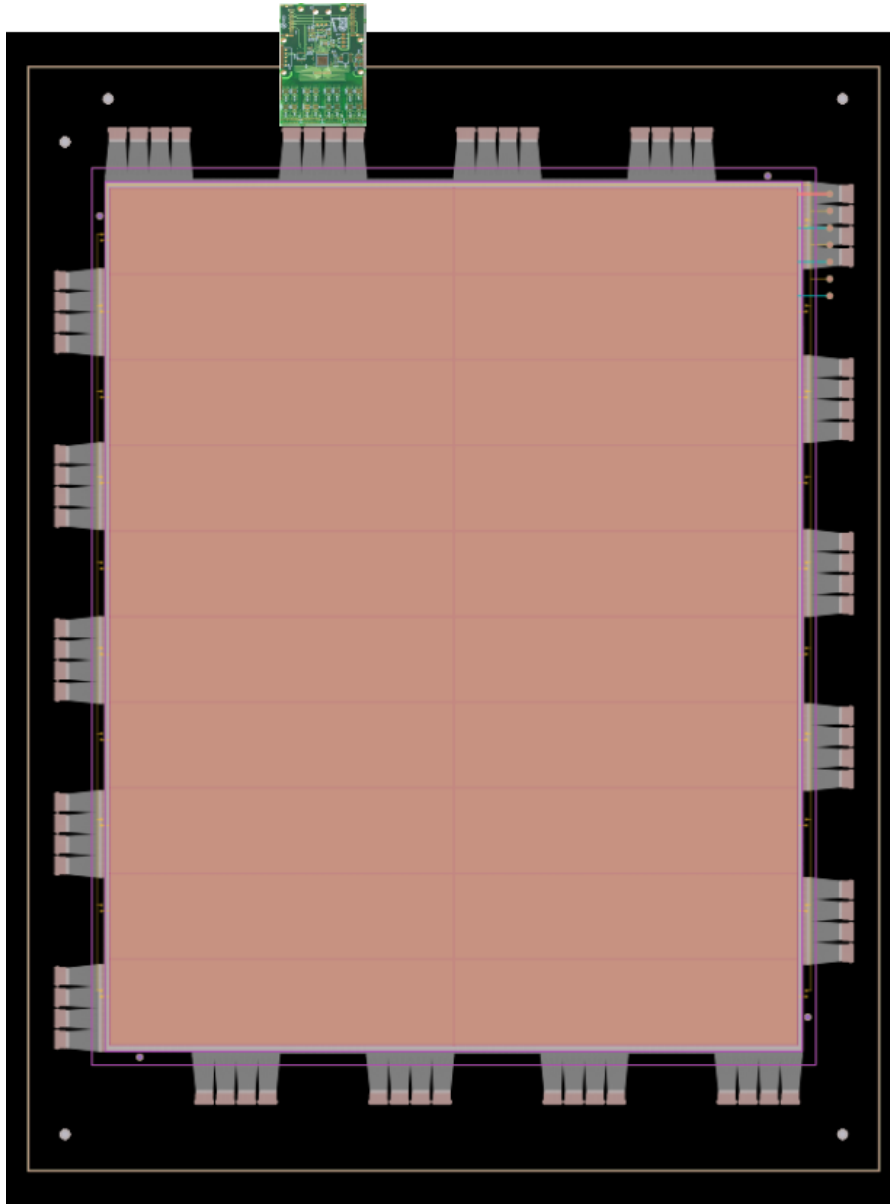


GEM foil (first 40x50 cm² / double mask technique)

- **7 independent HV channels** for each chamber (TBC)
- 3 HV identical doublets + 1 for drift (same on all GEM foils); each doublet serves one GEM foil, unused will be cut.
- SMD protection resistors, under the thin frame

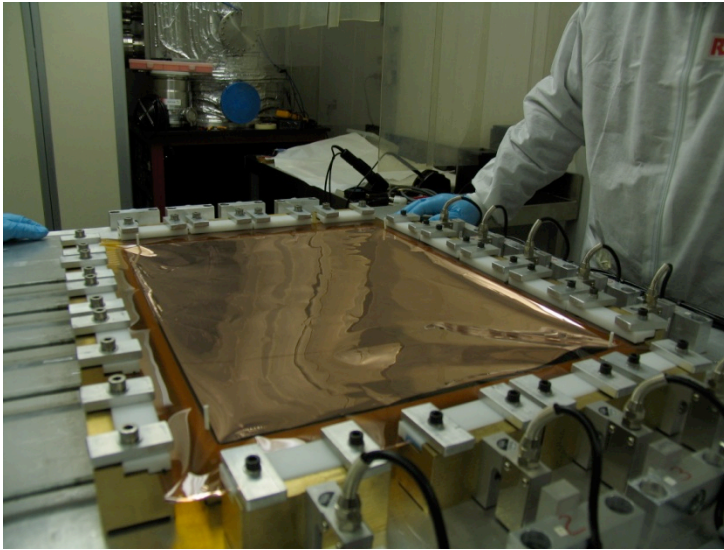


Readout Foil

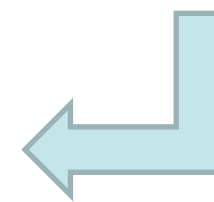
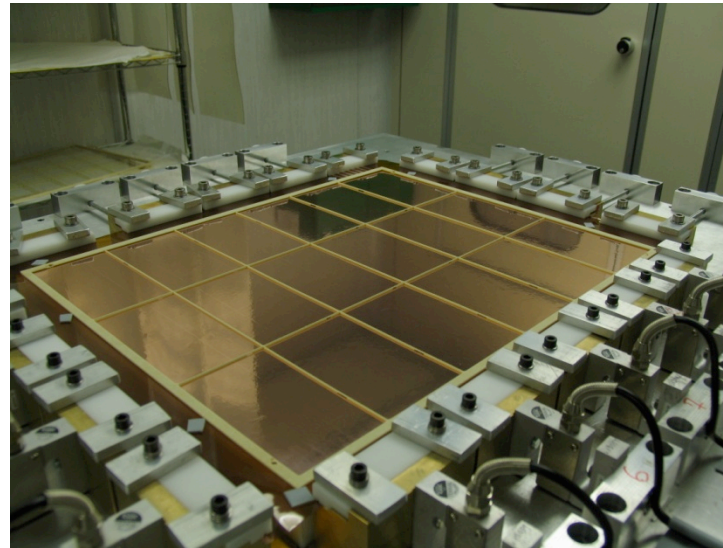
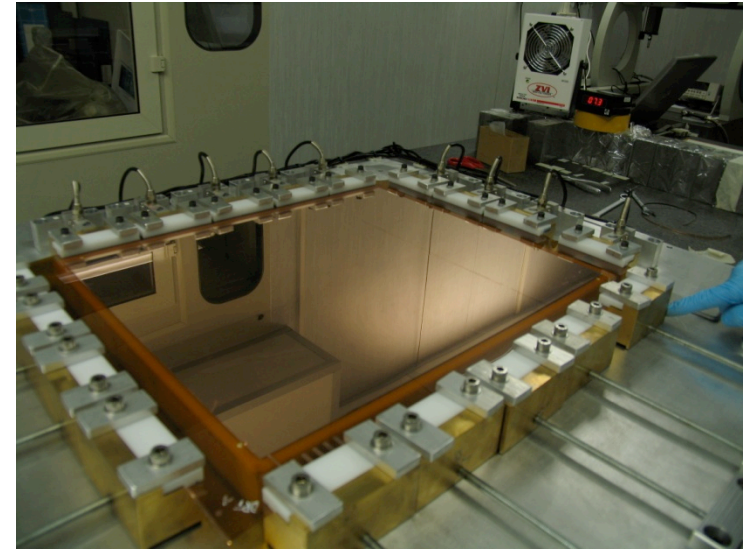
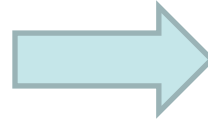


No soldering, very thin connections
Laser cutting required

Assembling the first 40x50 cm² module



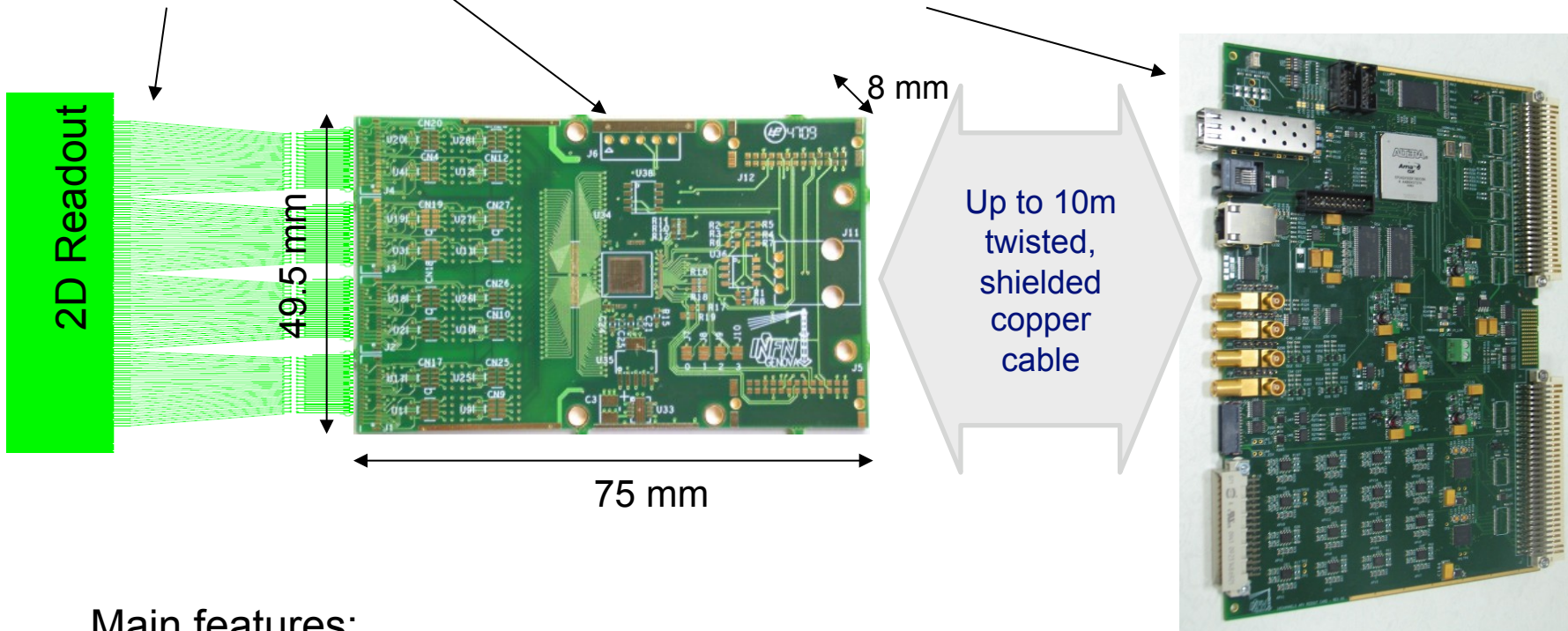
Stretching



Gluing the next
frame with
spacers

Electronics Components

GEM ⇒ FEC ⇒ ADC+VME Controller ⇒ DAQ

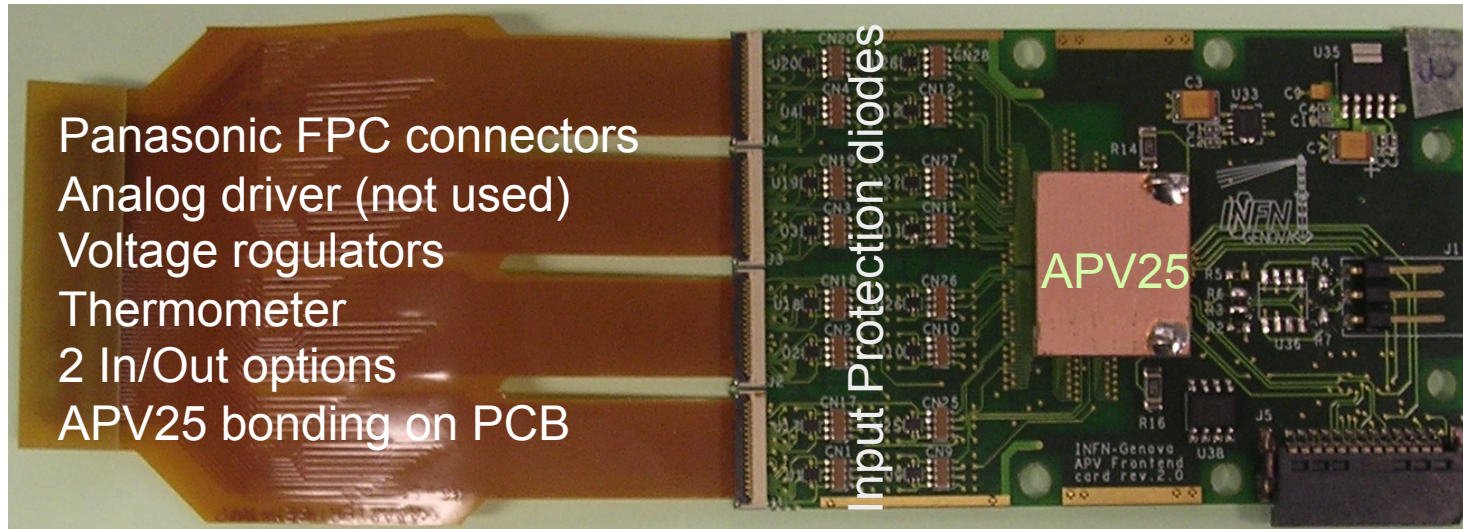


Main features:

- Use analog readout APV25 chips
- 2 active components: Front-End card and VME64x custom module
- Copper cables between front-end and VME

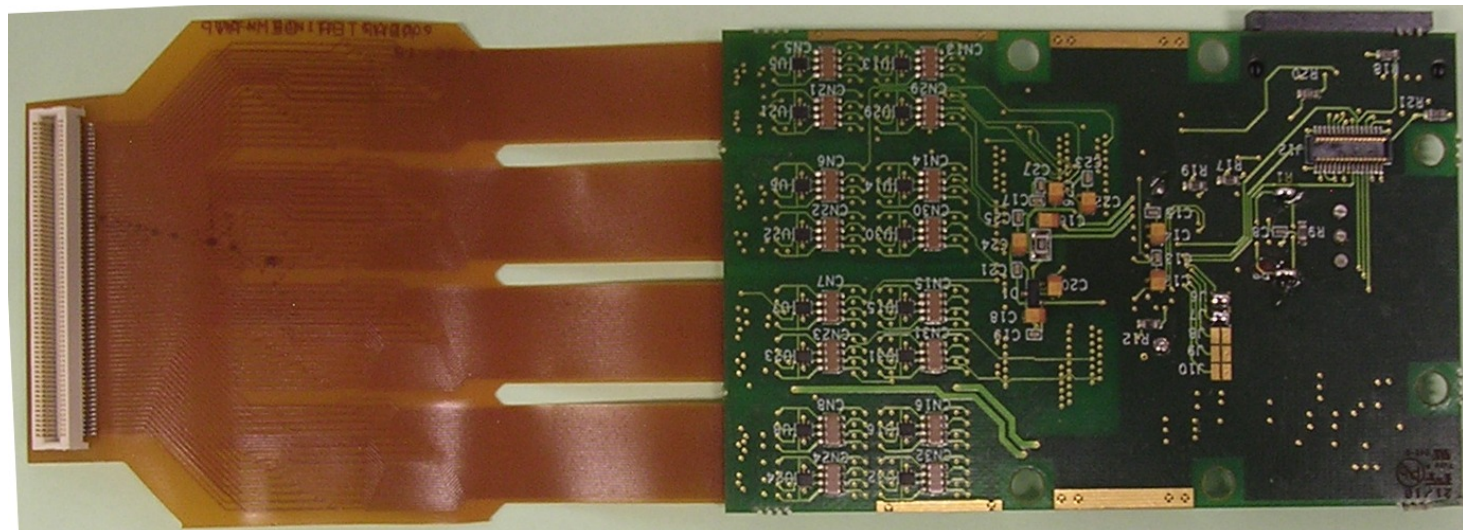
Front End Card (Proto 1)

GEM ⇒ **FEC** ⇒ ADC+VME Controller ⇒ DAQ



Analog
Output

Digital Input +
Power supply

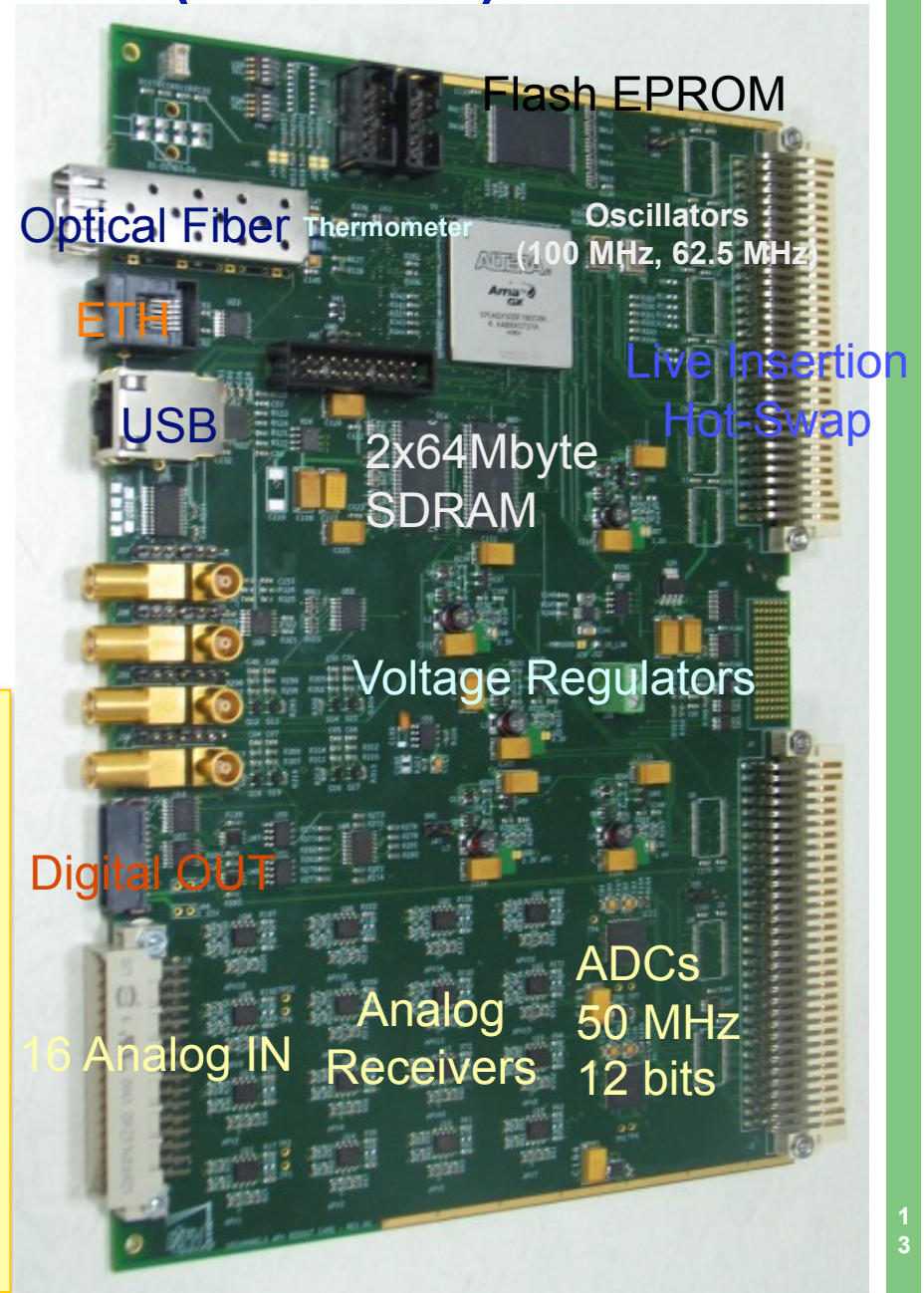


Analog out +
Digital Input +
Power supply

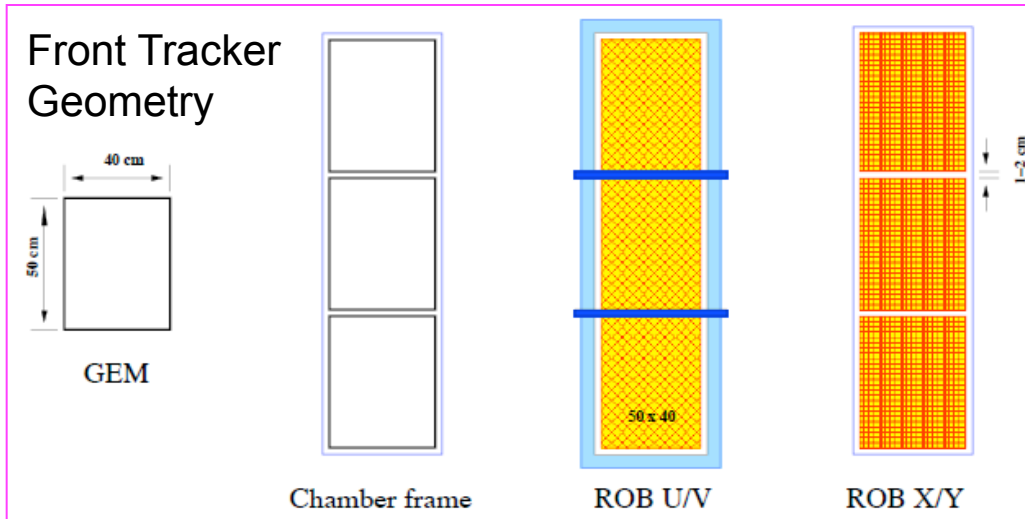
VME64x Controller (Proto 0)

- VME controller hosts the digitization of the analog signals coming from the front-end card.
- It handles all control signals required by the front end cards (**up to 16 FE**)
- **Compliant to the JLab/12 VME64x VITA 41 (VXS) standard**
- We intend to make it accessible by standard VME/32 as well

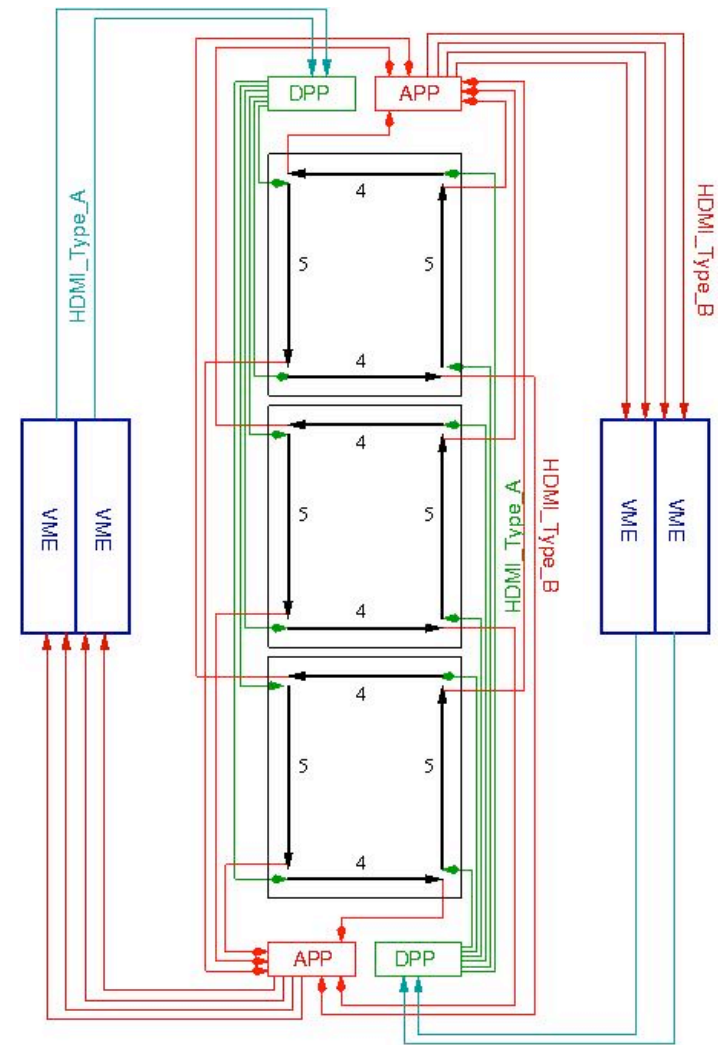
- **Version 1 submitted for production:**
 - Minor bug fixed
 - 2 HDMI-type A: digital lines + 2 analog lines (compatible with SRS hybrids connector)
 - 2 HDMI-type B: 16 analog lines
 - Added delay line for clock-convert phase fine tuning (DELAY25 from CERN)



GEM Electronics Layout



1. Use high density, high quality, standard HDMI (A-type for digital signals, B-type for analogo output)
2. Analog and digital lines rus independently
3. Analog and Digital patch panels collect and reroute channels
4. Similar solution for the SiD planes



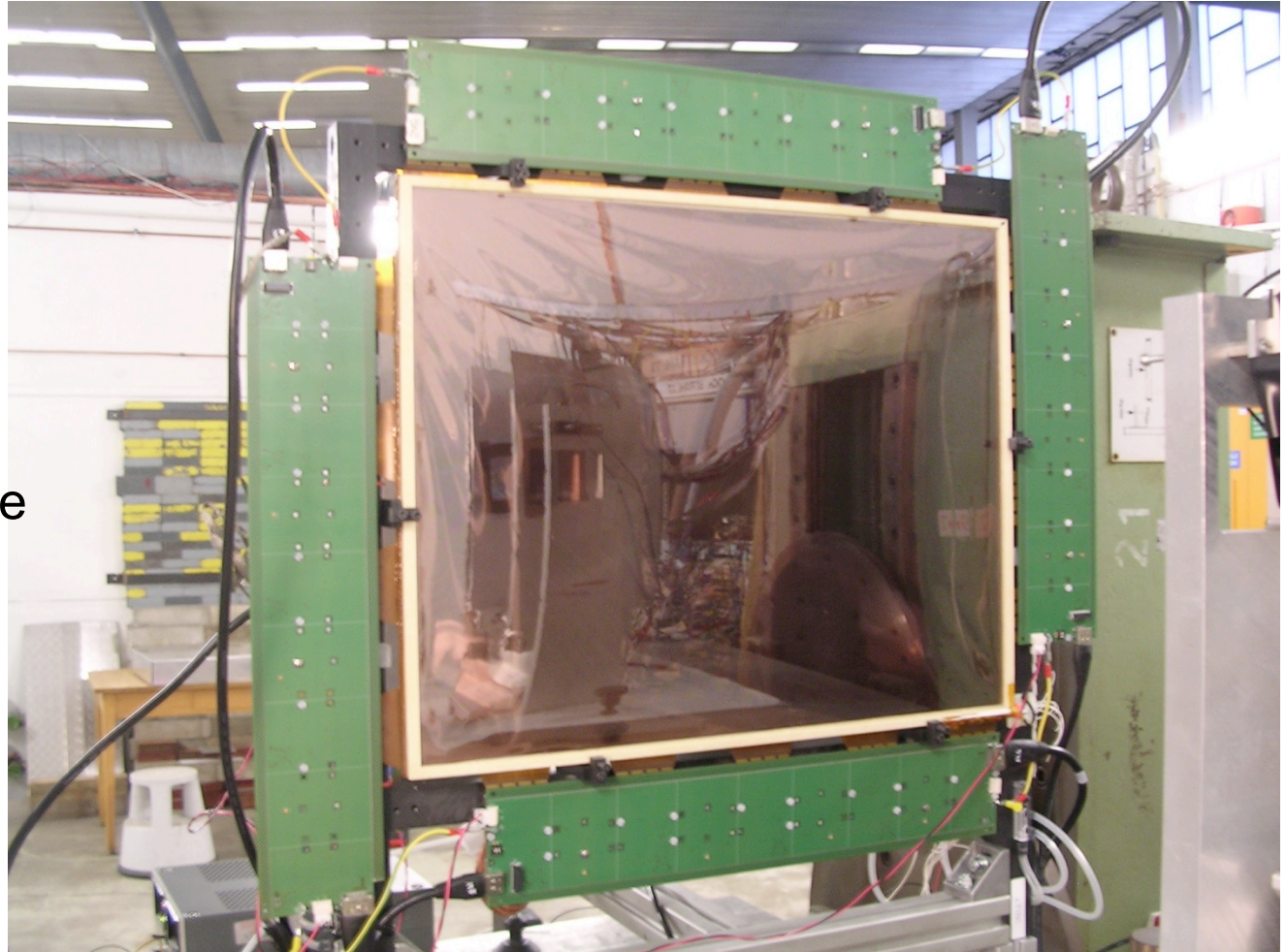
VME ⇔ Patch Panel ⇔
Backplane ⇔ Front End Cards

Beam test @ DESY (EUNET support)



Beam test @ DESY (EUNET support)

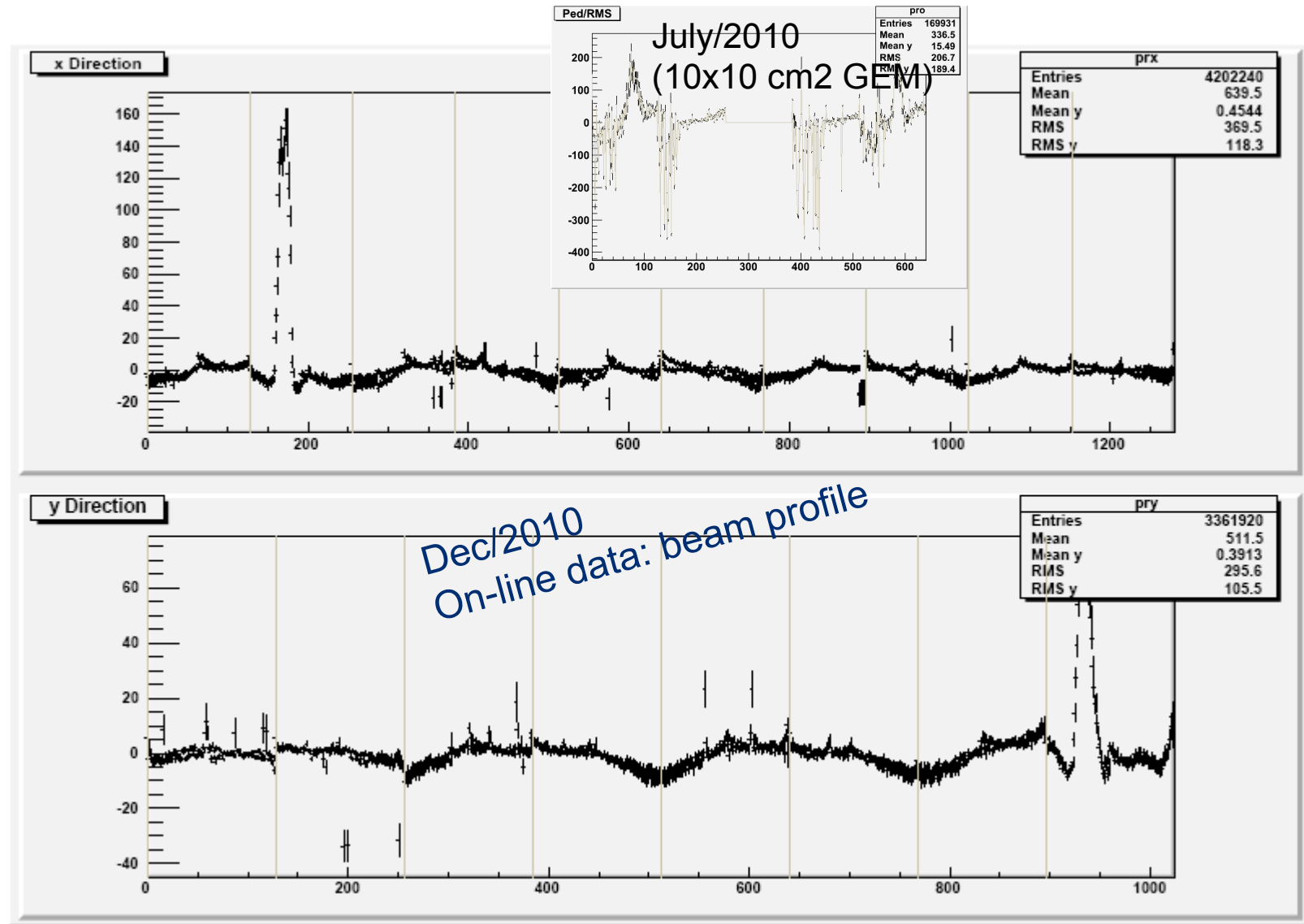
- Fully equipped GEM module
- 18 front-end cards
- 2304 channels
(front end cards on the other side)
- 7 independent HV levels



2-6 GeV low intensity electron beam / silicon tracker available

Data taking: 28/Nov-3/Dec 2010

Beam test @ DESY (EUNET support)

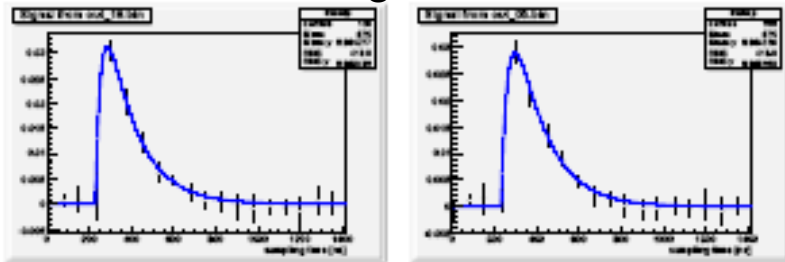


Large improvement from July

Analysis has just started

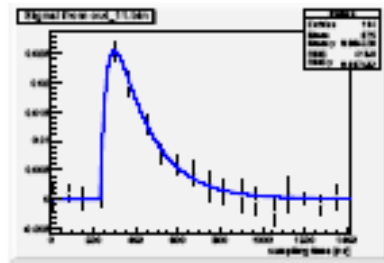
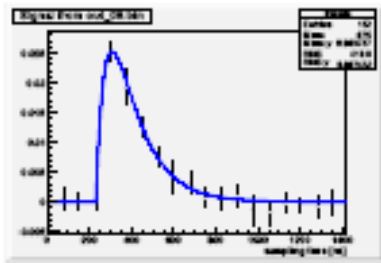
Signal vs Cable length

Test signal



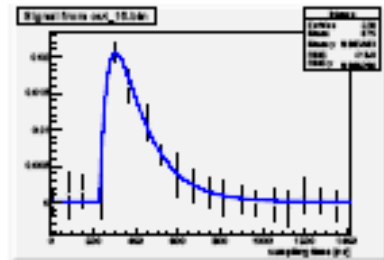
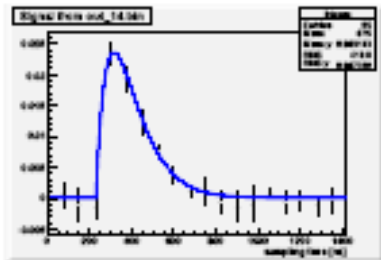
3 m

6 m



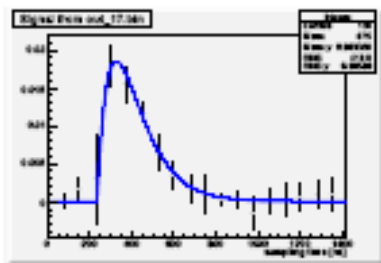
10 m

13 m



16 m

26 m



36 m

Amplitude

⇒ Long cables seems to work well: no distortion, noise slightly increase, amplitude attenuation as expected

Capacitance coupling to be optimized (in final size chamber)

APV25 parameters to be tuned!

Conclusions

- GEM:
 - First full size module built and beam-tested
 - Analysis of the test data just started
 - Improvement of the assembling procedure ongoing
 - Pre-Production will start soon
- Electronics:
 - Second prototype tested, both front-end and VME controller - Can be considered final version
 - APV parameters tuning
 - Firmware under heavily development

- we finalize the first 40x50 cm² and tested it in DESY (2-6 GeV electronbeam) last 2 weeks, together with the latest version of the electronics. There is still some noise but the situation is much better respect to the test we performed in July with a small 10x10 cm² GEM. Next weeks will be devoted to the analysis of the data, to the improvement of the assembling procedure of the GEM module and to the further development of the firmware for the VME controller. The attached slides summarize the current status and present the very first results. The analysis has just started.