Hall A DAQ status and upgrade plans

Alexandre Camsonne
Hall A Jefferson Laboratory

Hall A collaboration meeting
June 10th 2011

Outline

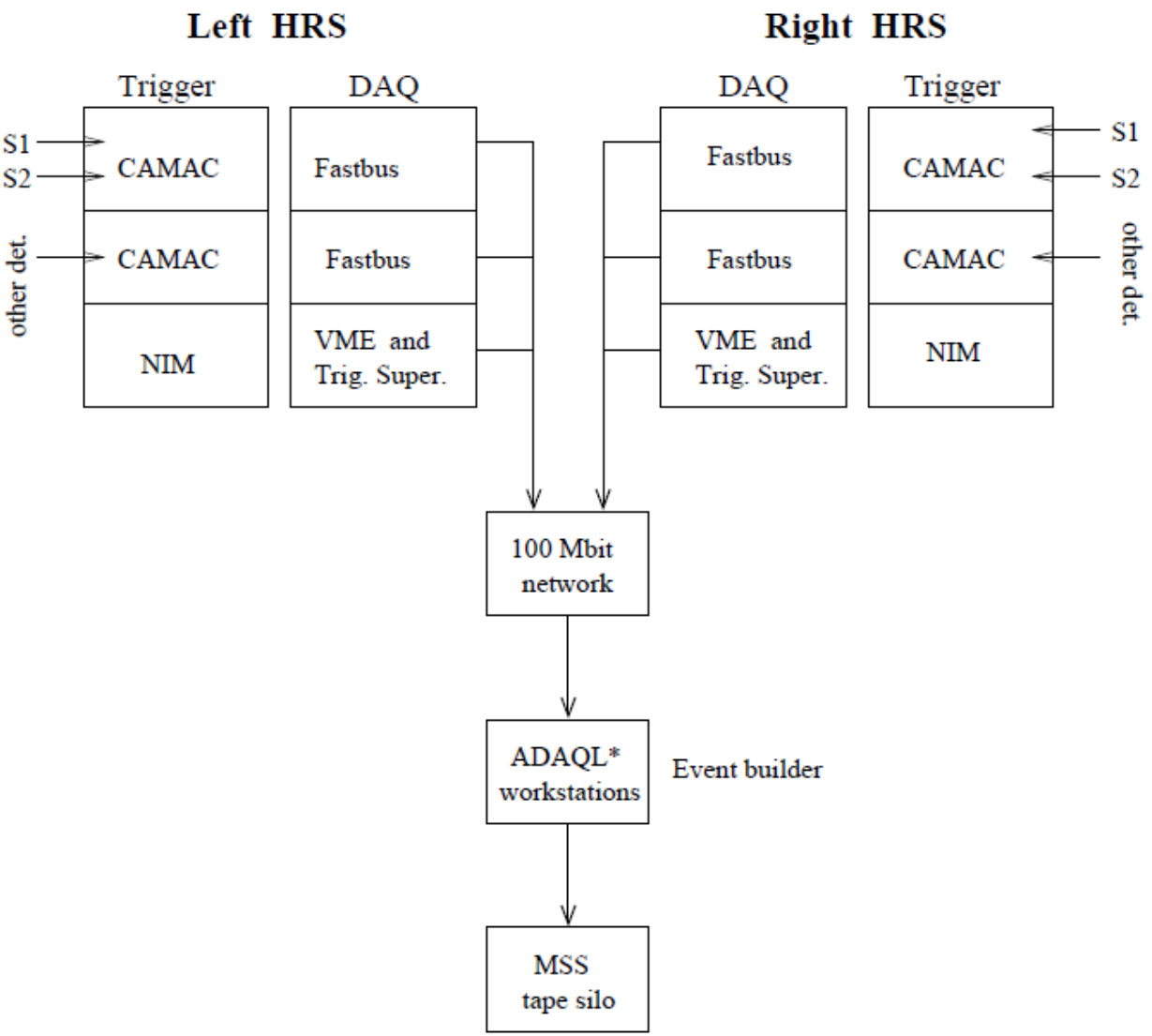
- HRS DAQ upgrade
  - Motivation
  - Current
  - Possible trigger layout
  - Timeline
  - Intel VME CPU
  - CAMAC
- Future experiments
  - Pipelined electronics
  - Fastbus
  - L3 Farm
- Summary

HRS DAQ upgrade motivations

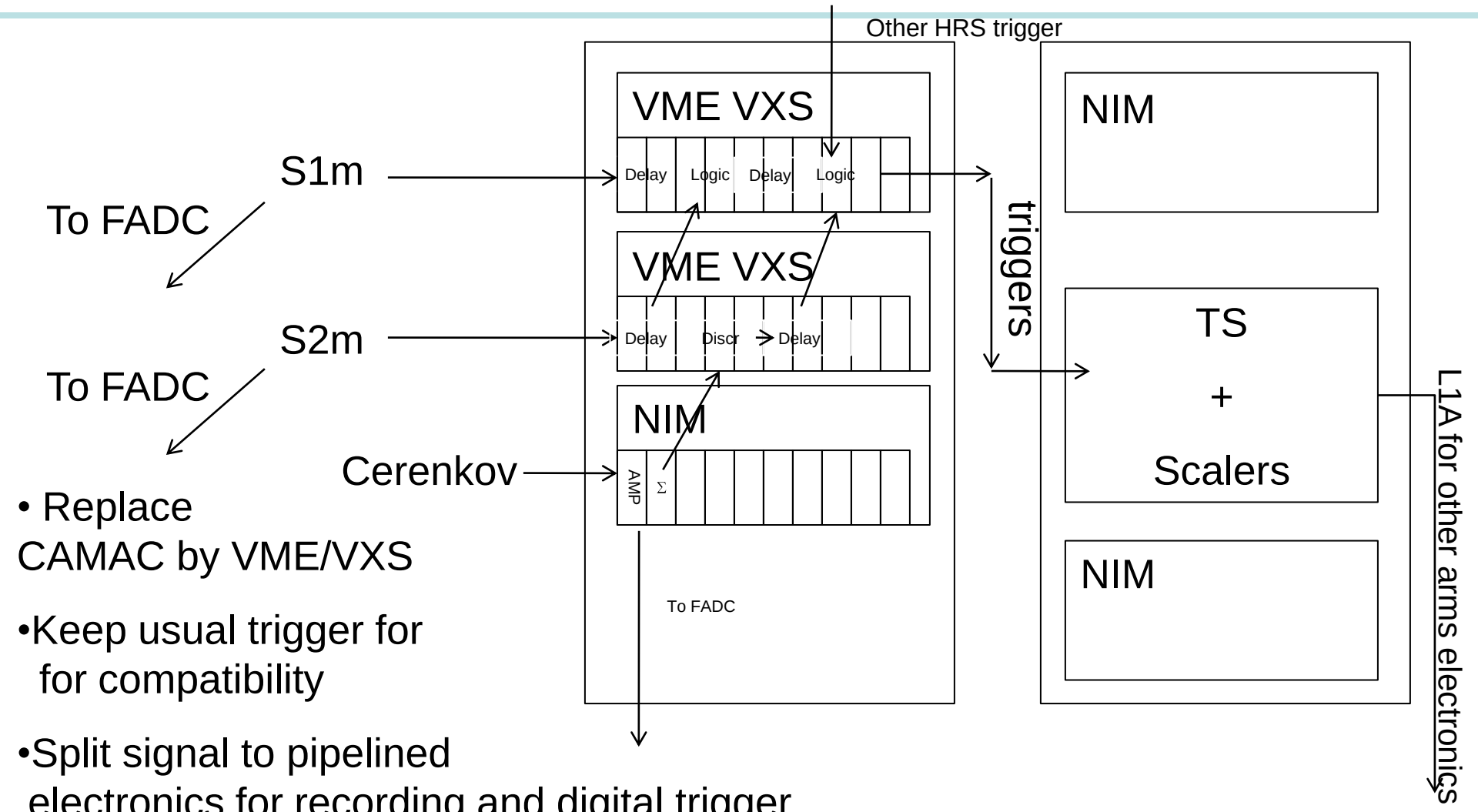
- Upgrade rate capability and deadtime : current rate limited to 4 KHz at about 15 % dead time
- CAMAC modules obsolete : replace with NIM and VME
- High resolution TDC 1875 replacement

http://hallaweb.jlab.org/equipment/daq/daq_12gev.pdf

Current HRS

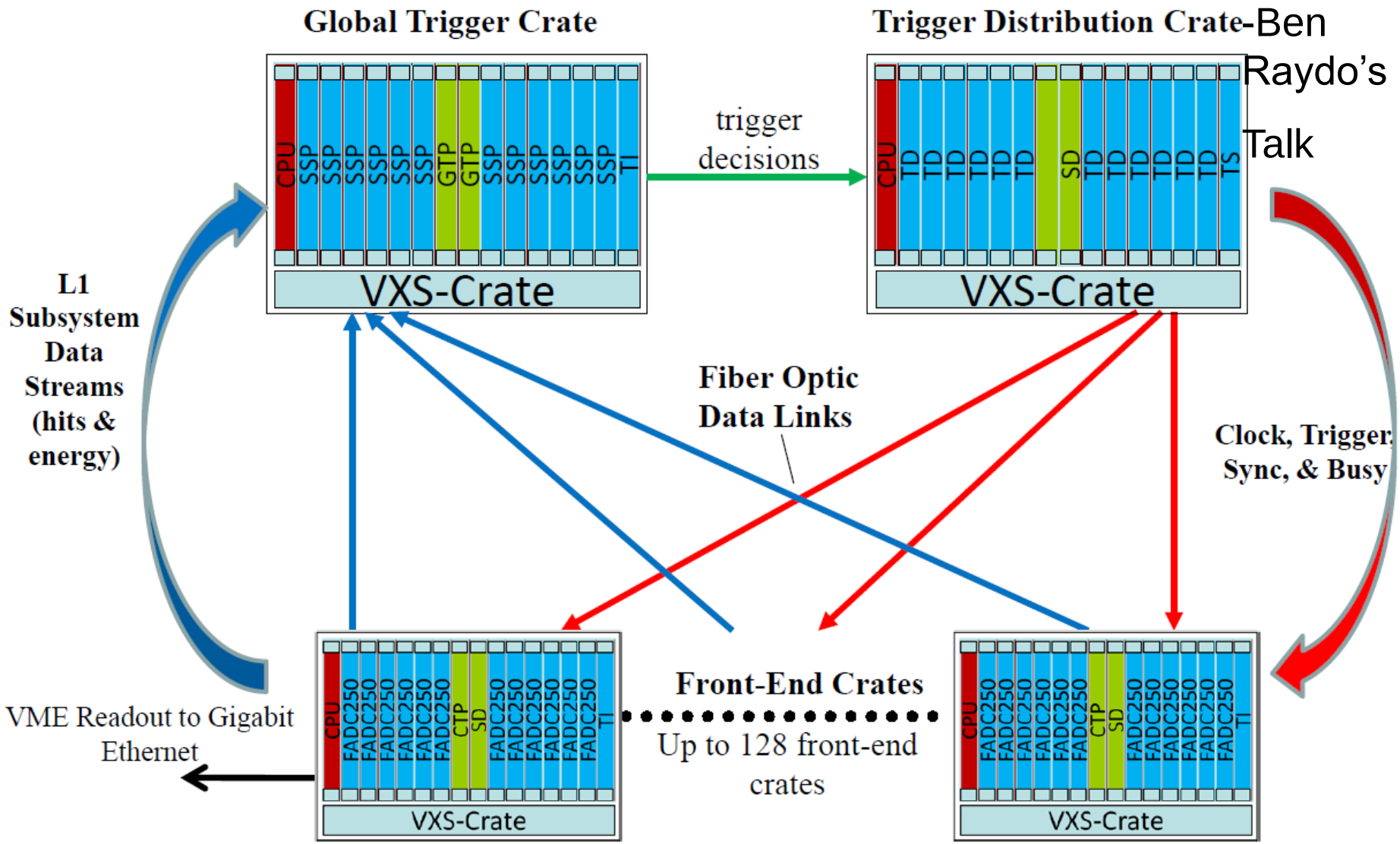

Left HRS
Right HRS
Trigger
DAQ
DAQ
Trigger
S1
S2
other det.
CAMAC
CAMAC
NIM
Fastbus
Fastbus
VME and Trig. Super.
Fastbus
Fastbus
VME and Trig. Super.
CAMAC
CAMAC
NIM
S1
S2
other det.
100 Mbit network
ADAQL* workstations
Event builder
MSS tape silo

Possible trigger layout



- Replace CAMAC by VME/VXS
- Keep usual trigger for for compatibility
- Split signal to pipelined electronics for recording and digital trigger

Level 1 & Trigger Distribution



HRS 12 GeV Hall A DAQ upgrade milestones

Milestone	Planned completion
• Test 1190 and 1290 TDCs on HRS	Oct-11
• Implement Fastbus upgrade with Intel Quad cpus	Nov-11
• Complete the Design of Test Stand for Pipelined Electronics	Dec-11
• Obtain prototype TIR boards, new ROC and EB components for CODA 3	Jan-12
• Complete the Design of the Delay Modules (Ben Raydo)	Feb-12
• Parts for Test Stand Delivered (FADC, TDCs, TIR, etc)	Mar-12
• Test of Delay Module Prototype Completed	Apr-12
• Initial Testing of Pipelined Electronics, informing final design	May-12
• Preliminary Design of DAQ and Trigger	Jun-12
• Order Delay Modules and other Trigger Modules	Jul-12
• Completed Tests of Pipeline Electronics	Aug-12
• Final Design of DAQ and Trigger	Sep-12
• Order ADCs and TDCs (at this point, looks like Jlab FADC and CAEN 1190)	Oct-12
• Order Crate Trigger Supervisor, Subsystem Decision Modules, etc.	Nov-12
• Order Fibers and Gigabit Ethernet	Dec-12
• All DAQ and Trigger modules delivered	Jan-13
• Analysis Software Upgrades Completed (based on Test Stand)	Feb-13
• Assembly of Full DAQ System Complete	Mar-13
• Preliminary Tests of Full DAQ System	Apr-13
• Final Tests of Full DAQ System	May-13

Intel VME CPUs

- Dual Core CPU
- Running Linux

- Deploy infrastructure for operating

- Support from DAQ group : Bryan Moffit and David Abbott
  Fastbus library adapted for the new CPU

- CPUs ordered and will be tested this summer

- Possible improvement of rate capability by a factor of 2 will be tested for g2p

CAMAC replacement

- Lecroy 4518 delay module
  - Development by Jlab electronics group
- Lecroy 4413 discriminator
  - JLAB VME discriminator available
    - 16 channels
    - 2 outputs with two different thresholds
    - Or output
    - Possibility to implement logic
- MLU 2373
  - CAEN V1495 : multipurpose FPGA logic module
  - very versatile logic but need to be careful for accurate timing

Future experiments

- SuperBigBite
  - GEM
  - Fastbus
- DVCS
  - Calorimeter
  - Analog sampling electronics
- SoLID
  - Fully pipelined electronics
  - L3 Farm

Pipelined electronics

- Continuous readout of data
- No dead time
- Fully digital logic
  - Digital sum and trigger generation for calorimeter / scintillators
- Drawbacks
  - need fully pilelined to take full advantage of DAQ
  - L1A latency of 2 us

- Possibilty to use as regular ADC with look back in time

(No more delay lines)

Pipelined electronics

- JLAB FADC 250
  - Flash ADC 12 bit 250 MHz 16 channels
  - VXS option for summing and triggering purpose
- Jlab F1 TDC
- CAEN V1190
- CAEN V1290
- APV25 GEM readout : 40 MHz

- DAQ group will handle event repacking from the block of events

Fastbus

- Large amount of channels available
- Will be used for SuperBigBite
- Drawback no pipelining/ event blocking
- 20 Mb/seconds transfer rate
- Sufficient for low rate experiments
- Might benefit from new Intel VME CPU

L3 Farm

- For data reduction for SoLID maybe SBS
- Do treatment of event for data reduction : expect factor of 5 reduction of data amount
- Need to implement test bench
  - Choose algorithms : coarse reconstruction, look up table, coincidence between detectors to optimize speed and data reduction
  - Determine efficiency and systematical effects

Summary

- HRS DAQ upgrade ongoing by stage
- Support legacy electronics while allowing fully pipelined operation
- New electronics being tested in different setups
- Availability of 100 KHz rate capabilities for future experiments
- HRS upgrade is building block of DAQ for future large experiment SBS and SoLID