

Nuclear Physics Division

# Description and Technical Information for the VXS-based Electron Trigger and Readout Card (VETROC)

Updated on: Jan. 14th, 2014

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# 1 Introduction

The VETROC (VXS-based Electron Trigger and ReadOut Card) is being designed for HallA Compton Polarimeter (Robert Michaels, Alexandre Camsonne, and Sirish Nanda: VETROC for Hall A Compton). The electron detector is a 4-plane silicon microstrip detector with 192 (8x24) strips per plane.

This is a replacement for the original ETROC board. The front panel input connectors match with the current cable, which is 0.1” 50-pin dual-row connectors.

This board can also be used as a generic IO board. The 96 channels of differential signals are converted into LVTTL, and connected to the FPGA. The FPGA supplies two independent MGT (MultiGigabit Transceivers) paths. One path (with 4 MGT transceivers) connects to VXS switch slot#A backplane, and the other path (with 4 MGT transceivers) connects to QSFP (Quad Small Formfactor Pluggable) on the front panel.

This board has the optional TI (Trigger Interface) interface (depending on the firmware implementation and front panel space allocation). It can be used to drive a TI board or receive from a TI board.

# 2 PCB design of the VETROC module

VETROC is designed as a VXS payload board. It also works in a standard 6U VME64 crate. It is used for the trigger and readout. Figure 1 is the VETROC diagram.



The Xilinx Artix-7 XC7A200T-FFG1156 FPGA is chosen for signal processing. It is less expensive, and it has enough IO and resources for signal processing. The Micron JS28F256P30B parallel NOR flash embedded memory is used to save the FPGA configure data.

Four sets of 24-pair differential signals are received using two 3M 3433-D302 condo connectors. The signals are converted to LVTTL on the PCB by TI SN65LVDT352, which translates any differential signals (LVDS, LVPECL, ECL) to LVTTL. Because of the LVTTL translation, it is better to keep the signal at 100 MHz or lower. (An upper limit can be obtained by the PCB test). The connector should be compatible with the current microstrip detector front end electronics output.

A set of four LEDs is used to indicate the board status, which is directly from the FPGA. The LEDs could be ‘board ready’, ‘VME DTACK’, ‘Trigger’ and ‘Board error/Reset’.

Because of the limitation on the front panel space, one 3M 3408-D302 connector (option one) or two QSFP connectors (option two) can be loaded. It is possible to load the 3M connector from the bottom, then trim the pins level to the top side of the PCB, and load the QSFP on the TOP side. This will require a double width front panel. The usefulness of loading both options may not worth the effort.

The option one (3M 3408-D302 connector) has 8 generic differential signal inputs, and 8 ECL output, which are connected to the FPGA through TI SN65LVDT352 receiver and On-Semi MC100EP91 driver respectively.

The option two (two QSFP connectors) has 4 MGT (Multi-Gigabit Transceivers) connected to the FPGA directly on one QSFP, and a Trigger Interface (TI) compatible set of signals on the other QSFP.

The VME64x is implemented, which uses the Geographic address and +3.3V supply. The board is compatible with standard VME64 backplane. If the board is plugged in the VME64 crate, the onboard DC-DC converter can be used to get the +3.3V power from the +5 supply. Five bits of the on-board switch are used to set the A24 (A23-A19) address space.

The VXS P0 connector are used to send the channel ‘HIT’ information to Crate Trigger Processor (CTP in Swich slot#A), and get the readout information from the Signal Distribution board (SD in Switch slot#B).

# 3 Functional Descriptions

**3.1 FPGA programming**

The FPGA XC7A200T needs about 80Mbit to configure. This configure data is saved in the Micron JS28F256P30B, which is 256 Mbit. The memory can save two versions of the FPGA configure file. This can supply a fall back design, which is especially useful when the board is used in an area that is difficult to access.

The FPGA is programmed in Master BPI mode with external clock of 33MHz and 16-bit wide data loading. The expected FPGA program time is about 150 ms. The Micron memory can be loaded by the iMPACT software through the on-board JTAG connector. The iMPACT software will load a special firmware to the FPGA through the JTAG connector and program the memory through the special firmware.

A VME Memory loading interface can be implemented in the FPGA firmware. If so, the Memory (and the FPGA) can be reloaded remotely if the FPGA is working.

To make it more robust for remote programming, a hardware (discrete logic) VME to JTAG engine is implemented on the board (copied from TS/TI/TD design) using the custom defined address modifier code (AM = 19), which will not get confused with the standard (VME specified) A24 address modifier codes. This engine can load the FPGA firmware even if the memory is corrupted (or simply, the memory is empty) and the FPGA can not be loaded by the memory. The engine has been tested on TI to load the Xilinx PROM successfully. It should be able to load the FPGA. In the JTAG engine, the VME data bit[1] is used for TDI, bit[0] is used for TMS, and all the other bits are unused. The higher bit of A24 address should match with the geographic address, and the lower A24 address is set to be 0x0FFFC.

**3.2: Clock Distribution**

There are three main clock sources for the PCB. As a VXS payload board, it gets the clock (250 MHz) via VXS P0 backplane from SD/TI board. For the test or application without the VXS crate, an on-board oscillator (250MHz) is implemented. The third source is the optional front panel TI fiber. Only one clock source is selected as the FPGA clock, which pipelines the trigger and readout logic. The clock source is set by two bits of the on board switch. This switch can be overwritten by the FPGA software.

The FPGA should receive the 250MHz clock and distribute to the MGT blocks. The FPGA PLL should clean up the clock before being used as the MGT reference clock. This will ensure the low clock jitter and phase alignment across the system (within the crate, and across the crates).

**3.3 Trigger logic**

The four sets of 24-channel detector signals are received as LVTTL to reduce the IO usage on the FPGA. TI SN65LVDT352 is the receiver, which accepts almost any differential signals (LVDS, LVPECL, ECL etc.). The 96 signals will be processed in the FPGA.

The simplest processing will be to find the HIT signals on these channels and send the HIT information to CTP via VXS P0 connector.

If the four sets of the inputs are aligned (detector positional alignment), the board can perform some track finding logic. In this case, the generic IO connector can be used to connect to the ‘right’ and ‘left’ of the detector for track overlap. If the number of overlapping channels is large, the QSFP option can be used, which can pack in more channels than the generic IO connector. The track segment can be sent to the CTP or even the SSP directly.

**3.4 VME interface**

The VETROC board is a VXS payload slot board. It is compatible with VME64x backplane. Normally, it is a VME slave board, with interrupt capability.

The VETROC can also be a master VME board. It supports single level bus request (BR3, level 3) only, as we do not expect many boards to be a VME master in the crate. The VME master capability has not been tested yet.

For simplicity, three kinds of VME address modifier codes are implemented. (1), User defined address modifier. (0x19,0x1A, 0x1C and 0x1D) This is similar to the A24 address modifier. It is used to load the FPGA by the onboard discrete logic (also called emergency JTAG engine). (2), Standard A24 address modifier. This is used to readout the registers on the FPGA, slow controls of the board. (3), A32 data transfer. This is used to transfer data to the ROC (Read Out Controller). This is implemented the same way as other ADC/TDC board, so the ROC needs only one read to get all the front end boards’ data out for higher efficiency.

**3.5: Readout logic**

The readout is initiated by the readout trigger from TI via SD and VXS P0 backplane. The channel HIT information (which channel, what time) can be readout via VME A32. The readout logic can be borrowed from other projects. The readout trigger can be used as time\_0 for the channel hit information if the resolution requirement is less than 4ns.

# 4. Specification Sheet

**4.1 Mechanical**

* Single width VITA 41 Payload Module. It will be positioned in PP2-PP16 in VXS crate; it can also be plugged into any slots in standard VME crates without VXS.

**4.2 High speed serial P0 inputs and outputs:**

* Switch slot#A (CTP) four lane MGT connections
* Switch slot#B (SD) compatible connections.

**4.3 Front panel inputs and outputs:**

* 4 x 24 LVDS detector inputs;
* 8 generic differential signal inputs;
* 8 generic ECL outputs.
* In lieu of 8 generic IO, 4 channels of MGT on one QSFP, TI or TImaster fiber IO on the other QSFP.

**4.4 LED Indicators: Front Panel (**FPGA controlled**):**

* Bit 1 (close to the PCB): FPGA programmed and the clock (DCM locked) is ready;
* Bit 2: VME DTACK, VME activity;
* Bit 3: Readout trigger is detected;
* Bit 4: MGT Rx error;

**On board:**

* Power OK near each regulator and DC-DC converter (The LED is OFF when the power is OK);
* FPGA program DONE (The LED is OFF when programmed);

**4.5 Programming:**

* VME to JTAG A24D32 with user defined AM (Address Modifier) for remote FPGA firmware loading.
* onboard JTAG connector to FPGA;
* Custom VME to Micron memory engine will be implemented in the FPGA using A24D32 for memory loading (FPGA firmware);
* Up to two revisions of the FPGA firmware can be stored in the memory simultaneously.

**4.8 Power requirements:**

* +5v @ 1 Amps; -12V @ 0.25 Amp; +3.3V @ 2 Amps
* With Optional DC-DC converters for +3.3V, +5V @ 3A, +3.3V is not required from backplane.
* Local regulators for other required voltages: +1.0V, +1.2V, +1.8V, +2.5V, and -5V.

4.9 Environment:

* Forced air cooling;
* Commercial grade components ( 0-75 Celsius or better)

# 5 VETROC operation procedures:

The VETROC needs to be properly set, and plugged into the proper crate and slot. Damage may happen to the VETROC, the crate, or other PCBs in the crate if the right procedure is not followed.

5.1 VETROC Power supply:

The VETROC can use +3.3V directly from VME64x crate. It can also generate its own +3.3V supply by a DC-DC converter. Proper settings are needed to avoid damage to the board or backplane.

If the VME64x crate +3.3V power is used for the VETROC:

(1). The fuse, FG1 is stuffed;

(2). The DC-DC converter UP2 is removed.

If the VME64x crate +3.3V power is not used, or +3.3V is not available from the backplane:

(1). The fuse, FG1 is removed;

(2). The UP2 is stuffed.

The default setting for the VETROC is assuming that there is no +3.3V from the backplane.

* 1. FPGA program mode setting:

The FPGA program can be set to MasterBPI mode or JTAG mode. For MasterBPI mode:

(1). Remove RBJ2 and RBJ3;

(2). Load RBJ1 and RBJ4.

For JTAG mode:

(1). Remove RBJ1 and RBJ4;

(2). Load RBJ2 and RBJ3.

5.3 Local trigger and SD link:

The VETROC can send the local trigger information (for example: a track segment) to the SD. The source could be a standard FPGA LVDS IO pad, or a MGT high speed differential PAD. (VXS P0 pin#D15/E15)

For LVPECL driver (driven by FPGA LVDS pad):

(1). Remove CGT1 and CGT2;

(2). Load RS01 and RS02.

For MGT high speed driver:

(1). Remove RS01 and RS02;

(2). Load CGT1 and CGT2.

The VETROC can also receive from SD. The receiver could be a standard FPGA LVDS IO pad, or a MGT high speed differential PAD. (VXS P0 pin#A15/B15)

For LVPECL signal driver (driven by FPGA LVDS pad):

(1). Remove RS07 and RS08;

(2). Load RS03 and RS04.

For MGT high speed receiver: (it is a receiver, not driver)

(1). Remove RS03 and RS04;

(2). Load RS07 and RS08.

5.4 VETROC 8-bit switch S2 setting:

Bit[8:4]: set the VME A24 address space A[23:19] when the VETROC is in non-VME64x crate. If it is in VME64x crate, the geographic address is used, the switch is not used.

Bit[2:1]: Clock select. This can be overwritten by the FPGA (software):

(1). 00: TI/SD clock from VXS P0 backplane;

(2). 01: Front panel TI clock;

(3). 10: no clock;

(4). 11: onboard oscillator;

5.5 VME to JTAG discrete logic:

For standard A24 address modifier (0x39 etc.), load RB41 and remove RB42; For user defined address modifier (0x19 etc.), load RB42 and remove RB41.

6. VME Programming Requirements (This part will be updated as the firmware develops)

The VETROC supports three categories of Address Modifier codes: the user-defined codes (A24) for emergency firmware loading; Standard A24 for FPGA register read/write and slow control; A32 block transfer for VME data readout.

6.1 VME to JTAG emergency loading:

The AM[5:0] user defined codes are used for this logic. This works even before the FPGA is programmed and working. It is almost the same as A24D32 mode. The valid AM codes are: 0x19, 0x1A, 0x1D and 0x1E. These AM codes are user defined, and similar to the AM codes 0x39, 0x3A, 0x3D and 0x3E.

The valid address bits are A[31:24] do not care; A[23:19]=GA[4:0] for VME64x crates, or A[23:19]=0 for non-VME64x crates; A[18:2]=b’00011111111111111.

VME Data bit[1] is TDI; VME data bit[0] is TMS.

For example, if the board is in slot#5 (that is ~GA(4:0)= 11010), you need write to A(23:0)=0x28fffc. If data(1:0)=00, both TMS and TDI will be low; if data(1:0)=01, TMS is high, TDI is low; if data(1:0)=10, TMS is low, TDI is high; if data(1:0)=11, both TDI and TMS are high. The normal A24 address should try to avoid this address (0x0fffc).

A more advanced example: Instruction register shift (8-bit, shift in 0x5a) starting from/end up at the ‘reset idle’ mode: 14 consecutive writes to the address 0x28fffc with AM=0x19, 1a, 1d or 1e, the data are 1, 1, 0, 0, 0, 2, 0, 2, 2, 0, 2, 1, 1, 0 respectively.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Data | 1 | 1 | 0 | 0 | 0 | 2 | 0 | 2 | 2 | 0 | 2 | 1 | 1 | 0 |
| TMS | H | H | L | L | L | L | L | L | L | L | L | H | H | L |
| TDI | 0x | 0x | 0x | 0x | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0x | 0x |

* “TMS H” means logic High, “TMS L” means logic Low, “TDI 0” means 0 or Low, “TDI 1” means 1 or High, and “TDI 0x” means DO NOT CARE by the JTAG, but the set value is 0.

6.2 Configuration Registers:

A24D32 are used for register read/write. Similar to the emergency loading logic, the base address is determined by the Geographic Address in VME64x crate, and external switch for non-VME64x crate. That is, A[23:19]=GA[4:0], or SW[8:4].

* Address offset: 0x00000: Board ID:

Bit 7-0 (R/W): Crate ID; Reset default 0x00;

Bit 12-8 (R): A24 address, higher 5 bits; Reset default 000

Bit 23-16 (R): PCB related setting, 0x01: production board, 0x00; prototype board;

Bit 31-24 (R): Board type: 0x71: TI, 0x75: TS, 0x7D: TD, 0x??: VETROC.

6.3 VME data acquisition:

For data acquisition, the A32 block reads are used. The base address is set by the upper 9 bits of A24 register 0x00010, that is A[31:23] = RegData[31:23] of A24=0x00010.

7 Pin out tables:

7.1 VXS P0 Pinout Table

|  |
| --- |
| Payload slot#18, TI or TImaster |
| Pin name | Signal Description | Signal Level | Direction |
| DP1 (A1+, B1-) | CTPRX1 |  | 🡨 SWA |
| DP2 (D1+, E1-) | CTPTX1 |  | 🡪 SWA |
| DP3 (B2+, C2-) | CTPRX2 |  | 🡨 SWA |
| DP4 (E2+, F2-) | CTPTX2 |  | 🡪 SWA |
| DP5 (A3+, B3-) | CTPRX3 |  | 🡨 SWA |
| DP6 (D3+, E3-) | CTPTX3 |  | 🡪 SWA |
| DP7 (B4+, C4-) | CTPRX4 |  | 🡨 SWA |
| DP8 (E4+, F4-) | CTPTX4 |  | 🡪 SWA |
| SE1 (G1) | STAT\_OUT | LVTTL (+3.3V) | 🡪 SWA |
| SE2 (G3) | STAT\_IN | LVTTL (+3.3V)  | 🡨 SWA |
| DP23 (B12+, C12-) | Readout TRIGGER | LVPECL(DP) | 🡨 SWB |
| DP24 (E12+, F12-) | SYNC | LVPECL(DP) | 🡨 SWB |
| DP25 (A13+,B13-) | CLOCK | LVPECL(DP) | 🡨 SWB |
| DP26 (D13+, E13-) | Trigger2 | LVPECL(DP) | 🡨 SWB |
| DP27 (B14+, C14-) | TOKEN\_IN | LVPECL(DP) | 🡨 SWB |
| DP28 (E14+, F14-) | TOKEN\_OUT | LVPECL(DP) | 🡪 SWB |
| DP29 (A15+,B15-) | SD\_Link | LVDS/MGT | 🡨 SWB |
| DP30 (D15+,E15-) | TrigOut | LVPECL/MGT | 🡪 SWB |
| SE7 (G13) | Busy\_Out | LVTTL  | 🡪 SWB |
| SE8 (G15) | Stat\_IN | LVTTL  | 🡨 SWB |

##### Appendix D: Document revision history:

Initial document: Jan. 13, 2014;