Hall A 12 GeV DAQ Upgrade

Robert Michaels, Alexandre Camsonne,
Jack Segal, Dave Abbott

Thomas Jefferson National Accelerator Facility

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I INTRODUCTION

The 12 GeV upgrade plan includes possible funding for an upgrade of the Hall A HRS DAQ. There are two themes to this upgrade: 1) Replace obsolete components, and 2) Achieve a much higher DAQ rate using full pipelining, possibly 200 kHz with practically zero deadtime. Such a rate increase could open the door to a number of new experiments. The higher rate is achievable for two primary reasons: 1) The frontend digitizers have a pipeline (large buffer) and minimal conversion processing time ($\leq 5\mu$sec); and 2) The frontends will support blocking of events and a new trigger distribution system (TS) will block trigger data. This anticipated higher speed still needs to be demonstrated in a test stand.

This document describes the result of our project engineering (PED) effort. Section II describes the existing system and section III outlines the upgrade design, while section IV provides an estimate of the costs and the timescale.

II DESCRIPTION OF EXISTING HALL A DAQ

The data-acquisition (DAQ) systems in Hall A use CODA (CEBAF On-line Data Acquisition System) developed by the JLab Data Acquisition group.

The hardware elements include commercial front-end Fastbus and VME digitization devices (ADCs, TDCs, scalers), the Struck Fastbus Interface (a VME interface to Fastbus), single-board VME computers, Ethernet networks

(100 Mbit at the frontend), Unix or Linux workstations, and a mass storage tape silo (MSS) for long-term data storage. Custom hardware elements made at JLab include the trigger supervisor which synchronizes the read-out of the front-end crates and handles the dead-time logic of the system, as well as interface cards for the Fastbus and VME crates which facilitate communication between the trigger supervisor and the front-end crates. CODA also includes a number of custom software components, like the event builder, etc. Because of the modular nature of CODA and its emphasis on commercially available components, data-acquisition systems can be built and reconfigured rapidly.

The present DAQ is shown schematically in fig 1. On each HRS we have two Fastbus crates which are nearly full. They contain TDCs (obsolete LeCroy models 1877 and 1875) and ADCs (1881M). In addition, each HRS DAQ has a VME crate with scalers primarily and some miscellaneous I/O. Various third-arm spectrometers are deployed for different experiments. For example, the BigBite DAQ has three Fastbus crates with mostly 1877 and a few 1881M, and two VME crates with CAEN TDCs and a third VME crate with F1 TDCs. Other major third-arm systems have been the RCS calorimeter, the DVCS detector system, and the BigHand detector.

The typical performance for a 2 kHz trigger rate results in a $\sim 20\%$ dead time in coincidence mode. If compromises are made, as appropriate for some experiments, e.g. drop the slow TDC 1875 modules, the speed can be approximately doubled. We believe we can improve the rate capability to ~ 200 kHz with the future design (next section).

The trigger system is built from commercial CAMAC and NIM discriminators, delay units, logic units, and memory lookup units (MLU). The primary trigger is formed from a coincidence between scintillator detector planes. Sometimes other detectors, e.g. gas Čerenkov detectors, are involved in forming various types of triggers. The trigger modules are remotely programmed by CAMAC commands sent from a software control package. The electronic deadtime is measured with a custom-made pulsing system that adds signals to the PMT pulses.

One major concern with the current system is that both the DAQ and the trigger contain many hardware elements which are obsolete and would be difficult if not impossible to repair or replace in case of failures. In the next section we identify replacement components.

III 12 GEV UPGRADE PLAN

We need to replace all our Fastbus and CAMAC modules. For the Fastbus, the present plan is to use the JLab-built VME-based F1-TDCs and FADCs, or suitable commercial units. These also have the important upgrade potential of allowing pipelining and higher rates. Some commercially available VME units might become competitive, in particular TDCs and FADCs from CAEN, and the FADCs from SISGmbH. The F1-TDC can be run in either a low-resolution mode (120 psec) or high-resolution mode (60 psec); the former is a replacement for the model 1877 Fastbus TDC, and the latter replaces the 1875. The JLab-FADC will be a replacement for the 1881M ADC. This FADC will be a 250MHz 12 bit unit. We might need preamps and shaping to get the resolution. In the next few years, we will be using the JLab-built units as well as commercial VME units in various setups, e.g. BigBite and Compton. The experience will help us evaluate what is best for the future.

To take full advantage of faster frond-end readout we will also need VME64X crates, Gigabit ethernet, and a new Trigger and Clock Distribution System that is being designed by the DAQ group. The frontend VME cpus will need to be fast (supporting higher VME transfer modes, 2eVME and 2eSST), multicore, and have Gigabit ethernet, and will have the option of using embedded Linux.

We also need to replace our CAMAC trigger modules with NIM and VME based electronics. It is doubtful that CAMAC has much of a future. However, we will keep one CAMAC crate in each HRS with "legacy" modules. This will house our EDTM system and we will make available CAMAC delay and discriminators that may still exist. The strategy is to eliminate our reliance on CAMAC, but we can still use the existing modules where convenient.

Our quantity of CAMAC spare modules is dangerously low and the modules are either difficult or impossible to fix since they are based on obsolete components. Note, the danger is not quite as bad with Fastbus because we've obtained a large supply of excessed material from other labs, so as the old modules go bad they can be swapped out. This strategy should help us survive the next few years with Fastbus.

IV ESTIMATES OF COST AND TIME

We have identified replacement items for all the trigger modules if we had to buy them "tomorrow", see table 1. A notable exception is the programmable delay (LeCroy model 4518), for which there is no currently available commercial replacement. Therefore we have requested the JLab electronics group to build a programmable delay module in VME format with the same features (plus small improvements) over the existing ones. A specification has been written and Chris Cuevas's group has accepted responsibility for building this delay unit.

Figure 3 is a possible schematic of our future trigger and fig 2 shows the future DAQ layout. Table 1 is a snapshot of what's available now on the market, and it is somewhat uncertain how this will change in the next few years. Also in table 1 is an estimate of the costs for upgrading the HRS DAQ and trigger. The rough estimate of the total cost is 833 K$.

The schedule is somewhat flexible. Since the greatest danger we face is our obsolete CAMAC, we could upgrade the trigger first (38 k$ per HRS) starting with one HRS. To spread the cost over time, we could replace a few items at a time. We will need a test area of about $3 \times 3m^2$ ($\sim 10' \times 10'$) to test the trigger/DAQ. This will minimize downtime and check the less-certain items before making a major financial commitment. Table 2 is a schedule suggested for discussion.

V APPENDIX – EXPERIENCE FROM HALL B

Experience from the Hall B upgrade (Sergey Boyarinov) may be relevant. They have replaced their 1872 and 1875A TDCs with CAEN 1180 and 1290. This alone has led to an improvement in speed because the 1872/75A are the slowest of the fastbus modules. Hall B also plans to use the JLab-built FADC to replace the 1881M. Hall B has also made software improvements to their readout and to the event builder which improves the buffering. Where applicable, these improvements are being incorporated into CODA version 3 and will benefit Hall A when we upgrade our frontend hardware. CODA 3 will be available on the timescale of this upgrade.

TABLE 1. HRS DAQ and Trigger 12 GeV Upgrade

Item	Replacement	Num. Units	Cost Each (K$)
DAQ			
TDC 1877 (0.5 nsec)	F1 TDC or CAEN 1190	80	4
TDC 1875 (0.05 nsec)	F1 TDC or CAEN 1190 or 1290A	8	4
ADC 1881M	JLab FADC, STR3320, or CAEN1720	50	5
Crates	Wiener or CAEN 64x	6 (have 2)	8
VME cpus	Motorola	6	5
Trig. Supervisor	JLab electronics	1	5
Distribution Module	JLab electronics	1	5
Trig. Interface	JLab electronics	8	2
Fiber Cable			10
Gigabit Ethernet			25
Trigger			
LeCroy 4518 delay	JLab custom delay	10	2
LeCroy 4413 discr	Phillips 706 or CAEN 895	10	1.5
LeCroy 4516 logic	Phillips 758, 756, 757	22 (tot)	1.5
LeCroy 2373 MLU	CAEN V1495	6	4
TOTAL COST			833 K$

TABLE 2. Possible Timeline for DAQ/Trigger Upgrade

Time (years)	Task	Cost (K$)
0	purchase trigger	75
0.5	trigger test stand	
0.7	deploy trigger	
1	purchase most F1TDC for 1 HRS	120
1	purchase some crates and cpus	43
1	purchase a couple FADCs	10
1	trigger distrib. system and fiber	36
1.5	F1TDC/FADC test stand	
1.7	deploy F1TDC for 1 HRS	
2	purchase remaining F1TDC	200
1	purchase remaining crates and cpus	30
3	purchase hi-res TDCs	32
3	partial purchase FADCs	68
3.5	test stand hi-res TDCs	
3.7	deploy hi-res TDCs, FADCs	
4 & 5	purchase remaining equipment	219

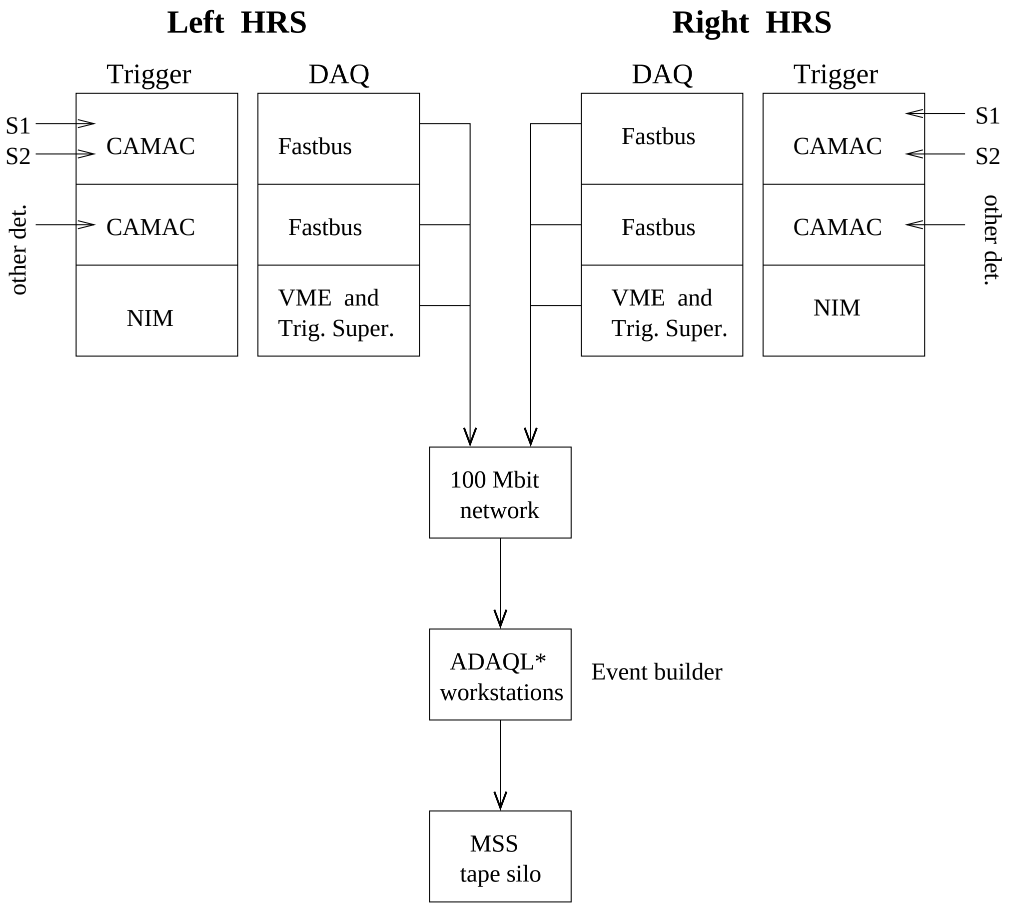

FIGURE 1. Overview Schematic of Present DAQ/Trigger.

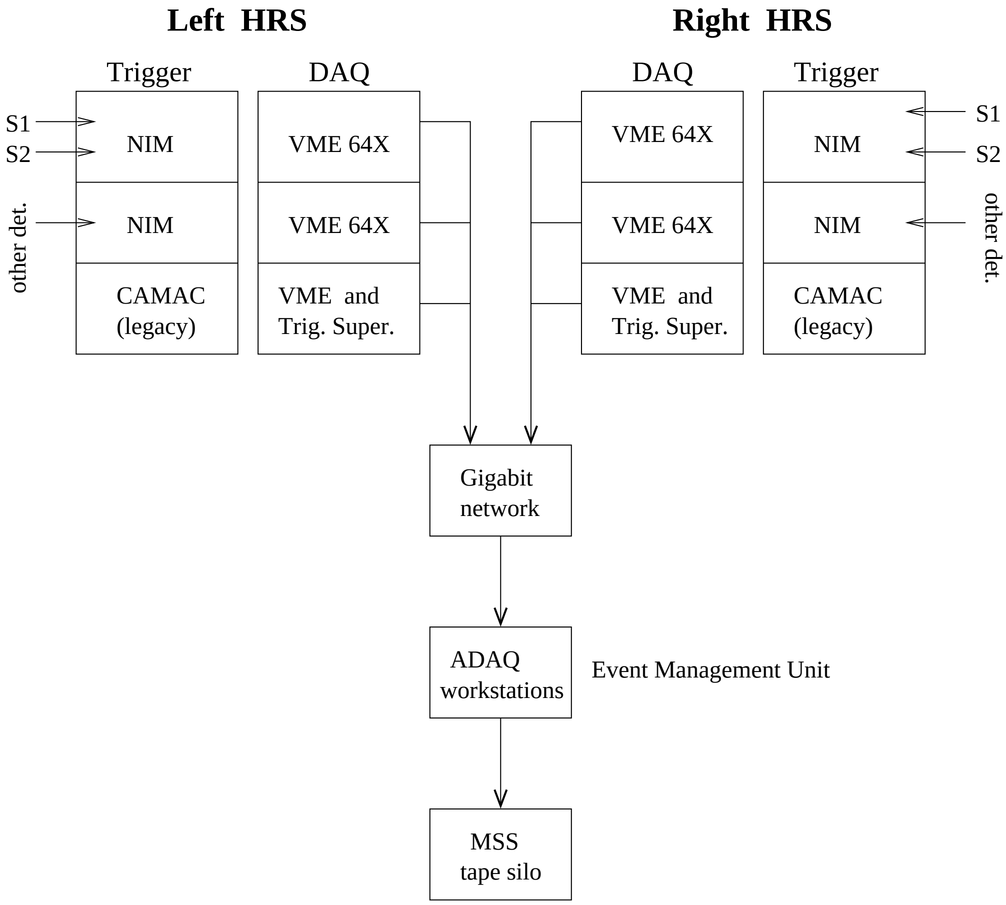

FIGURE 2. Schematic of 12 GeV DAQ/trigger.

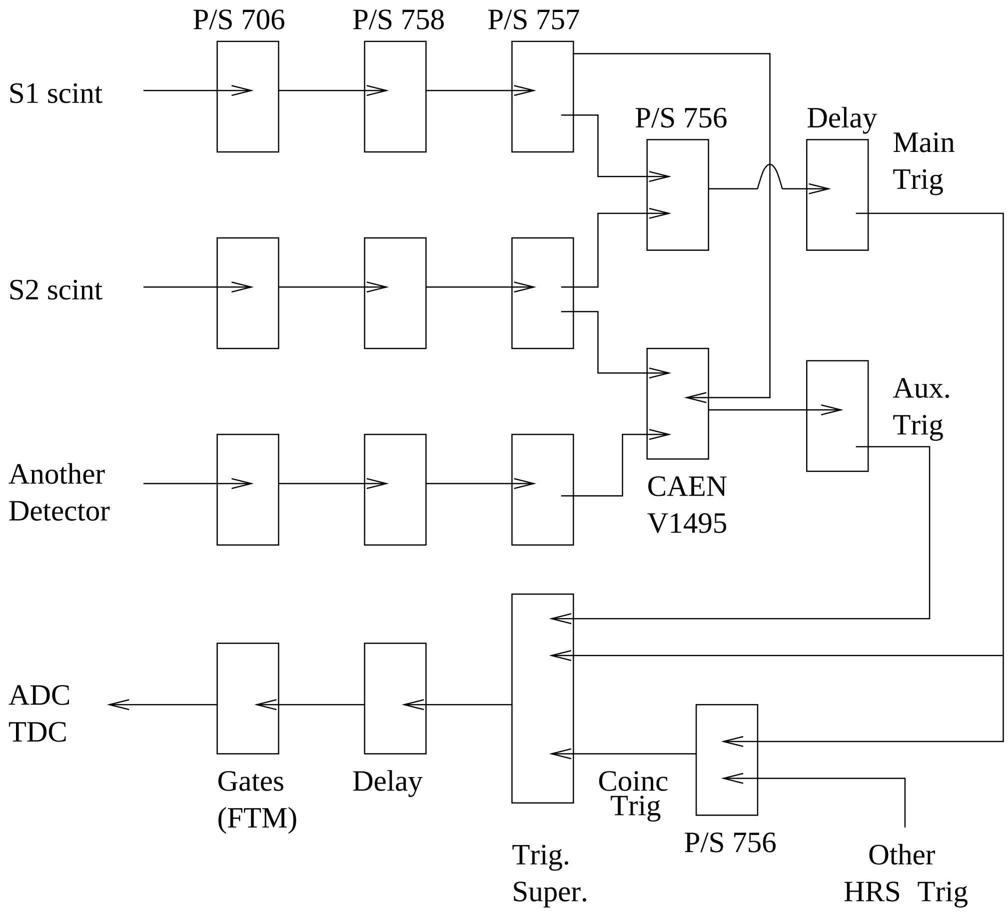

FIGURE 3. Schematic of 12 GeV Trigger using Phillips Modules (P/S) as an example.