Schematic of Electronics for Helicity Info in Hall A HRS during Qweak

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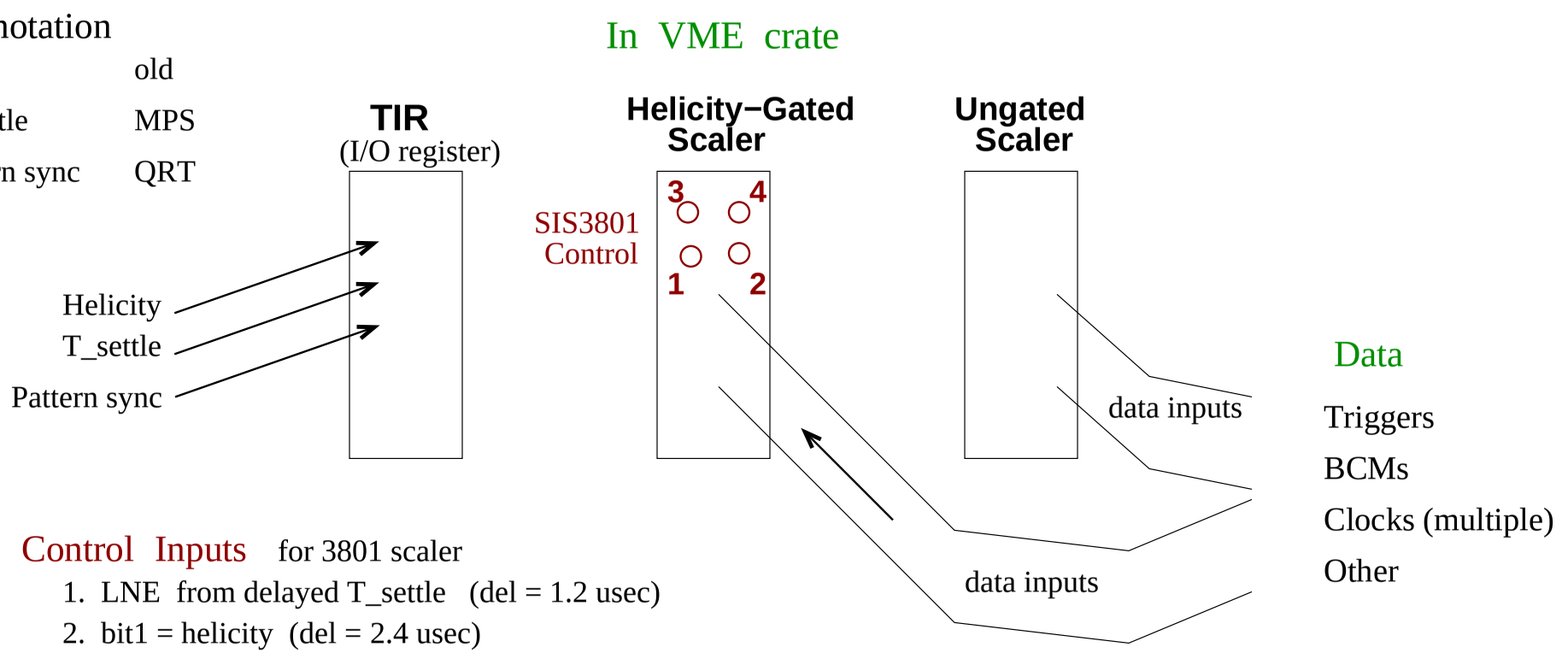
notation

new	old
T_settle	MPS
Pattern sync	QRT



Control Inputs for 3801 scaler

1. LNE from delayed T_settle (del = 1.2 usec)
2. bit1 = helicity (del = 2.4 usec)
3. bit2 = pattern sync (del = 2.4 usec)
4. Gate = T_settle with appro. polarity and undelayed. (TRUE disables counting)

At frequency "f" (f = 1 kHz normally) we must:

1. Read helicity−gated scaler with zero deadtime.
2. Keep a queue in memory of the cpu of [helicity, pattern sync, and clock(s)]
3. Sort the plus and minus helicity, adding the data to "virtual" scalers for online consumption.
4. Check data for errors. Issue warnings.

For each trigger accepted by Trigger Supervisor, we must:

1. Read the (a) TIR bits and (b) clocks from ungated scaler.
2. Flush the memory queue (see 2 above), to have full sequence of helicity data.