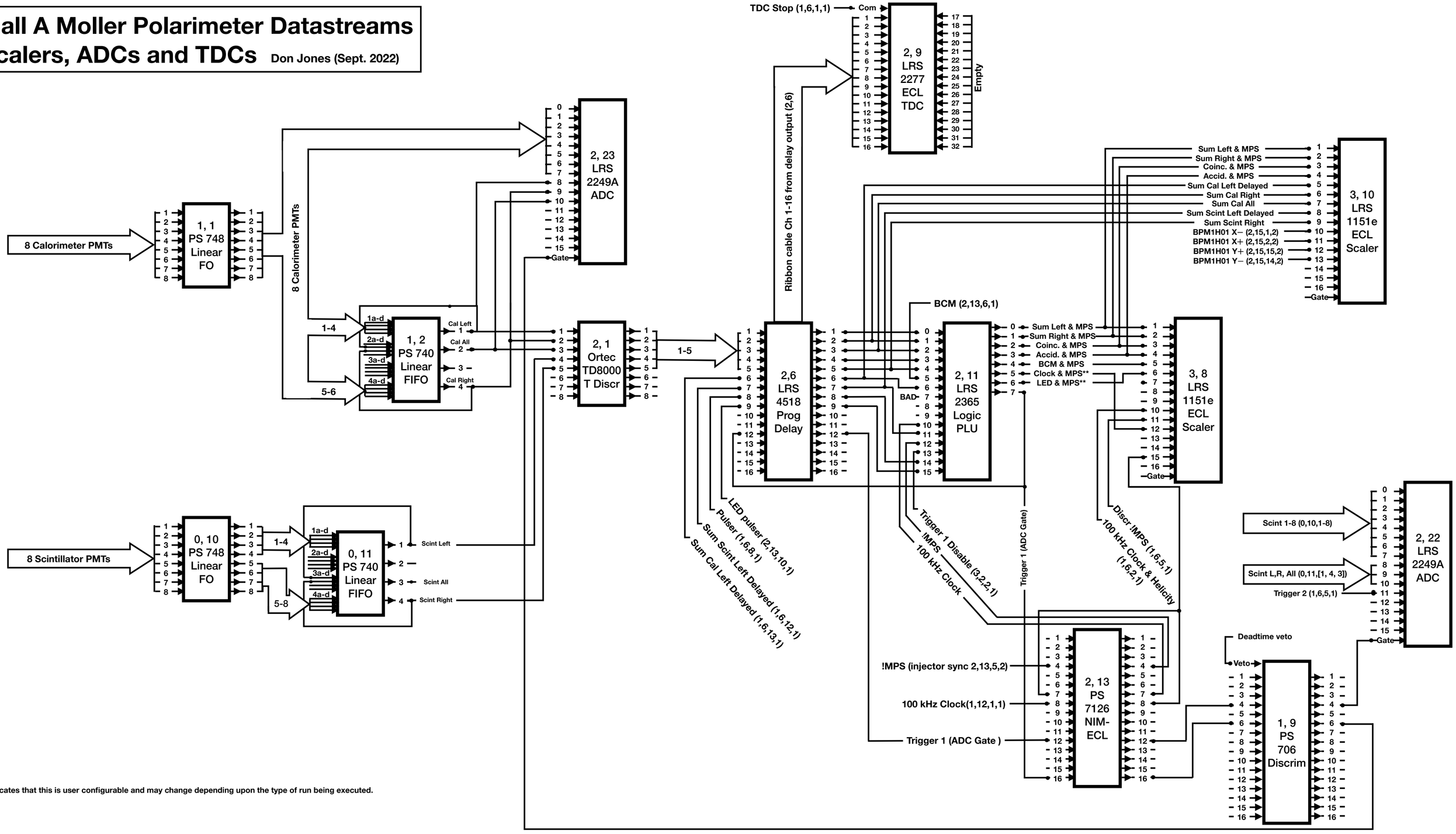
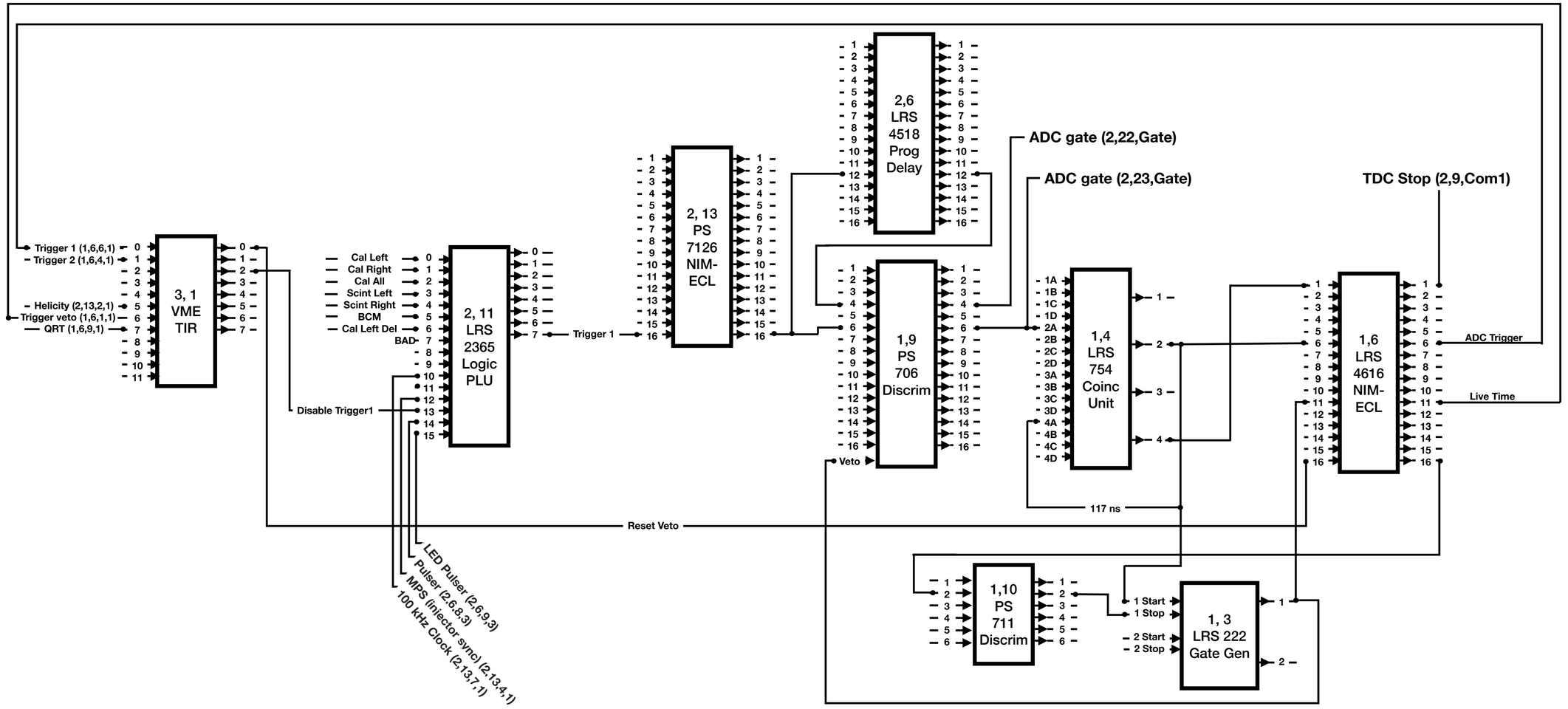
Hall A Moller Polarimeter Datastreams
Scalers, ADCs and TDCs

Don Jones (Sept. 2022)



**indicates that this is user configurable and may change depending upon the type of run being executed.

Trigger 1 (for ADC/TDC)



The ADC trigger starts with the PLU and is set with the logic for output 7. This is typically set to right PMT sum, left PMT sum, or Right-Left coincidence and is often OR'd with the Disable Trigger from the TI. This signal from PLU output 7, is transformed into NIM from ECL and sent to a discriminator that creates the logic signal for the ADC gate. The discriminator signal is further fanned out via a coincidence unit and copies sent to the TI (after transformation back to ECL) and also sent to the Start input of a gate generator which starts a veto signal to prevent further pile up events from firing the discriminator until the TI gives the clear signal. The TI sends out a veto reset signal to the Stop input of the gate generator when the ADC event has been processed.

Trigger 2 (Scaler gate)