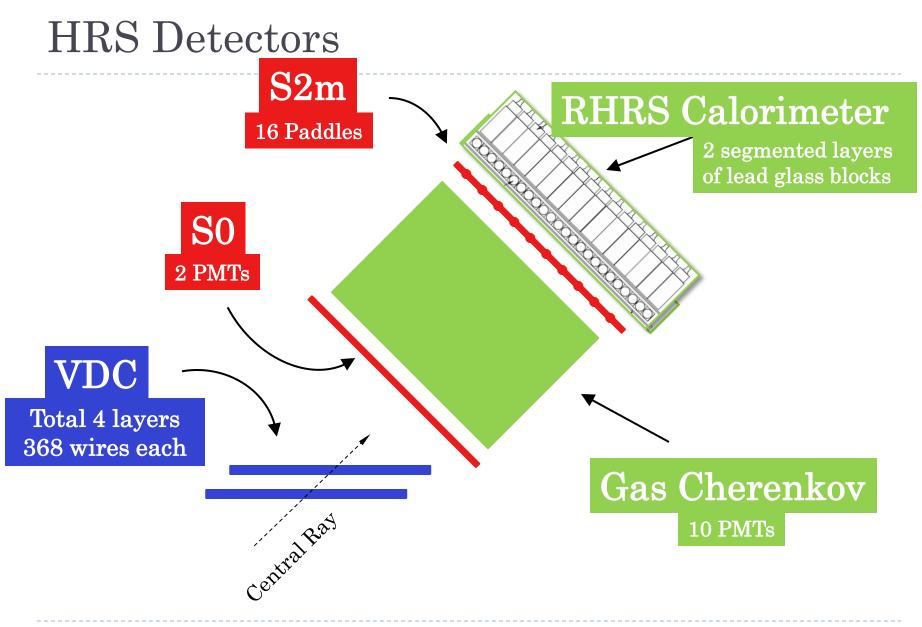
APEX Trigger and DAQ

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APEX collaboration

Overview

- Requirements
- Trigger improvements
- DAQ improvements
- Summary



Detector channels

Detector	Detector Channels	DAQ channels
Gas Cherenkov	10	10 time 10 amplitude
Scintillators	17	17 time 17 amplitude
Calorimeter	128 – RHRS 68 – LHRS	128 amplitude 68 amplitude
VDC	1472	1472 time

LHRS

112 amplitude channels – 2 ADC modules 1516 time channels – 16 TDC modules

RHRS

172 amplitude channels – 3 ADC modules 1516 time channels – 16 TDC modules

Trigger rate

Setting	Α	B	С	D
Energy (GeV)	2.2	4.4	1.1	3.3
e ⁻ (kHz)	4500	700	6000	2900
π - (kHz)	100	2200	36	1000
e ⁺ (kHz)	31	3.6	24	23
π^+ (kHz)	100	2200	36	1000

Possible Improvements

Trigger

- Reduce coincidence timing
 - Suppress pions

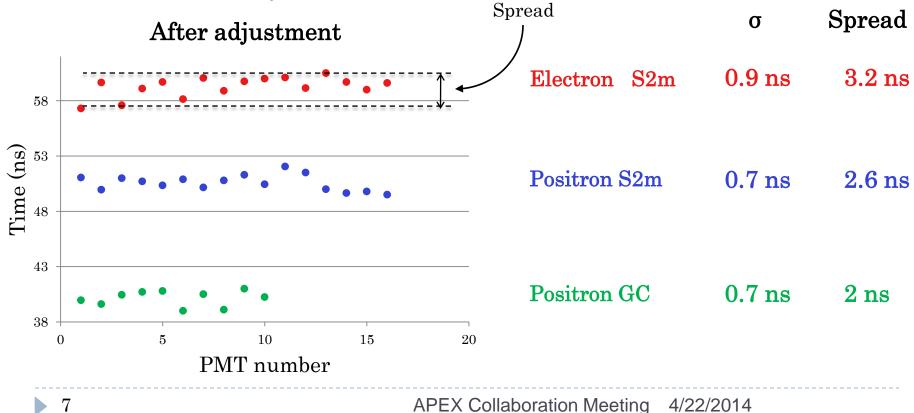
DAQUsing of sparsification

Trigger Logic

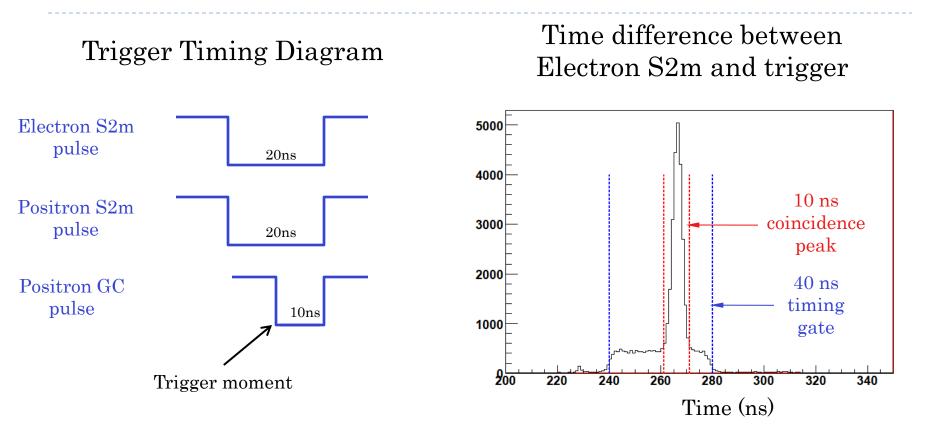
- Electron Arm Trigger (T1)
 - Electron S2m
- Positron Arm Trigger (T3)
 - Positron S2m
- Coincidence Trigger (T4)
 - Electron S2m + Positron S2m
- "Golden" Coincidence Trigger (T6)
 - Electron S2m + Positron S2m + Positron Gas Cherenkov

Timing Alignment in Hardware

- Run at high rates, small timing gate is important
- Must align timing of the trigger detectors
 - ▶ S0 counter as a reference
 - ▶ Inserted 1–5 ns delay cables



Coincidence Timing

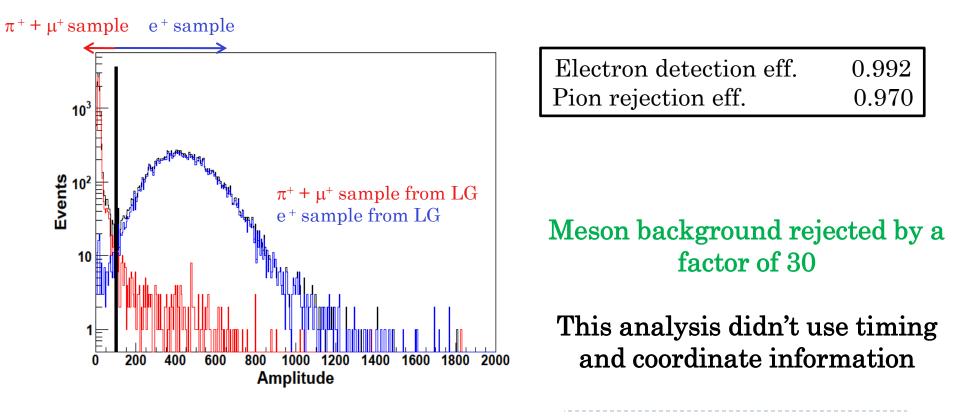


20 ns coincidence time easily achievable Ideally 10ns could be used

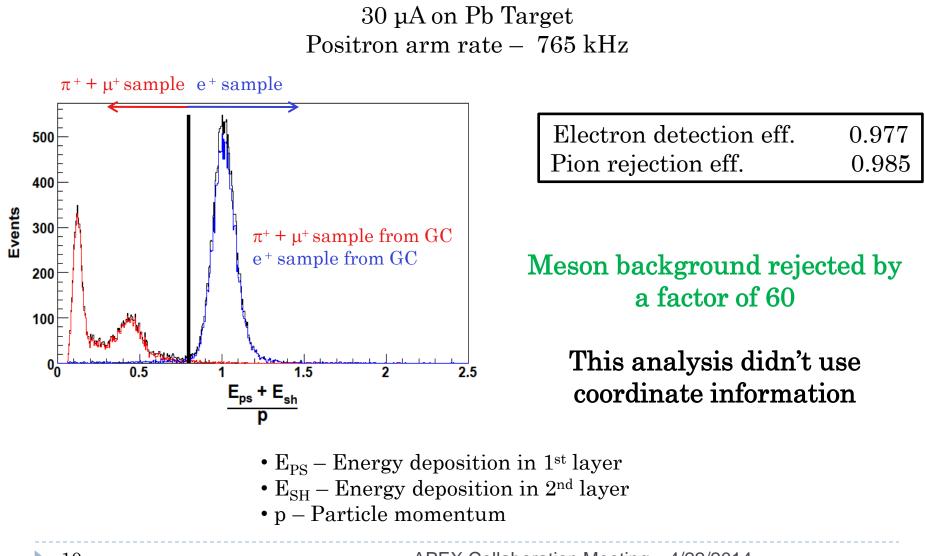
APEX Collaboration Meeting 4/22/2014

Gas Cherenkov in Positron Arm (high rate)

30 µA on Pb Target Positron arm rate – 765 kHz (close to maximum expected rate)



Lead Glass Particle ID in Positron Arm (high rate)



Trigger rate

Setting	Α	B	С	D
Energy (GeV)	2.2	4.4	1.1	3.3
e ⁻ (kHz)	4500	700	6000	2900
π ⁻ (kHz)	100	2200	36	1000
e ⁺ (kHz)	31	3.6	24	23
π^+ (kHz)	100	2200	36	1000
T6 rate (kHz) 20ns window	3.2	4.5	3.0	4.4
π^+ rejection = 30				

For 4 kHz DAQ dead time is 10% APEX can run without any improvement to DAQ!

3 Crate configuration

LHRS

112 amplitude channels – 2 ADC modules 1516 time channels – 16 TDC modules

RHRS

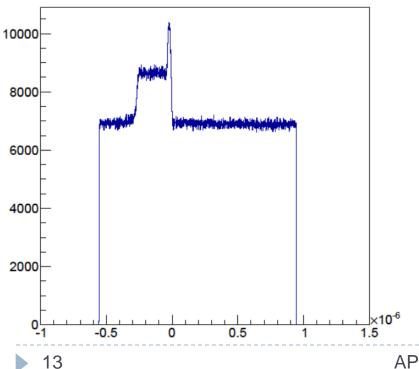
172 amplitude channels – 3 ADC modules 1516 time channels – 16 TDC modules

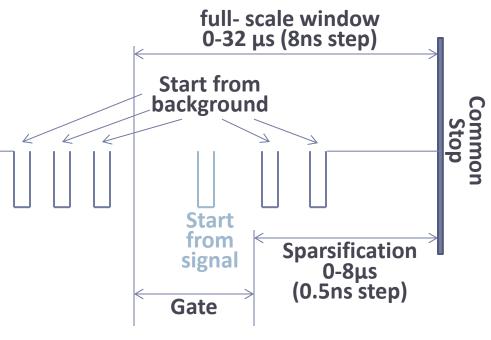
Crate 1: 5 TDC + 1 ADC Crate 2: 5 TDC + 1 ADC Crate 3: 6 TDC Crate 1: 5 TDC + 1 ADC Crate 2: 5 TDC + 1 ADC Crate 3: 6 TDC + 1 ADC

By reducing number of channels which go to each crate we reduce the amount of data to be recorded and improve dead time.

Sparsification

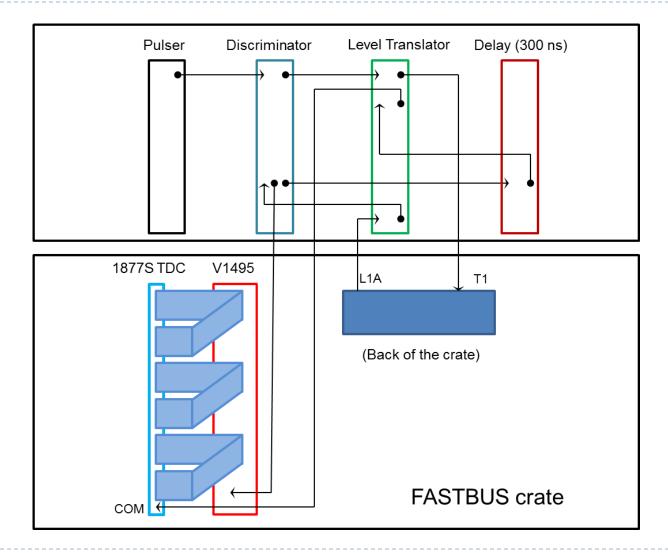
Typical TDC spectrum without sparsification. Only 300ns window out of 1.5µs full scale window has useful data





Enabling of sparsification allows to significantly reduce event size. All TDC modules have been tested to work in sparsification mode.

TDC test setup



TDC test procedure

Sparsification CRL #1

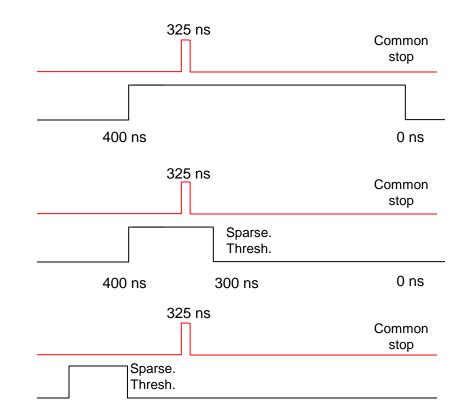
Full scale time window = 400 nsSparsification threshold = 0 ns

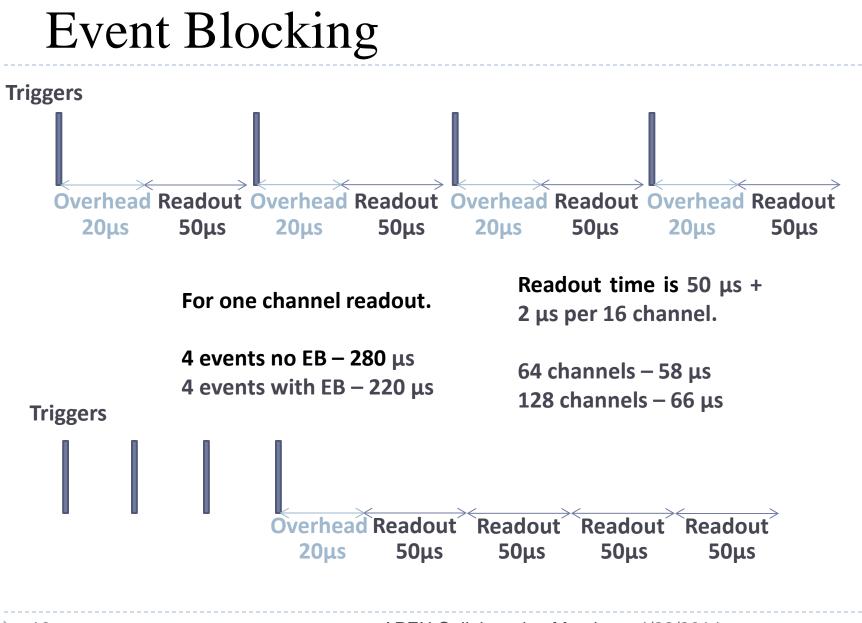
Sparsification CRL #2

Full scale time window = 400 ns Sparsification threshold = 300 ns

Sparsification CRL #3

Full scale time window = 496 ns Sparsification threshold = 424 ns





Event Blocking test results

20 kHz rate
New TI version 3
Linux CPU

Event Blocking	Number of channels	Number of modules	Life time (%)
1	1	1	71
4	1	1	90
1	64	3	65
4	64	3	80

Summary

- 20 ns coincidence window and factor 30 online pion rejection in Right HRS should be enough to keep DAQ rate under 4.5 kHz
- 10 ns window and factor 50 online rejection is not impossible

- DAQ can operate with 10% dead time at 4 kHz
- DAQ dead time can be improved by easy steps of implementing sparsification and using 3 crate configuration (both hardware and software are ready to use)
- Further improvement could be done by using event blocking