Design Specification for NIM-ECL Level Translator for PVDIS

Robert Michaels[1], Albert Shahinyan [2], Bogdan Wojtsekhowski[3] and Xiaochao Zheng[4]

March 12, 2007

This document describes the design specification for NIM-ECL level translators to be used in PVDIS (E05-007) DAQ test setup. The translator is expected to have no less than 16 channels per module, each channel converts one NIM/LEMO input to 4 ECL/flatcable outputs. The input are from the trigger electronics and the outputs are fed to TDCs and scalers.

For PVDIS DAQ, the lead glass detectors will be divided to 15 segments. Each segment forms a set of triggers including: preshower high threshold (ps#h), total shower high threshold (ts#h), electron narrow (e#na), pion narrow (p#na), electron wide (e#wa) and pion wide (p#wa). All are NIM signals with pulse width 20 ns (for e#na and p#na) and 100 ns(for ps#h, ts#h, e#wa and p#wa), respectively. In additon, electron and pion triggers from all 15 segments will be "OR"ed to form the final electron narrow (en), electron wide (ew), pion narrow (pn) and pion wide (pw) triggers, which also need to be converted and sent to the TDC and the scalers. The total number of channels needed (for HRS-R DAQ test setup) is thus (15 segments) $\times$ (6 per segment) + 4 final trigger = 94 channels.

For each channel, one output will be sent to TDCs in the HRS DAQ to cross check the trigger. The 2nd output will be sent to SIS3800 scalers for helicity-gated event counting. The 3rd and the 4th outputs are not used in the current trigger design but will be useful for other independent check later. Figure 2 shows the full trigger design for reference.

Because there is very limited space in the detector hut, we have space for only 6 single-width NIM modules to accomodate the level tranlators. Therefore each translator should accomodate at least 16 channels. Figure 1 shows two possible designs of the front panel, one design has all four outputs in the front and the other design has two sets of outputs in the front and the rest in the back panel.

Detailed specifications for the level tranlator are listed as follows:

1. Single-width NIM module;
2. At least 16 independent channels per module, more will be better;
3. Each channel has a single input LEMO connector which accepts a fast negative NIM level < 1 ns time jitter, 50 $\Omega \pm 10\%$ input impedance; -300 mV threshold; input protected to ± 8 VDC;
4. The input signals have a nominal width between 10 ns and 100 ns with a typical rise time of 2 ns.
5. Each channel converts to four (4) ECL outputs grouped in flat cables with 34 pin headers and lock and eject feature;

[1]rom@jlab.org
[2]shahinya@jlab.org
[3]bogdanw@jlab.org
[4]xiaochao@jlab.org

6. DC - 200 MHz translation;

7. The input to output is direct coupled with the output duration equal to the input duration. The delay should be no more than 10 ns, is reliable and has little variation. The variation in delay time of all modules should be less than 1 ns;

8. The 4 ECL outputs in each channel should be isolated from each other;

9. Each ECL output should have 2 ns rise and fall times;

10. The crosstalk between neighboring channels must be less than 35dB and 60 dB is desired;

11. In addition, there are four logical "OR" outputs per module in the form of LEMO connectors (NIM standard). Each of these outputs is an "OR" of a group of 4 inputs. The timing specifications are the same as the ECL outputs.

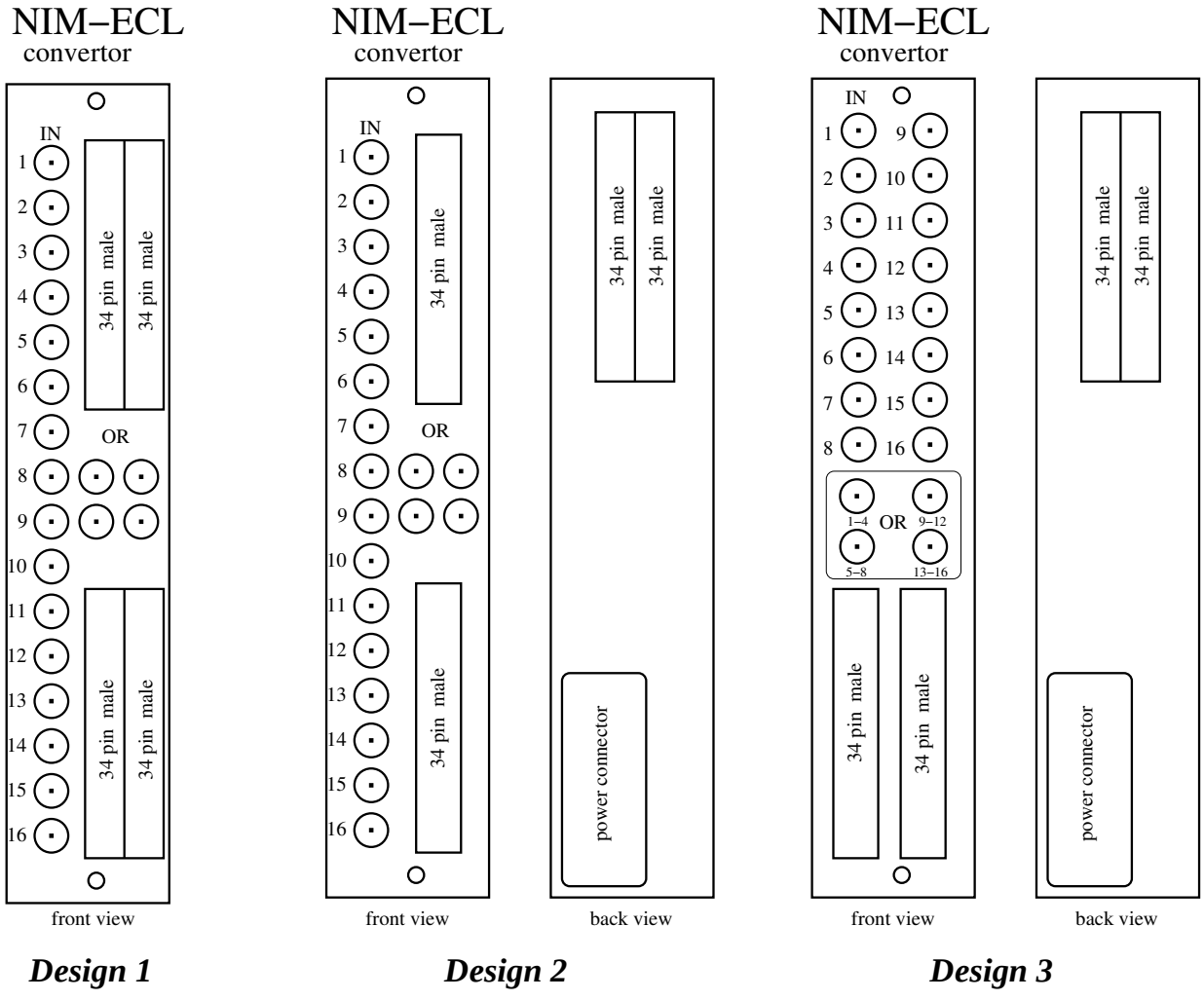

Figure 1: Three different designs for the front panel.

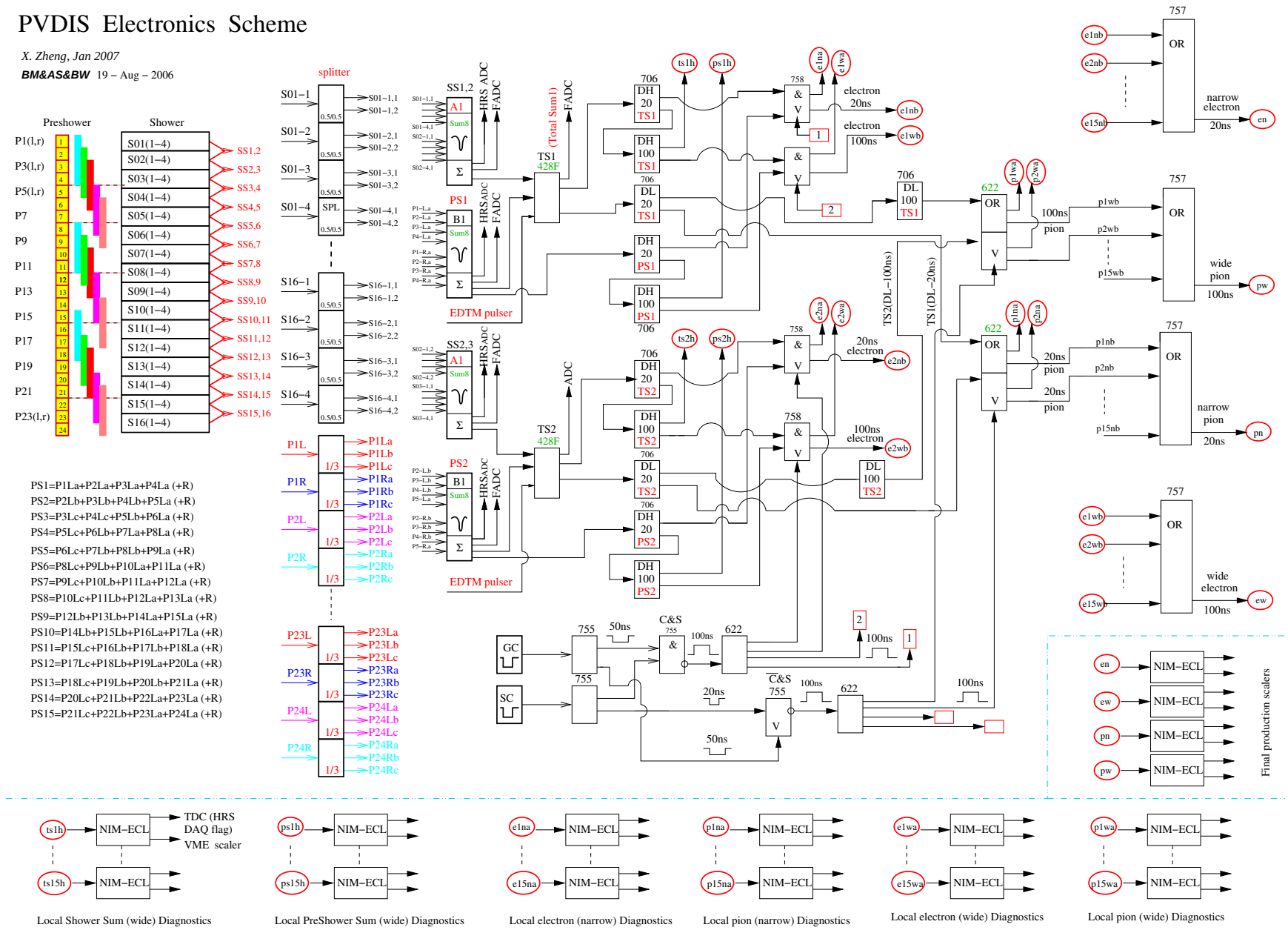

Figure 2: Trigger design for PVDIS fast counting DAQ.