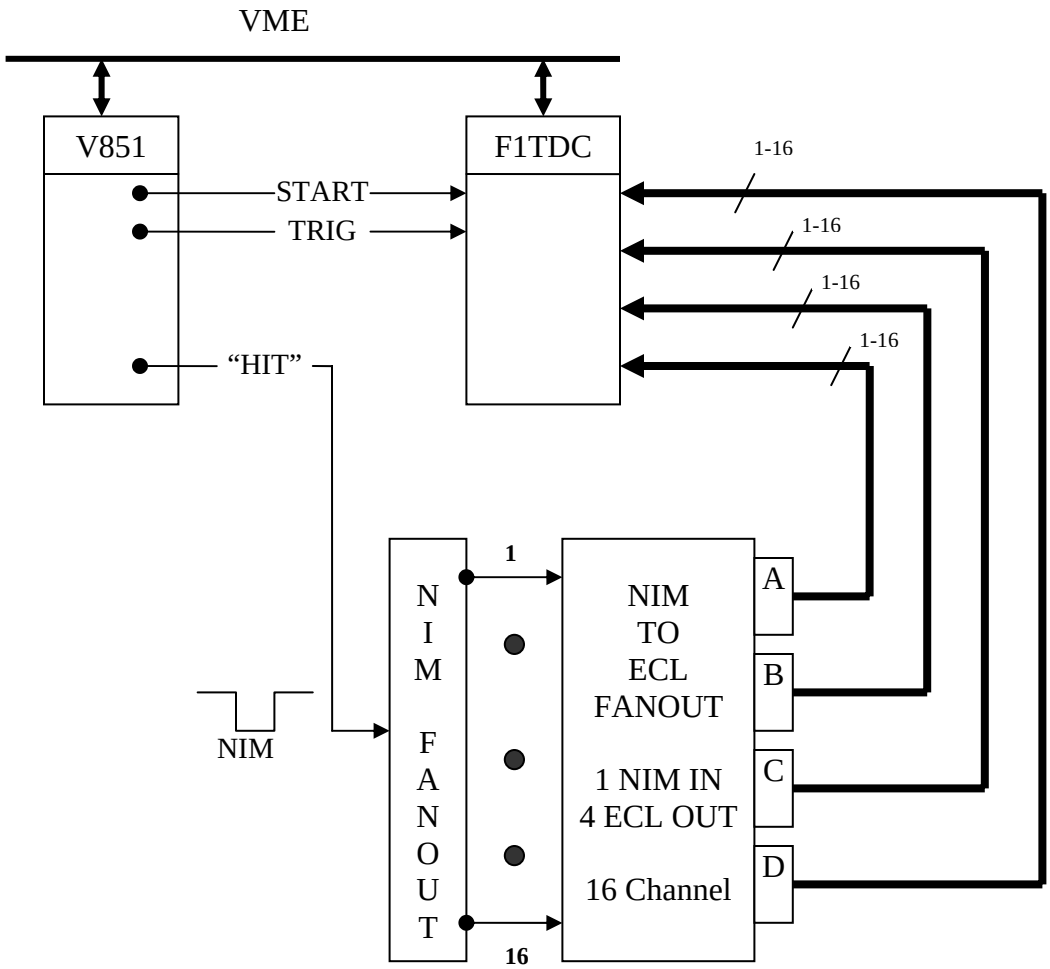

Figure 1: TDC test setup for NIM to ECL [Prototype] Module

Devices:

1. V851 Highland Technology – Digital Delay Generator
2. JLAB F1TDC – 64 channel 'normal' resolution (112ps per count)
3. VME 1 to 16 NIM fan-out module
4. DEVICE UNDER TEST [DUT]

TEST DESCRIPTION

The JLAB F1TDC module is used in normal resolution mode which allows for 64 channels of ECL input with a least significant count of 112ps.

The V851 digital delay generator is programmed to produce the required signals to initiate a data acquisition cycle from the F1TDC. The START to "HIT" delay is 1.4uS and the trigger rate is 1 KHz.

The single NIM output from the V851 is connected to a NIM fan-out module that produces 16 NIM inputs to the prototype 16 channel NIM to 4 ECL output converter module [DUT]. The four output connectors from the DUT are routed to the F1TDC inputs. Each of the four output cables carries 16 differential ECL signals to the F1TDC.

Cables from the NIM fan-out module to the DUT and the output cables from the DUT are the same length, and the differences in pulse arrival time is measured with the F1TDC.

RESULTS (1st test run)

Data shown below is an extracted from a recent test with the 64 channel JLAB F1TDC module. The F1TDC is programmed to run in non-synchronous mode, and with a least significant count of 112ps. The number of trigger 'events' is over a million as displayed in the last column of the data. All channels received the same number of triggers.

As shown in Figure 1, the HIT signal is sent to the NIM fanout modules, and the delay from the START is measured to be 1.4us. Note that the standard devation(SIG) is less than 1 count of 112ps, so the whole setup has low intrinsic jitter. One thing to note about the test setup, is that the delay of the 16 channel NIM fanout module will be included in the measurement. Cable lengths from the NIM fanout to the NIM-to-ECL converter are the same, and the data show that the transition delay between channels is less than 1ns.

Chip 1 Chan 0 AVG = 14378.476 SIG = 0.8642 min = 14374 max = 14383 diff = 9 (num = 1226009)
Chip 1 Chan 1 AVG = 14383.825 SIG = 0.8544 min = 14380 max = 14388 diff = 8 (num = 1226009)
Chip 1 Chan 2 AVG = 14374.734 SIG = 0.8591 min = 14370 max = 14379 diff = 9 (num = 1226009)
Chip 1 Chan 3 AVG = 14381.479 SIG = 0.8646 min = 14377 max = 14385 diff = 8 (num = 1226009)
Chip 1 Chan 4 AVG = 14374.618 SIG = 0.8220 min = 14370 max = 14379 diff = 9 (num = 1226008)
Chip 1 Chan 5 AVG = 14380.090 SIG = 0.8691 min = 14376 max = 14384 diff = 8 (num = 1226008)
Chip 1 Chan 6 AVG = 14375.501 SIG = 0.8662 min = 14371 max = 14380 diff = 9 (num = 1226008)
Chip 1 Chan 7 AVG = 14385.343 SIG = 0.8727 min = 14381 max = 14390 diff = 9 (num = 1226008)

Figure 2: Initial TDC Test Data (8 channels shown)

Timing Diagram: