Specification of HAPPEX II ADC Timing Board, Revision 1

- Added a second 12-bit DAC, with its own V/F convertor with optical output, for 2nd feedback.
- specified number of oversample to be 1-20
- Check with source group on desired feedback signals. put appropriate symbols on both feedback outputs.

The primary function of the HAPPEX ADC Timing Board is to generate the timing signals controlling the triggering and readout of the HAPPEX ADCs. In addition, the board performs several secondary functions, acting as a two-channel input register, generating a signal of fixed frequency which can be used to implement feedback schemes at the electron source, and providing a 16-bit DAC for use in the calibration of the HAPPEX ADCs. This board is implemented as a VME module in order to allow timing parameters and other information to be set via the backplane.

1 ADC Timing

Each ADC board requires high-precision external timing signals to perform the integration cycle. The Timing Board provides those signals which are distributed to the ADCs through a ribbon cable. An additional signal, available through a separate ribbon cable connector, is used to trigger the DAQ readout of those ADCs.

The timing of all signals is based on a 20 MHz crystal clock oscillator specified to have 50 ppm stability. This clock is divided down to 400 kHz by counters to form the basic timing unit. Two timing parameters, **Ramp**

Inputs	**Outputs**	**Diagnostic Ouputs**
Master Trigger	Reset Peak Baseline Convst VME Trig	Integrate Gate

Table 1: List of input and output signals for Timing function.

$-+$	*unused*
$-+$	Reset
$-+$	Convst
$-+$	Peak
$-+$	Baseline

Table 2: Order of output signals on ADC Ribbon Cable, top to bottom, pins 0-9.

Delay and **Integration Time**, are set via the VME interface, in units of these $2.5\mu s$ clock steps.

One input signal **Master Trigger** is received by the timing board as an external trigger. Both optical fiber and optically-isolated TTL connectors are provided for the **Master Trigger** input signal. Five separate output signals are produced. Four of these are differential positive ECL (PECL) signals, delivered to the ADC boards via ribbon cable: **Reset**, **Baseline**, **Peak**, and **Convst**. (As measured on the current board, $V_{low} = 0.35V$, $V_{high} = 1.15V$, and the **Convst** signal has inverted polarity). The fifth, **VME Trig**, is an ECL signal which is delivered to a second ribbon cable connector (current board measured with $V_{low} = -1.8V$, $V_{high} = -0.8V$). An additional signal, **Integrate Gate**, is provided for debugging purposes through a lemo connector. **Integrate Gate** is asserted between the trailing edge of **Baseline** and leading edge of **Peak**. These signals are listed in Table 1 and the ADC ribbon cable configuration is shown in Table 2.

The **Master Trigger** initiates the data collection cycle. The input/output signal timing is illustrated in Fig. 1.

- In the initial state, **Reset** and **Convst** are set high, and all other output signals are set low.

- The arrival of a **Master Trigger** initiates the timing sequence. The first step of the sequence is a delay; the timing board pauses for a period of time determined by the **Ramp Delay** setting.
- At the end of the **Ramp Delay**, the **Reset** signal is dropped to low.
- $15\mu s$ after the **Reset** signal is dropped, the **Baseline** signal ($2.5\mu s$ width) is issued.
- The diagnostic signal **Integrate Gate** is asserted with the trailing edge of **Baseline**.
- The **Peak** signal ($2.5\mu s$ width) is issued, with the **Peak** leading edge delayed relative to the **Baseline** trailing edge by a time determined by the **Integration Time** setting.
- The diagnostic signal **Integrate Gate** is dropped with the leading edge of **Peak**.
- $2.5\mu s$ after the **Peak** trailing edge, the **Reset** signal is returned to high, where it remains until the next trigger is received.
- $22.5\mu s$ after the **Peak** trailing edge, the **Convst** signal ($2.5\mu s$ width) is issued.
- $7.5\mu s$ after the **Convst** trailing edge, the **VME Trig** signal is issued.

Two jumpers are used to select the rising or falling edge of the **Master Trigger**. If jumper 1 is on, a rising edge of the **Master Trigger** initiates the timing cycle; if jumper 2 is on, a falling edge initiates the timing cycle. If both jumpers are on, both a rising or a falling edge of **Master Trigger** initiates the timing cycle. In any case, a new timing cycle cannot be triggered while a timing cycle is in progress, so once the timing sequence has been initiated, the **Master Trigger** signal is ignored until the issuance of the **VME Trig**. (In the current wire-wrap implementation: tying pin 83 of FPGA to +5V causes trigger on rising edge, tying pin 58 of FPGA to +5V causes trigger on falling edge. If both pins are tied to +5V, both rising and falling edge cause a trigger.)

A number of oversampling periods, from 1 through 20, can be specified through the VME interface. For more than one sampling period, the timing

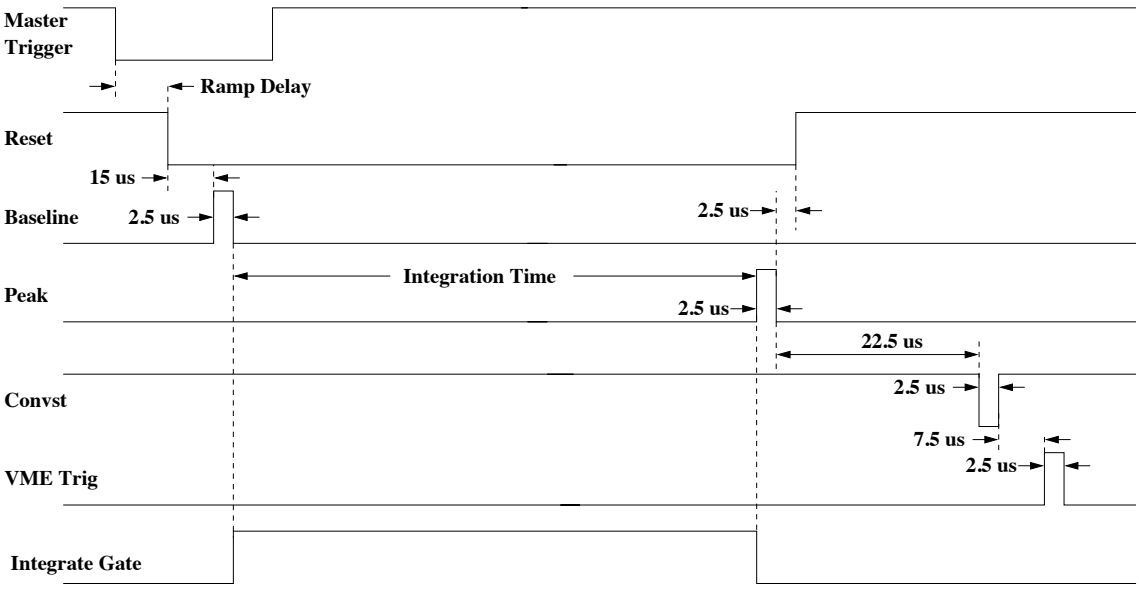

Figure 1: Timing diagram for Timing Board timing signals.

sequence described above is modified so that the **Ramp Delay** is used only once, while for each oversample, the relative timing of the 5 output signals is maintained. For each oversampling period after the first, the **Reset** signal is dropped to low at the trailing edge of the **VME Trig** signal. Thus, a delay of $52.5\mu s$ lies between the leading edges of a **Peak** signal and **Baseline** of the subsequent oversampling period.

2 Input Register Function

A secondary function of the ADC Timing Board is to act as a two-channel VME-interface input register . Both optical fiber and optically isolated TTL connectors are provided for each of the two channels. Each channel is used to set a bit in the VME register (Data0 and Data1 bits in Table 3). In addition, these inputs are converted to ECL and applied to a channel in the ribbon cable connector that also carries the **VME Trig** signal.

Hex Address	Register Name	Read/ Write	Bit	Description
$0	Input Data	R	0	Data0
		R	1	Data1
$2	*unused*			
$4	12-bit DAC #1	W		12-bit DAC set value
$6	12-bit DAC #2	W		12-bit DAC set value
$8	16-bit DAC	W		16-bit DAC set value
$A	Ramp Decay	R/W		
$C	Integration Time	R/W		
$E	Oversample	R/W	0-7	Oversample Setting
		R	8-15	Current Oversample

Table 3: Address map for the ADC Timing Board. All addresses are relative to the base address.

3 DAC and V/F Converter Functions

Two 12-bit DAC units apply an analog voltage to lemo connectors with an output range of 0-10 Volts. Each DAC also feeds a V/F converter, which is output through an optical connector with a range of 0-100 kHz. These DAC values are set on the VMEbus backplane at addresses $4 and $6.

The board also contains a second, high-precision 16-bit DAC, with an analog output range (through a lemo connector) from -5 to 5 Volts. The 16-bit DAC value is set at address $8.

4 VME Interface

The ADC Timing Board occupies 16 bytes of 16-bit VME address space. The address of a register on the board is given in hexadecimal by 0xffffXXXY, where $XXX is the 12-bit base address and $Y is the relative address. The base address is set by a 12-bit switch on the board. The address map shown in Table 3 gives the relative addresses of the registers on the board.

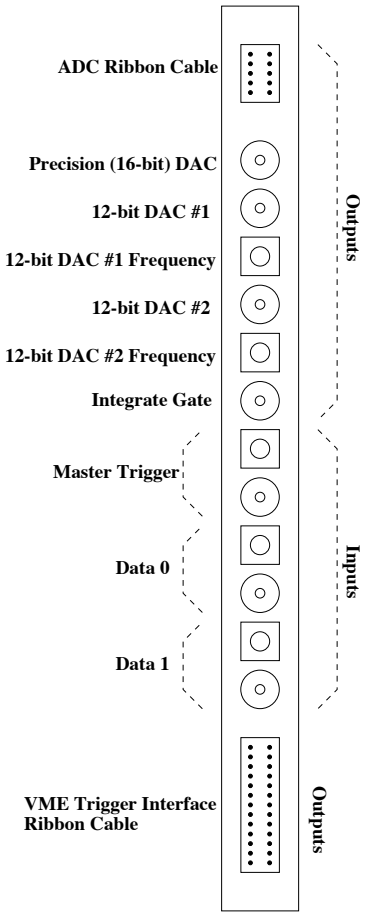

Figure 2: Front panel of Timing Board.