Shashlyk module test correction and scintillator plating test

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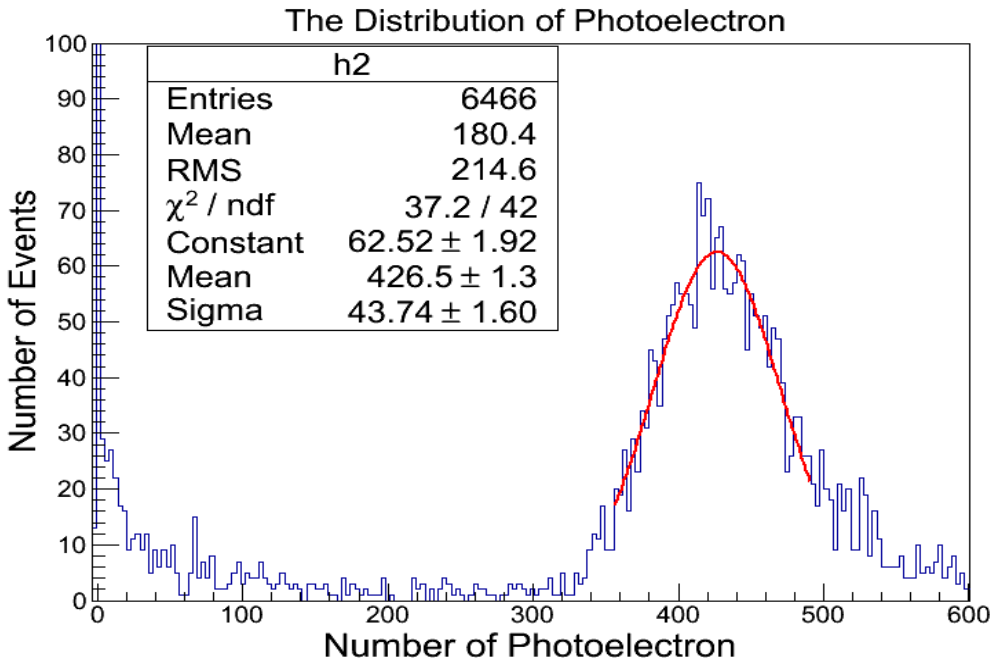
Error statement: double light yield for all shashlyk test showed before

I'm sorry for my mistake, for all shashlyk test showed in the meeting two weeks ago and Wuhan meeting, I used wrong script to calculate the photon number, in which the gain is set to 10^7, not the real gain 5*10^6, and the real light yield should be double. It just influence shashlyk test, the others' result is correct.

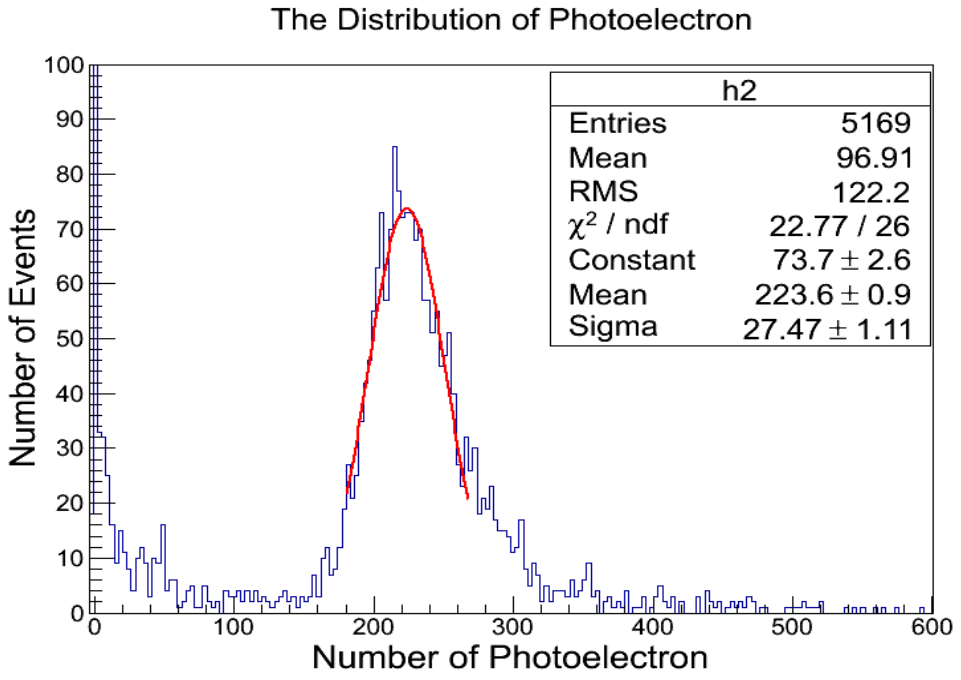
Calculation equation:

number[i]=(compensation*LSB_v965_high_range[channel]*(data_channel[i]-pedestal))/(1.6*Gain)

Corrected vertical test result for two modules:

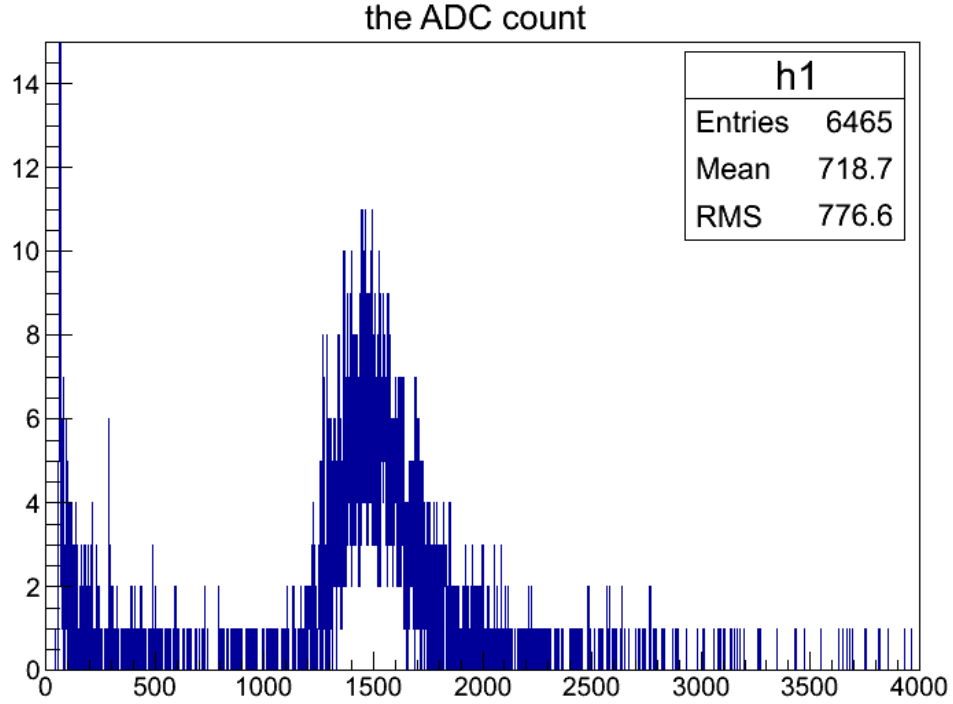


Module SDU #1

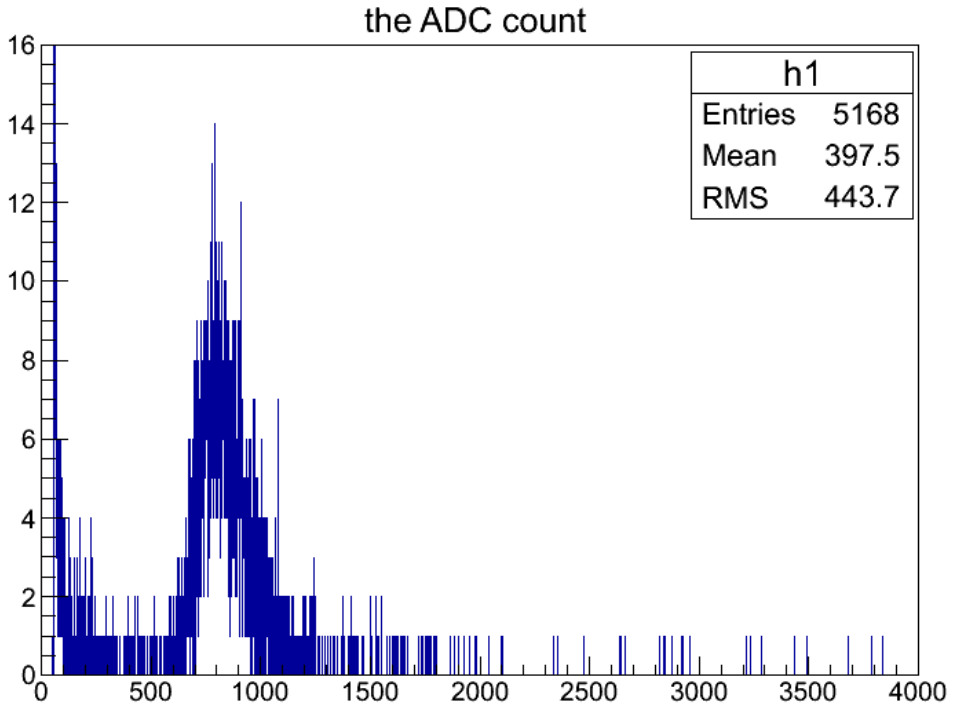


Module SDU #2

Raw ADC channel



Module SDU #2 vertical test ADC channel in high range

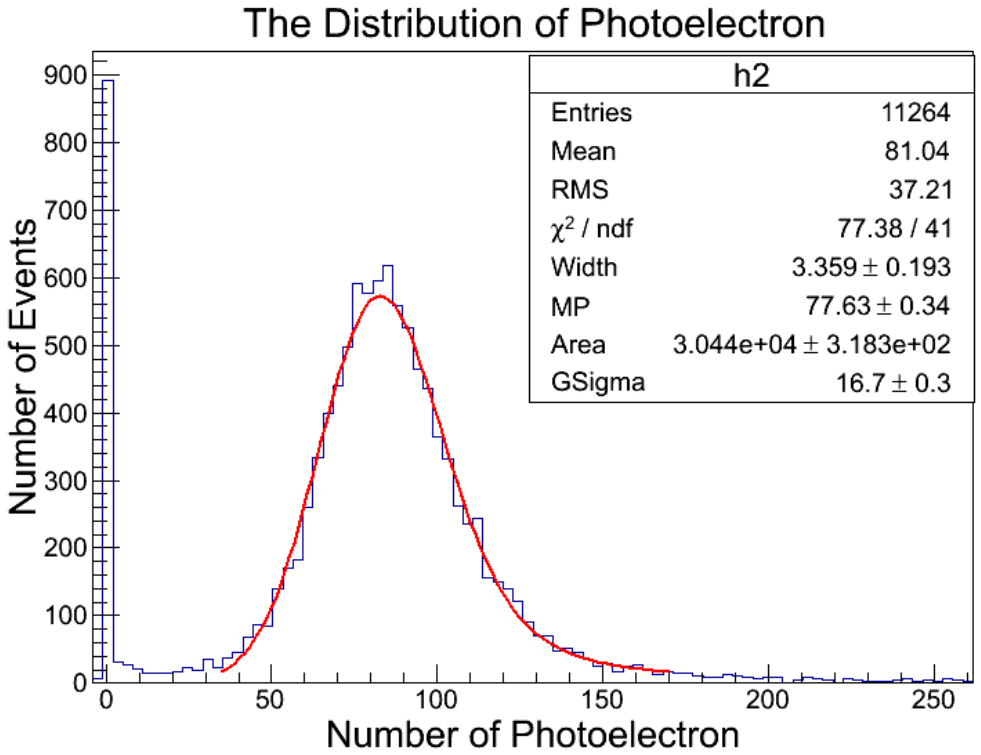


Module SDU #1 vertical test ADC channel in high range

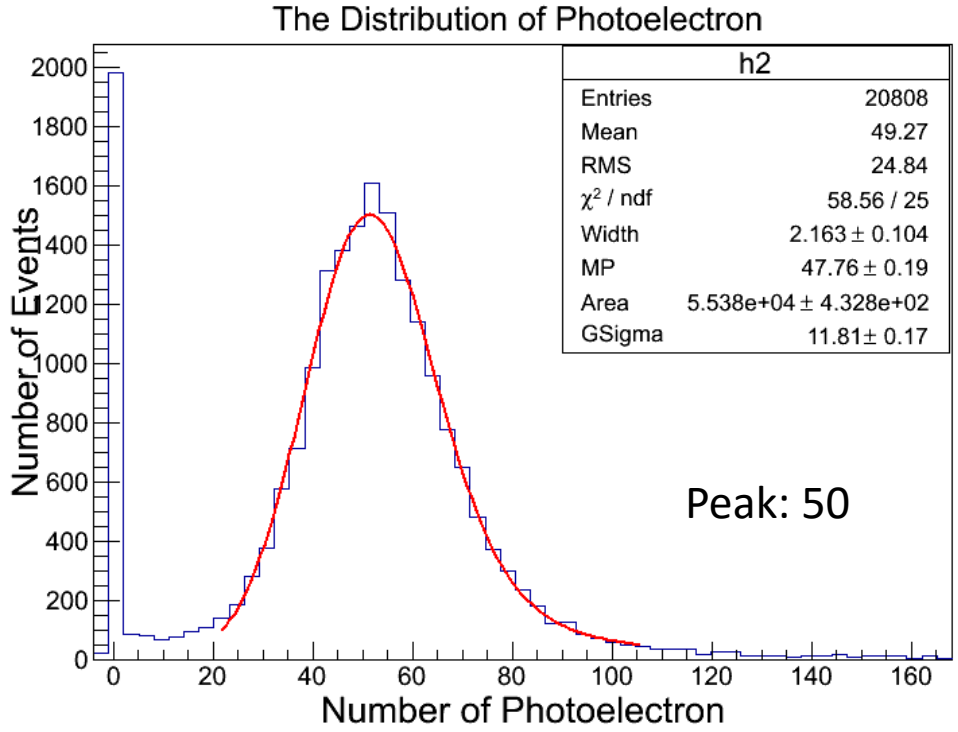
Setup for different module

Module No.	WLS fiber	Scintillator	Lead layer	Fiber end	Reflective layer	Front plate
SDU #1	BCF91	Kedi(original)	From US	No mirror	Print paper	
SDU #2	BCF91	Kedi(new)	From China	Silver mirror	Print paper	No holes

Horizontal test correction result



Module SDU #2



Module SDU #1

Shashlyk test result update

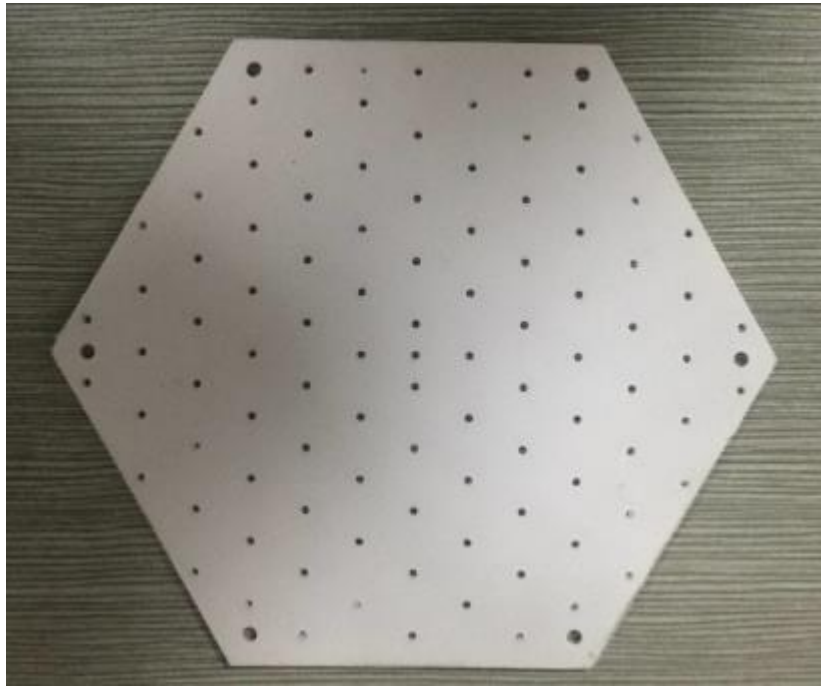
module	Vertical (resolution)	Horizontal	Horizontal(without Tyvek)
SDU #2	426.5(10.25%)	83	
SDU #1	223.6(12.28%)	50	38.6
RATE	1.907	1.66	

- Supplement: attenuation on delay cable (reference value)

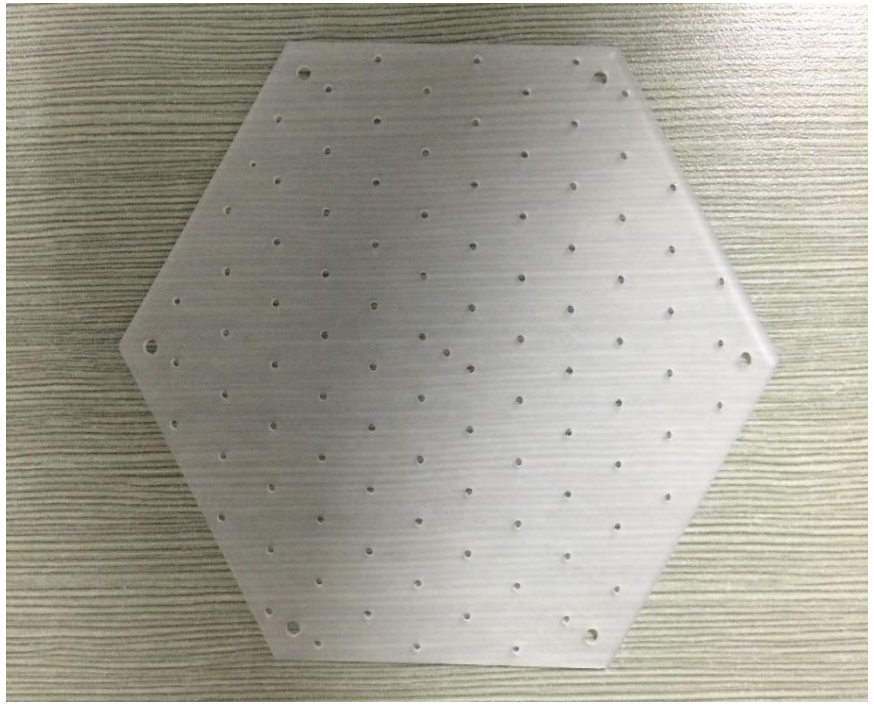
  With 63.5ns Delay cable, the attenuation is around 3% comparing with no delay cable. For 400 photo-electrons, the ADC channel is around 1600. (considering pedestal is 71.52)

LED voltage(V)	4.72	4.73	4.74	4.75	4.76	4.77	4.78	4.79
Without delay	1173	1325	1480	1663	1867	2090	2256	2488
With delay	1146	1290	1448	1620	1820	2032	2200	2432
attenuation	2.5%	2.87%	2.32%	2.78%	2.69%	2.96%	2.63%	2.37%

Scintillator plating material test



Surface plated by ZnS



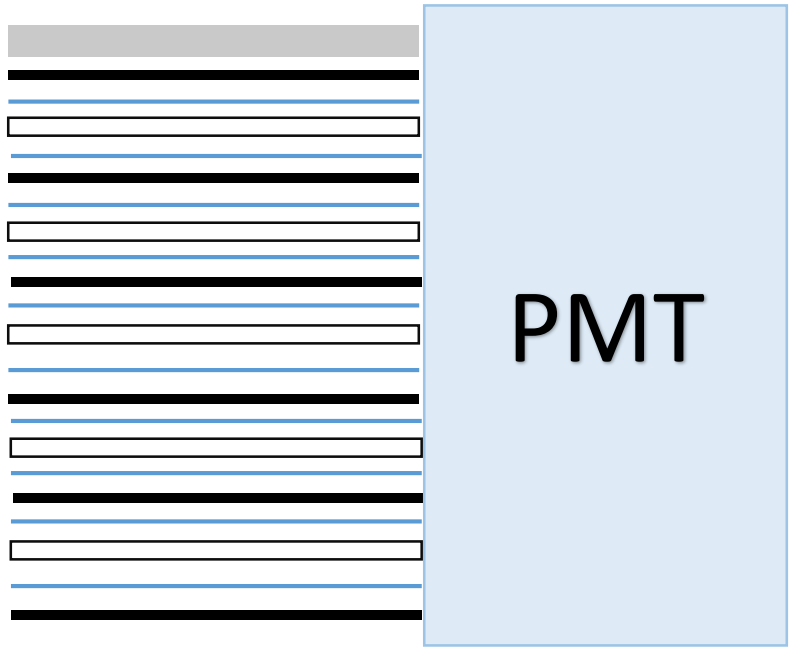
Frosted surface

The edge property of scintillator plated by ZnS is not good

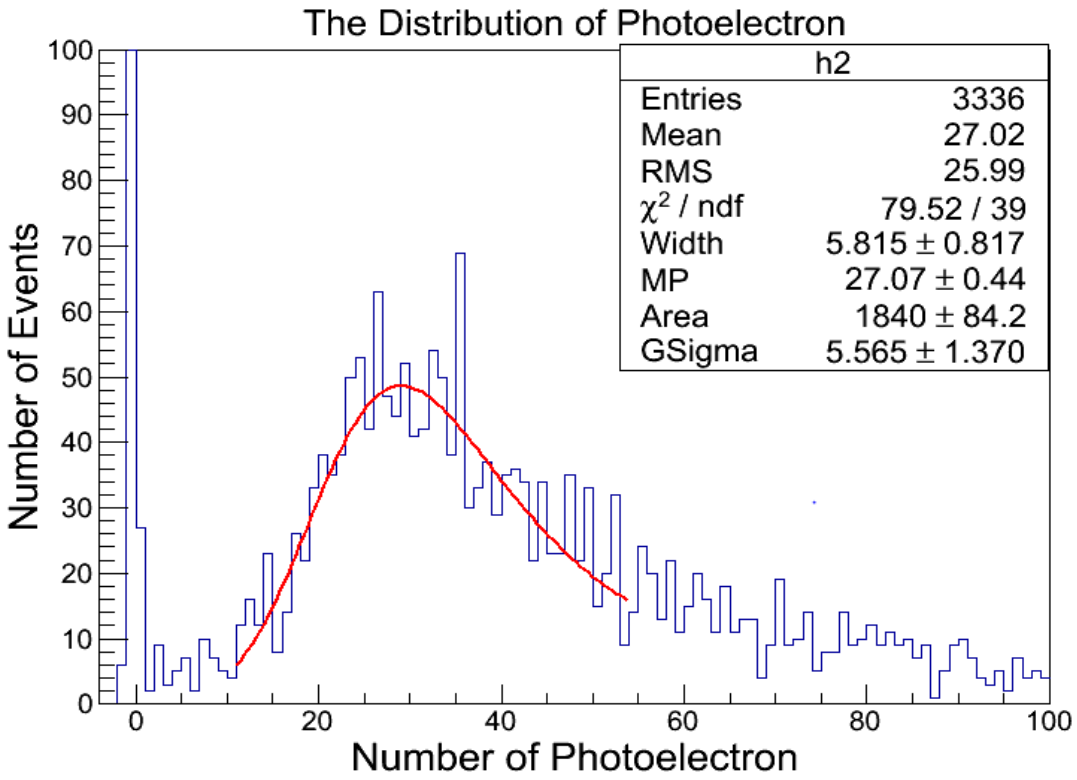
Original edge

After polishing by myself

Scintillator sheet test setup



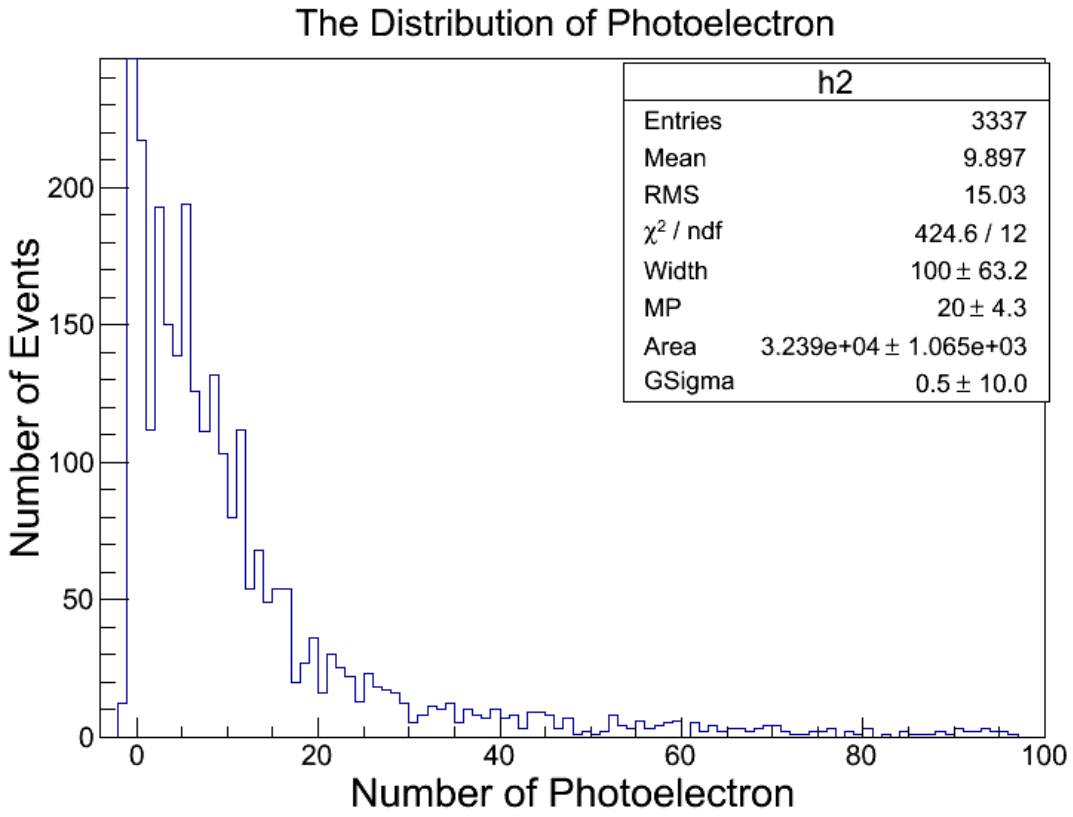
Lead + paper + scintillator + paper



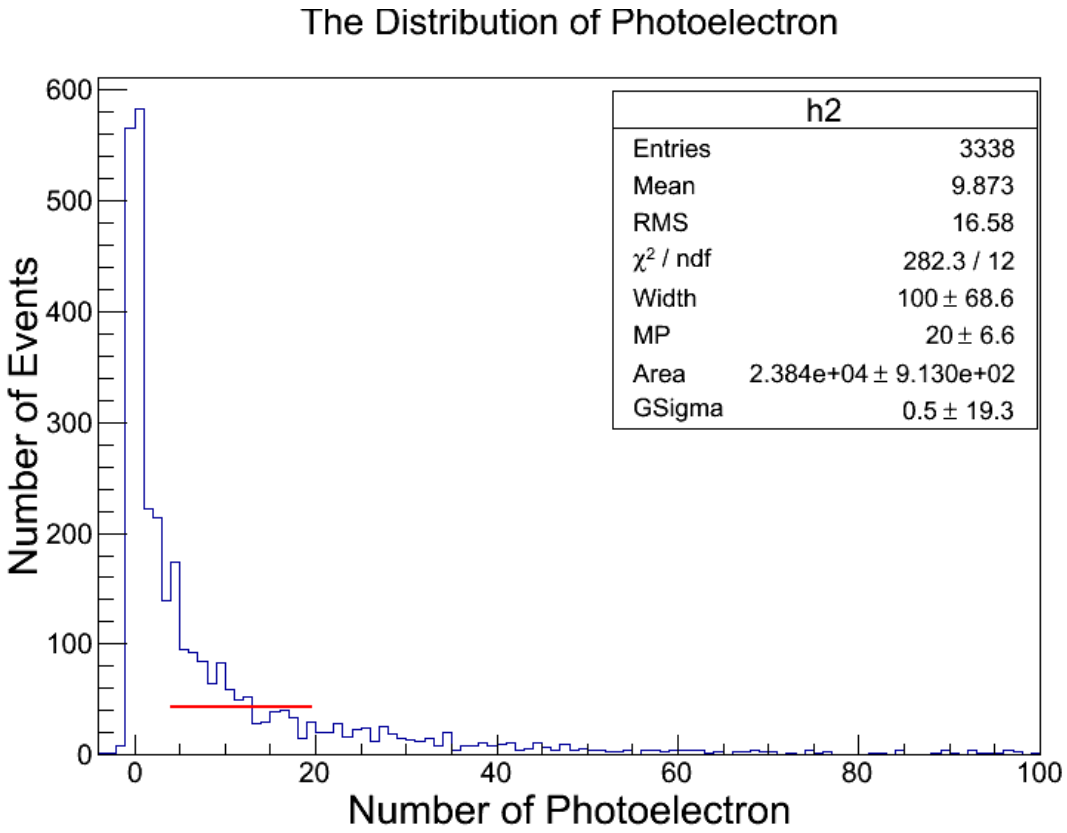
Setup： 5 scintillators in a group, coupled to PMT directly.

Normal signal from reference scintillator in same test （we test 4 groups at same time, and one is always used for reference scintillator.)

Plating surface test result



Surface plated by ZnS



Frosted surface

Both signal are very low, the result ned to confirm especially the ZnS plating which should not be so bad.

Back up: resolution calculation

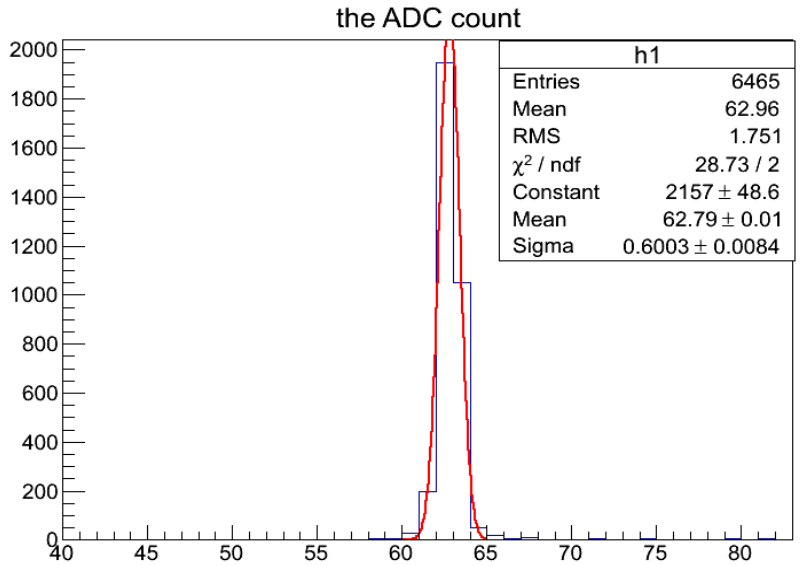
$$resolution = \frac{1}{\sqrt{N}} \cup \frac{\sqrt{\sigma}}{\sqrt{N}} \cup a$$

Other influence, such as electronic

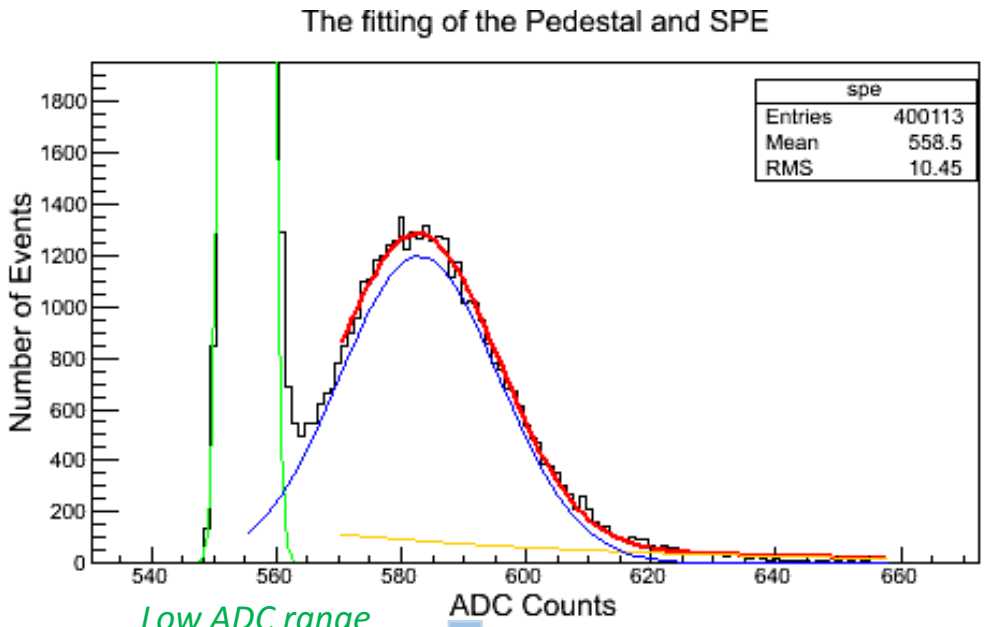
σ is the resolution of SPE spectrum.

Fluctuation from photon number,

For specific photon number, fluctuation from SPE resolution



Pedestal of high ADC range (1% resolution)



Low ADC range

```
****************************************
<All entries>: 400113
<Signal count start>: 565
<Signal entries>: 40367
<The radio of the signal>: 10.09%
<Peak value for pedestal>: 555.26
<Peak value for Single PE>: 582.59
<Peak to Valley ratio:>: 1.36(1272.56/936.78)
<spe_peak - pedestal_peak>: 582.59-555.26 = 27.33
<single PE resolution>: 12.75/27.33 = 0.467
<LSB for ADC-ch8>: 0.02977 pC/count
<Anode output charge of SPE>: 0.813475 pC
[Absolute Gain]: 5.0773E+06
****************************************
root [1]
```