The mixed analog/digital shaper of the LHCb preshower may 2006 documentation

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Abstract

The LHCb preshower signals show so many fluctuations at low energy that a classical shaping is not usable at all. Thanks to the fact that the fraction of the collected energy during a whole LHC beam crossing time is 85%, we studied the special solution we presented at Snowmass 1 999 workshop. This solution consists of 2 interleaved fast integrators, one being in integrate mode when the other is digitally reset. Two track-and-hold and an analog multiplexer are used to give at the output 85% of the signal plus 15% of the previous one. These 15% are digitally computed from the previous sample, and subtracted. A completely new design of this solution had to be made, see figure 2. This new design is described, including new methods to decrease the supply voltage and the noise, as well as to increase the quality of the reset and the linearity. An output stage, consisting of a AB class push-pull using only NPN transistors is also described. Laboratory and beam test results are given.

I. Introduction

The LHCb preshower is used for the level 0 trigger, for which a threshold corresponding to 5 minimum ionization particle (MIP) is applied, with a 5% accuracy. This detector is also used to improve electron and photon measurement up to 100 MIP. These two functions give us a dynamic range of 0.1 to 100 MIP (i.e. 10 bits).

The study of the signal [1] given by a scintillator cell and the 64 channels Hammamatsu PMT, with a good agreement with their simulation, shows us that at low energy, the dominant effect is the statistical fluctuation of the photoelectron collection, see figure 1. These conditions, and the fact that the signal length is always longer than 25 ns, drive us to the solution described before. We don't change the main electronic choices we made on 1 999 [2] :

- DC coupling from PM to ADC ;
- two interleaved half channels ;
- a fully differential design to minimize the noises ;
- bipolar transistors at the input stages to reduce the offsets ;

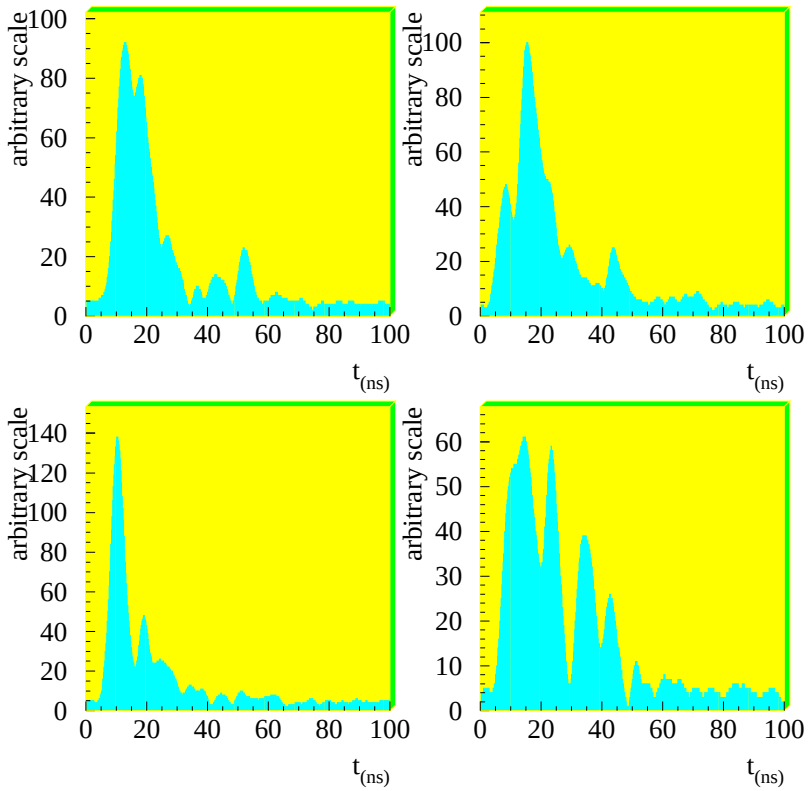


FIG. 1 – cosmic events

– AMS 0.8 μm BiCMOS technology and CADENCE tools (2004 final design).

We had to design the chip with the following considerations :

– because of the PMT ageing, the gain is 25 $k\Omega$. The first stage is a current convoyer. For the noise, the integrator input stage is new and for the offset and the operating point stability a special common mode feedback loop was added ;
– we need a very high quality reset, to be able to compute the subtraction with a negligible error, even in the cases of a maximum signal immediately followed by a "trigger level" one : the integrator itself was changed ;
– the supply voltage had to be decreased down to $\pm 2.75\,V$ to match the foundry specifications, and to obtain the "small power consumption" of 100 mW/channel ;
– to carry the 6 000 output analog signals, we plan to use simple ethernet differential cables on up to 20 m long, in this case, we must adapt this cable at both end, and then have to double the dynamic. To save power, this dynamic is done in the last stage by designing a differential analog multiplexer with a gain of two, and a $\pm 2\,V$ dynamic range with a $\pm 2.75\,V$ supply. This required the design of parallel linearity correction instead of the previous serial one ;
– we have to drive efficiently the cable without extra chips : an "all NPN A-B class push-pull " was designed.

II. Design considerations

Most blocks of the chip are designed around a simple bipolar differential pair : this scheme is stable, easy to use and economic in term of silicon area. In addition, in a fully differential design, each signal has its opposite, which is very useful to compensate parasitic effects. In our case, we have to take care of the linearity : our calibration will be done essentially by the MIP values which are only 10 ADC counts. For this reason we need a non linearity smaller than 1%, and we have five blocks (i.e. five non linearity sources) in serial, see figure 2.

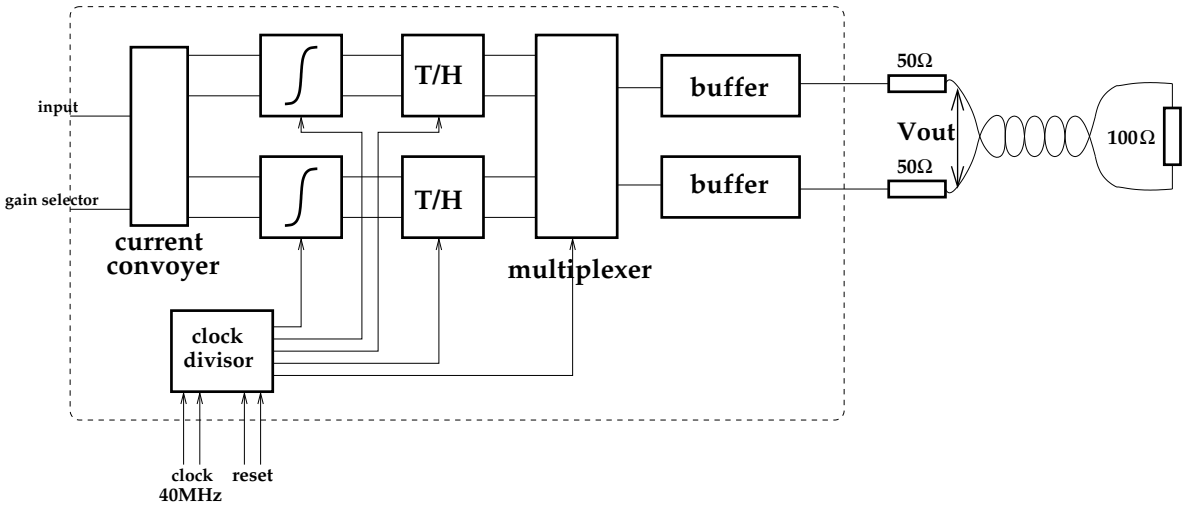


Fig. 2 – one channel design

It is well kown that the non linearity of differential pair, essentially due to the variation of the base-emitter voltage of the two transitors is easily corrected by the addition of one diode (gain of 1), or two diodes (gain of 2) in the collector branches to obtain the same voltage drop in emitter and collector load, see figure 3. However, the consequence of this "serial correction" is the lost of one or two diode voltage drops which is incompatible with a large dynamic range using small voltage power supply. The idea we explore to overcome this problem is to replace this "serial correction" by a parallel one, see figure 4.

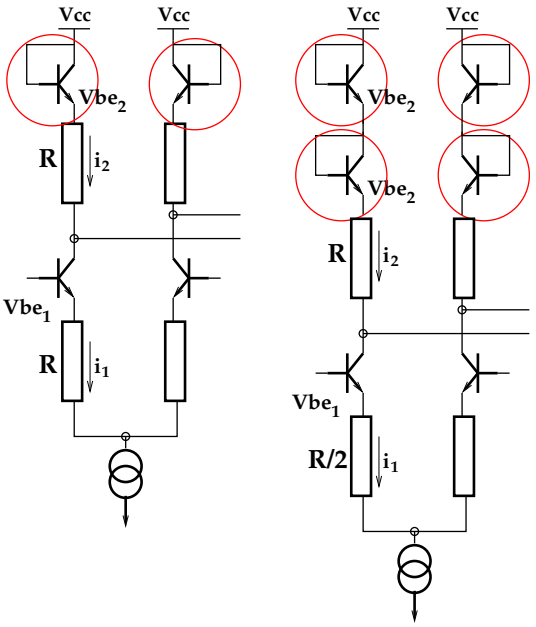


FIG. 3 – serial compensation

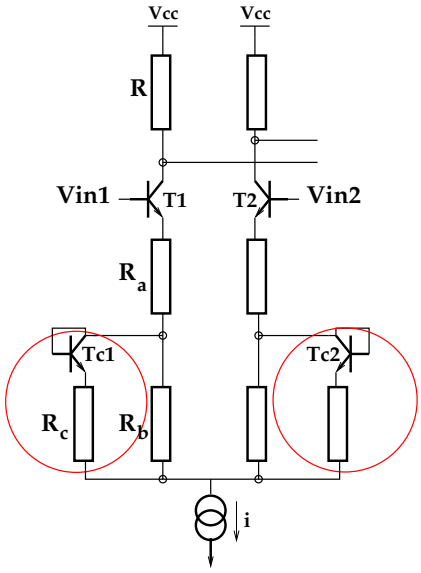


FIG. 4 – parallel compensation

In this new correction, the lost of gain is compensated by decreasing the emmitter load in the oposite branch. The gain obtained is double : we obtain a very good correction without lost of dynamic range and the over-compensation is possible. This is useful to compensates two stages with only one parallel correction.

As an example, see figure 3 and 4, on this application, a gain of 2 is needed in the multiplexer stage : using this correction a non linearity error of only $\pm 100\,\mu V$ was obtained for a 4 volt ($\pm 2\,V$) dynamic range including output stage, using a $\pm 2.75\,V$ power supply. Figures 5, 6, 7 and 8 shown the error obtained in this example in the cases of no compensation (5), under-compensation (6), over-compensation (7) and right compensation (8).

The solution described here is very sensitive to the clock jitter which determines the integration precision. For this reason, we decide to send to the chip the main 40 MHz clock, and to make the 20 MHz clock inside the chip. In the other hand to protect the analog parts of the chip against clock cross talk, the clock connections in the chip are all bipolar, low level, ECL, and the CMOS clocks of the integrators are generated inside each integrator block.

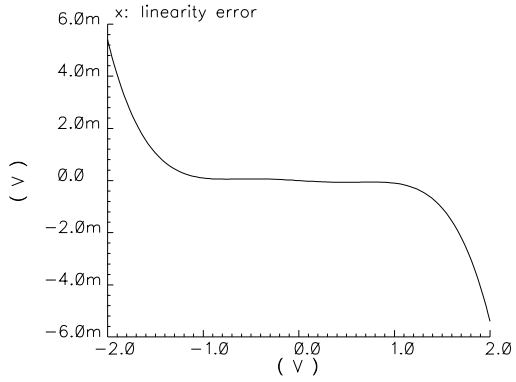


FIG. 5 – without

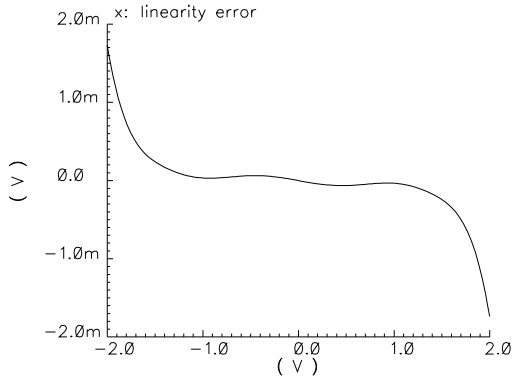


FIG. 6 – under

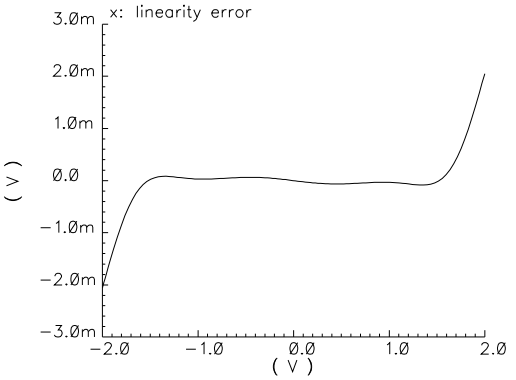


FIG. 7 – over

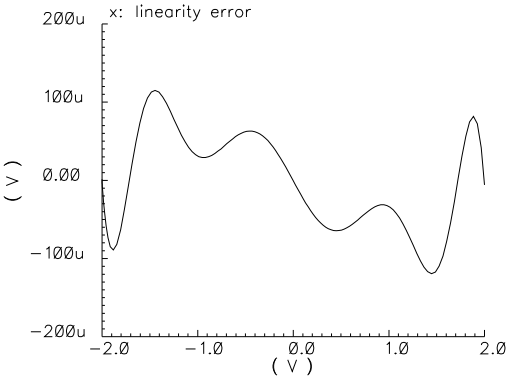


FIG. 8 – right

III. BUILDING BLOCKS

1.- CURRENT CONVOYER

Fig 9 shows the convoyer principle, and its simple scheme in $0.8\,\mu m$ technology. The PM current is handled in a super common base input, and then mirrored with gain. The goal is to retain the signal in current mode until the integrator output. Unfortunately, such a scheme is not differential and the quiescent current needed to assume linearity make it unusable like it is. A second, identical, dummy input stage solves this problem by giving a strictly identical quiescent current which is possible to subtract to the main one so that the result presented at the integrator input consists only on the true current signal alone.

Fig 10 shows the final scheme (convoyer output are doubled to drive the two integrators). In this scheme, the main noise contribution is the MOS transistor used to mirror the current. In the other hand, this transistor is also responsible of the offset and the bandwidth. If the bandwidth decreases, the α coefficient increases.

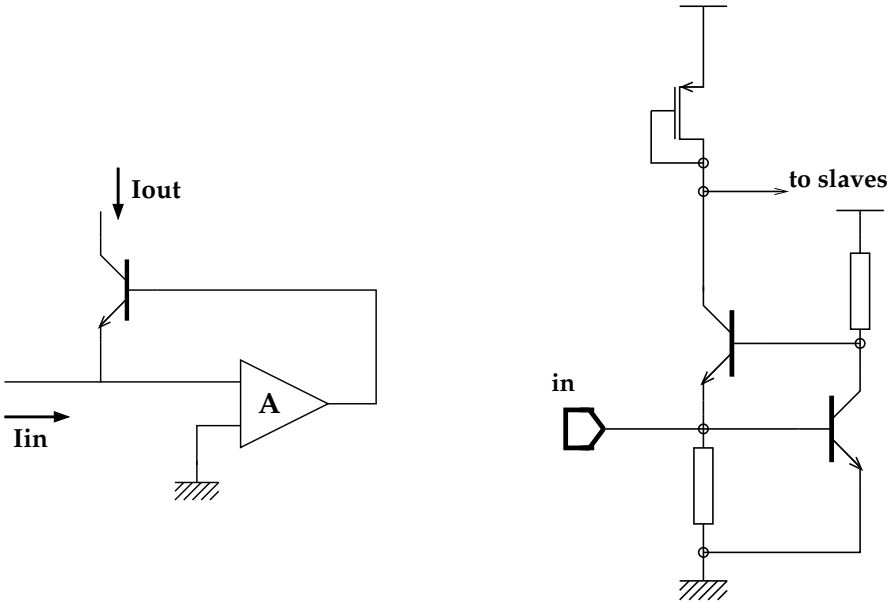


FIG. 9 – principle schemes

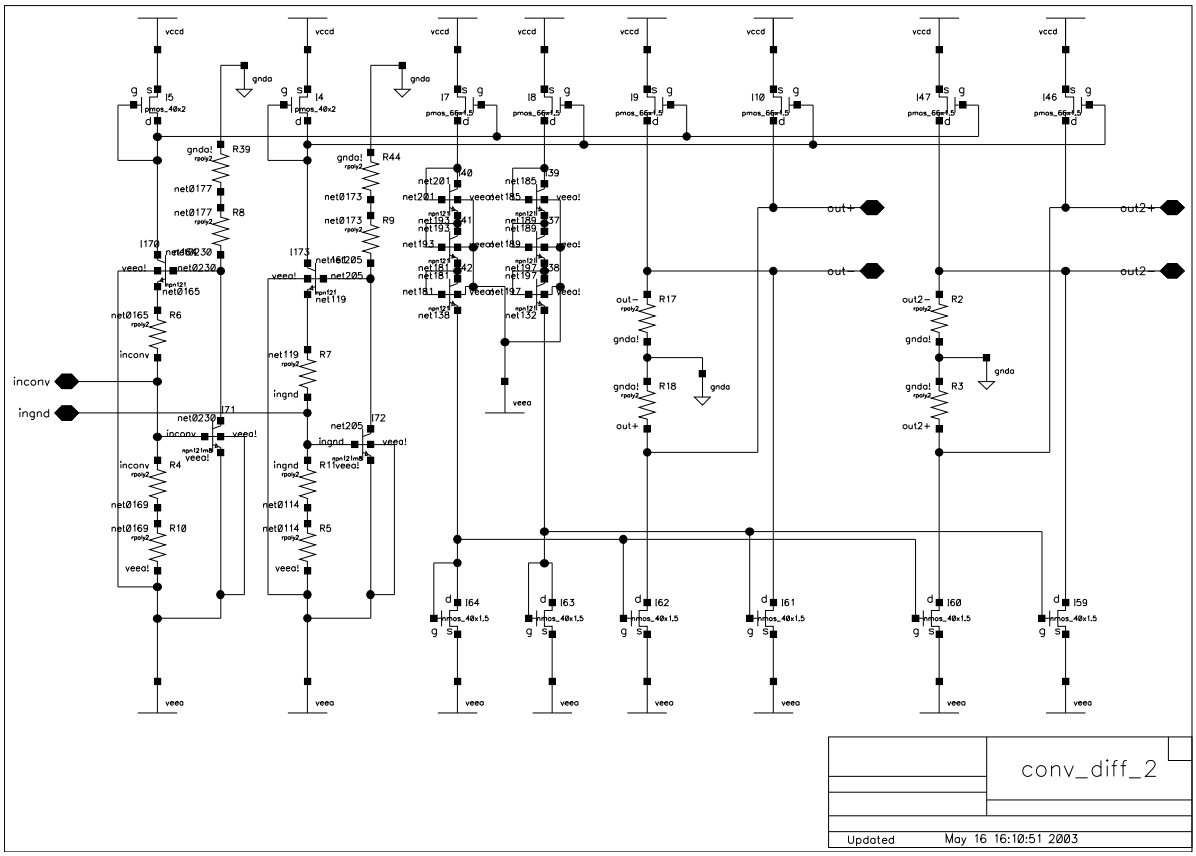
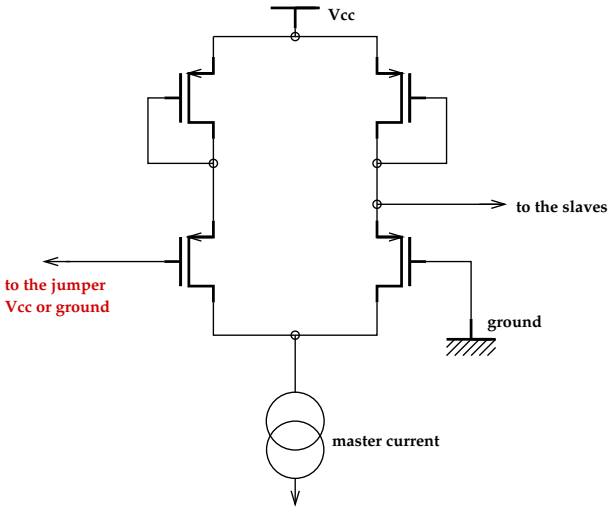


FIG. 10 – electric scheme of the current convoyer

2.- TWO GAINS

We modify the current master of the current convoyer.



We tune the gain with the jumper. If he is at ground, the current master passes one transistor, if he is at Vcc, the current master passes two transistors, the gain is decreased by a factor two.

3.- SWITCHED INTEGRATOR

This block, see figure 11, is built around the wide band high gain amplifier. It has two gain stages, the first is optimized to minimize the offset, the second is a rail to rail CMOS output. The connection between the two stages is a simple follower for the PMOS's and a fixed voltage drop (diodes and resistor at constant current) for the NMOS's.

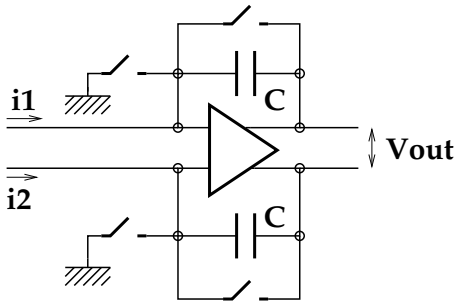


FIG. 11 – principle integrator

Two originalities are implemented :

During the integrate phase, from the DC point of view, the integrator is an open loop high gain amplifier : as a consequence the offset and the operating point stability are critical : for the offset greatest care was taken on the input stage (resistor load and transistors doubled and designed as a cross), and an extra feedback loop, acting only on the common mode signal was added see figure 12 : first the common mode voltage is obtain by summation of the two complementary outputs with 2 resistors. This voltage is then compared to ground and the error result amplified and applied with the same polarity on the two inputs. As a result, the output common voltage is maintained to ground, and the offset is reduced.

During the reset phase, inputs and outputs are shorted. As a conseqence the gain becomes very low and the virtual ground is not achieved. To overcome this problem two extra switches are added at the inputs. The four switches are designed with complementary MOS as usual to minimise the injected charge effect.

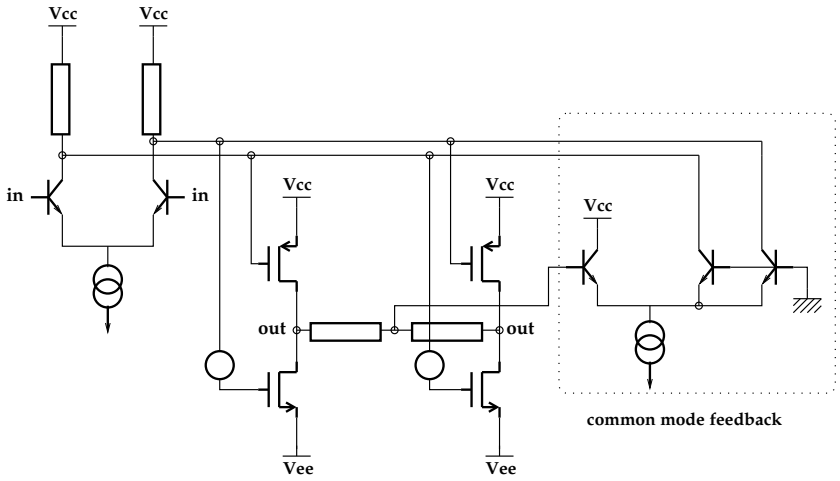


FIG. 12 – AOP with C.M. feedback

Results : the simulation results show a gain of 5 000 and a very high quality reset. The simulated linearity is perfect. An integrator was realized and tested alone. The test results are in very good agreement with the simulation : the offsets measured at the output vary from a few mV to a maximum of 100mV and the linearity is better than our measurement capability.

4.- TRACK AND HOLD

The used structure is described by Pieter Vorenkamp [3] and Jean-Marie Bussat [4], and already used and described several times. The compensation of the base emitter parasitic capacity was unchanged, but the "serial" linearity compensation was replaced by our new parallel one to be more confortable on dynamic and also to obtain the output operating point as high as possible. Under these condition, the $\pm 1\,V$ dynamic range was easily obtained with a linarity of few per thousand. These results were confirmed by the tests of the prototypes, see the LHCb web site [5].

5.- DIFFERENTIAL ANALOG MULTIPLEXER

The circuit was interesting to design : in this final version it is the key block where we had to go from $\pm 1\,V$ to $\pm 2\,V$ dynamic range, in a 25 ns multipexing operation without any crosstalk from one input to the other.

We start from the simple switch of two identical differential pairs of the figure 13. This scheme shows the following imperfections :

- it is a little too slow, specially to return to zero when the other input is high : The correction found is a simple pull up resistor, see figure 14 ;
- the non linearity errors, as explain before, was corrected with the "parallel compensation" ;

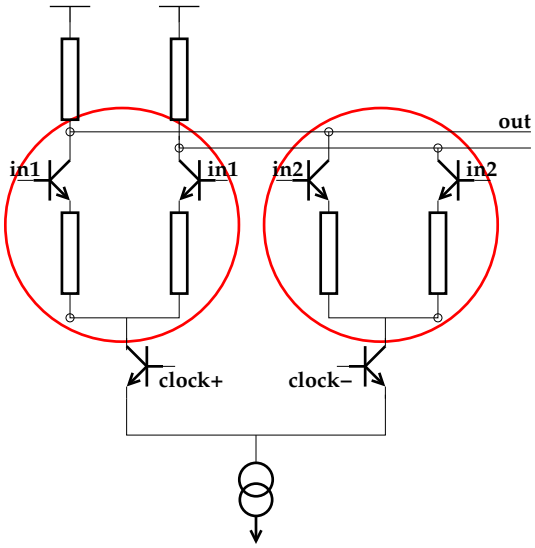


FIG. 13 – multiplexer design

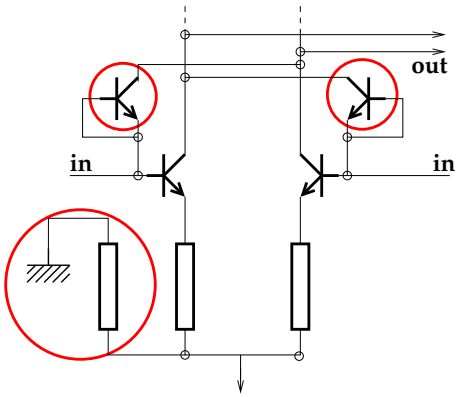


FIG. 14 – multiplexer detail

– as on many other multiplexers, there is a little cross talk between the two inputs, specialy when the unused input is fast and high. Here this fact is due to the fact that the blocked transistors of the non used input act as parasitic capacitor and inject on the output a little part of their own signal. Thanks to the fact that this design is fully differential, we used two extra transistors, always blocked, to inject also the opposite parasites, see figure 14. Notice that the 4 transistors have exactly the same base and collector operating points. As a result, the compensation is perfect, and the cross talk disappears fully.

6.- OUTPUT BUFFER

The output buffer is also a challenge : the consumption of the very front end board is very critical as we have to handle 64 channels and drive them on 27 meter cables, on a $7 \times 7\,cm$ PC board includind the 64 channel phototube ! A true class B or AB push-pull using only NPN transistors was designed. It can be seen on the figure 15 that transistors $T1$ acts as a usual complementary push pull. The transistor $T2$, which replaces the classical PNP is driven by a contol loop for which the transistors $T3$, $T4$ and $T5$ are added. $T1 + T3$ and $T4 + T5$ form a current mirror : they have same base

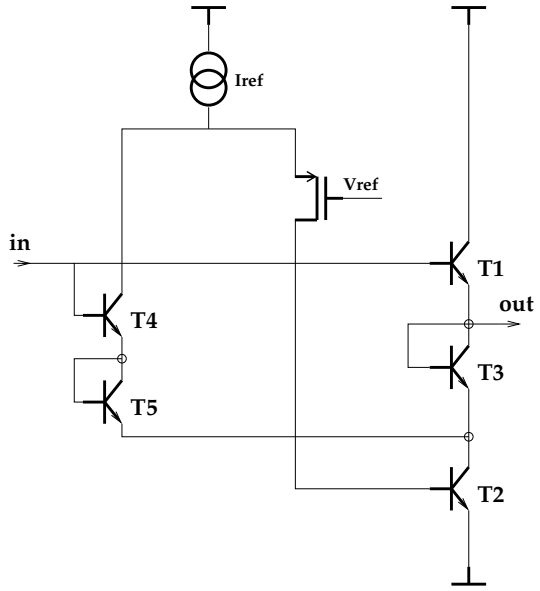


FIG. 15 – buffer design

and same emitter voltage. A fraction of the output current, determined by the size ratio of $T1$, $T3$ and $T4$, $T5$, is "measured" by $T4 + T5$ and subtracted to I_{ref}. The part of Iref which is not taken by $T4$, $T5$ is apply to the base of $T2$ by the PMOS transistor.

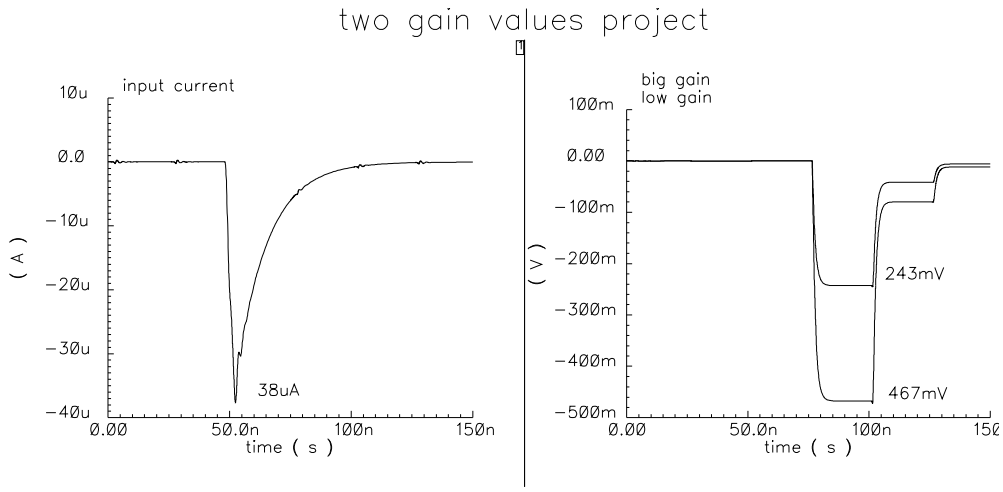
It is easy to verify that this feedback is stable : if a positive signal occurs, the current of $T1$ increases, its V_{be} increases and then the V_{be} of $T4$ and $T5$ increase. As a consequence, more current is taken to I_{ref} by $T4$ and $T5$ and the current given to $T2$ by the PMOS decreases to allow the output voltage to increase. The same analyze is easy to do with a negative going signal. The simulation confirms that this circuit is a true push pull. It is interesting to notice that the current feedback parameters are not critical at all, and very easy to adjust. It is also interesting to notice that the maximum dynamic range we can reach is only limited by the power supply and the lost of two V_{be} ($T1$ and $T3$), exactly like in a complementary Push Pull. The following table shows the results which could be easily reached with this output stage for 3 different quiescent currents :

power supply	quiescent currents	linearity error on 2 volts	rise time
$\pm 2.75\,V$	25 mA	2 mV max	2 ns
$\pm 2.75\,V$	16 mA	5 mV max	3.5 ns
$\pm 2.75\,V$	12 mA	8 mV max	5 ns

For our application, we chose to operate at 16 mA. Notice that, as explain before, the 5 mV non linearity error was corrected in the parallel compensation of the previous stage to reach, in simulation $\pm 100\,\mu V$ error with the two stages together.

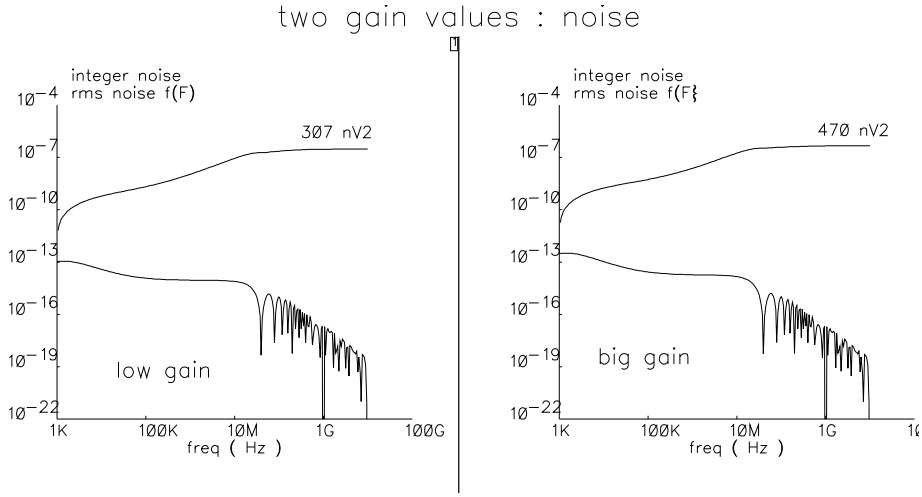
IV. Simulation results

1.- gain



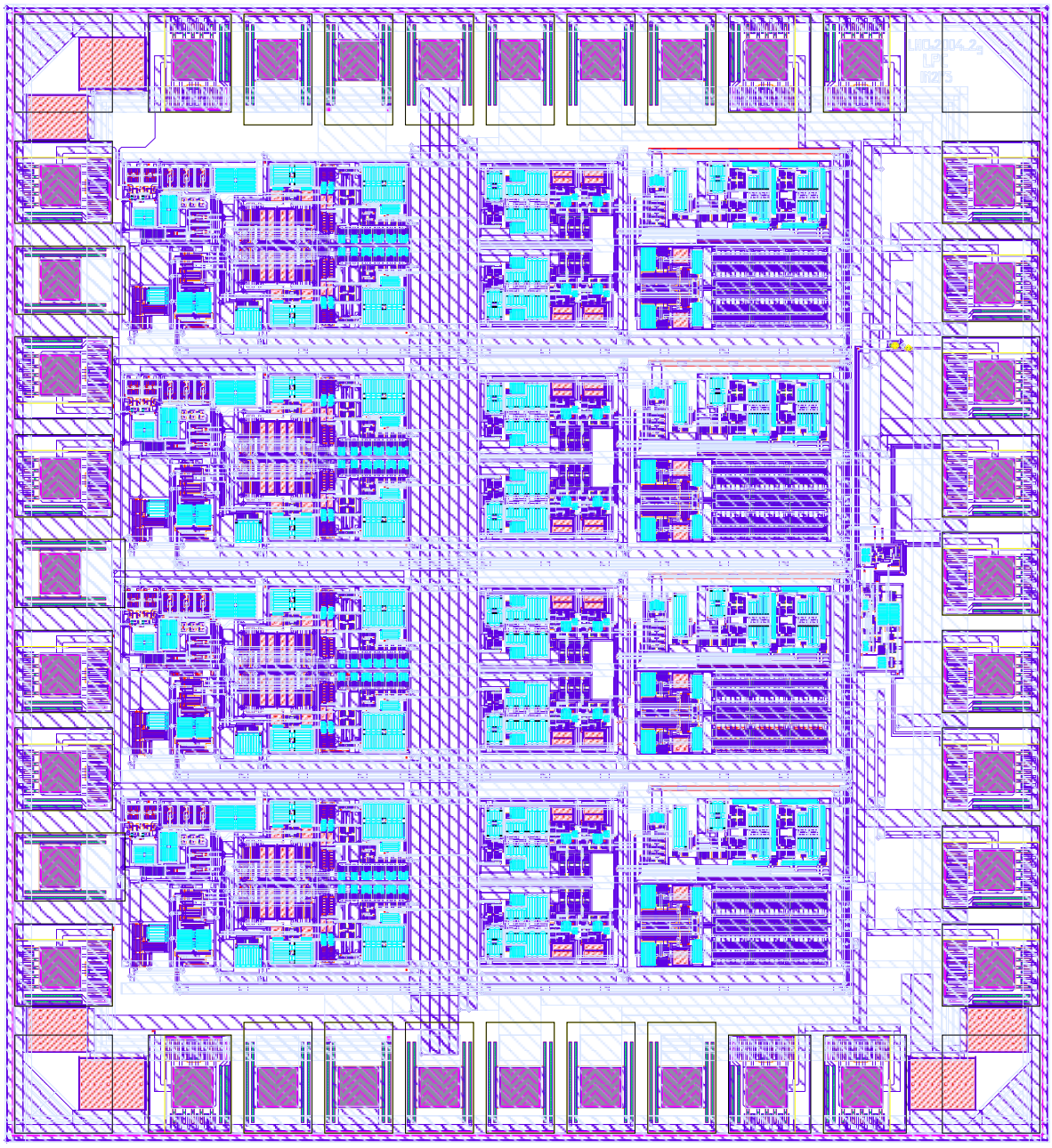
The gains are $\rho = 25.9\,k\Omega$, $\alpha = 17.1\%$ $\alpha_2 = 2.5\%$
and $\rho = 13.4\,k\Omega$, $\alpha = 17.0\%$ $\alpha_2 = 2.5\%$.

2.- noise

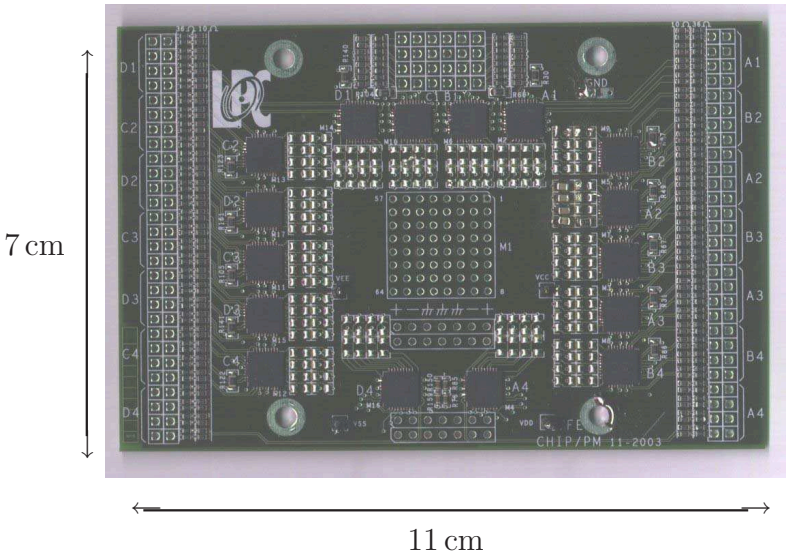


The low gain noise : $\sigma = 560\,\mu V$, it is correct.
The high gain noise : $\sigma = 690\,\mu V$, it is correct.

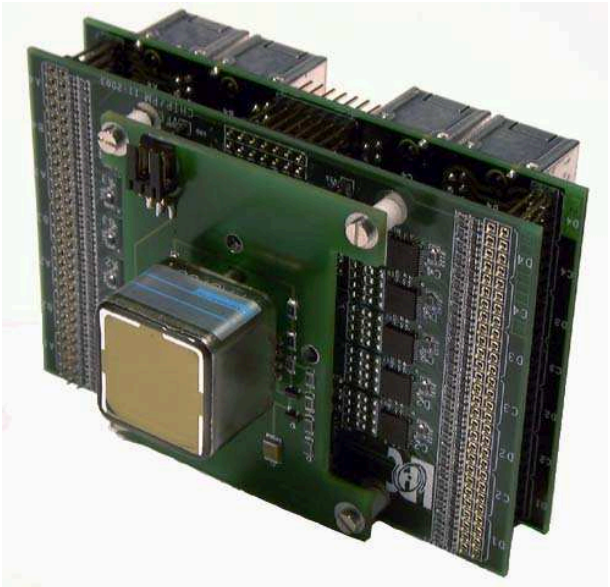
V. chip layout



VI. The VFE chip card



VII. The VFE board



VIII. CONCLUSIONS

The production of 6500 chips was terminated in april 2005. The results are in annexe.

Gain tuning is done by jumper at the VFE board and by soft ware at he FE board : by this way we can obtain a maximum variation gain of 4, which gis us a good safety margin against the gain dispersion fo the PMT channels.

Références

[1] Gérard Bohner and al., "LHCb Preshower Signal characteristics", LHCb note 2 000-026.

[2] Gérard Bohner and al., "A mixed analog/digital shaper for the LHCb preshower", Fifth worshop on electronics for LHC experiments, september 1 999, Snowmass.

[3] Pieter Vorenkamp, Johan P.M. Verdaasdonk. "Fully bipolar, 120-Msamples/s 10-b Track and Hold Circuit." IEEE journal of solid-state circuits, July 7, 1 992.

[4] Jean-Marie Bussat, thèse de doctorat "Conception d'un dispositif d'acquisition rapide de grande dynamique..." 5 juin 1 998.

[5] *http ://lhcb.web.cern.ch/lhcb*, calorimeter agenda, electronic review.

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