Testing of LeCroy 1877S TDCs

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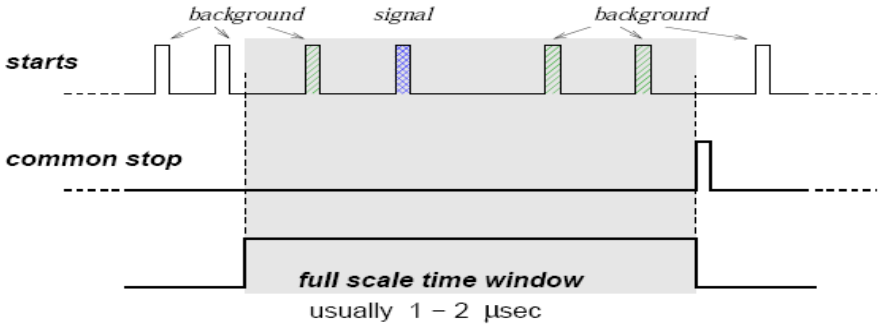
Hall A Group Meeting

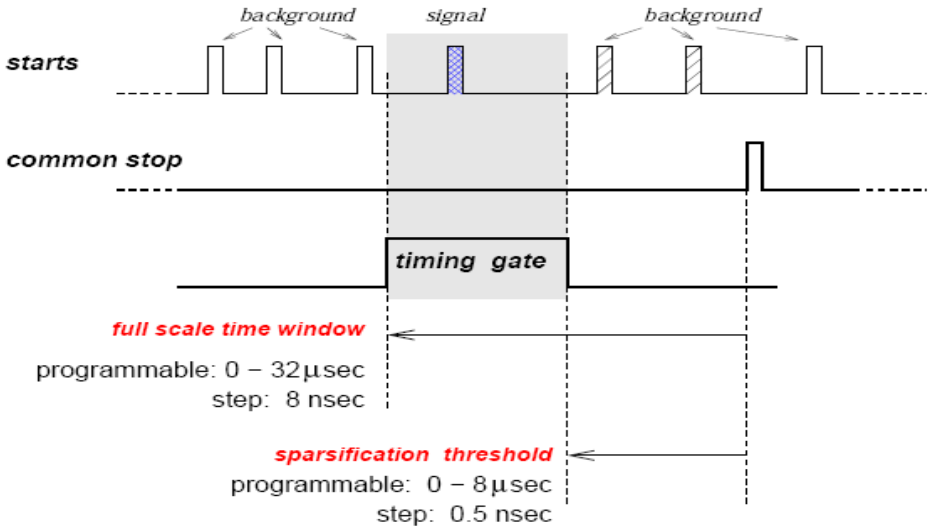
November 29, 2011

Sparsification

1877S TDC running in common stop mode **without sparsification**

- Constantly accepting start signals
- When STOP arrives it looks back the length of the full scale time window to find all signals inside of the window

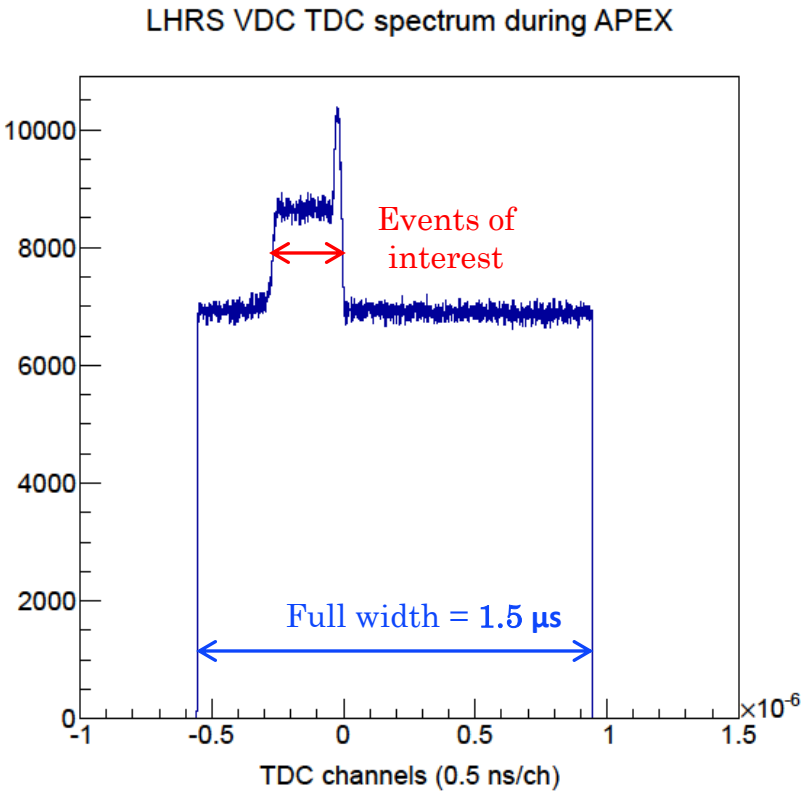




1877S TDC running in common stop mode **with sparsification**

- Still a full scale time window
- Sparsification threshold which gives the TDC a time after which no new start signals should be recorded

Why Sparsification?

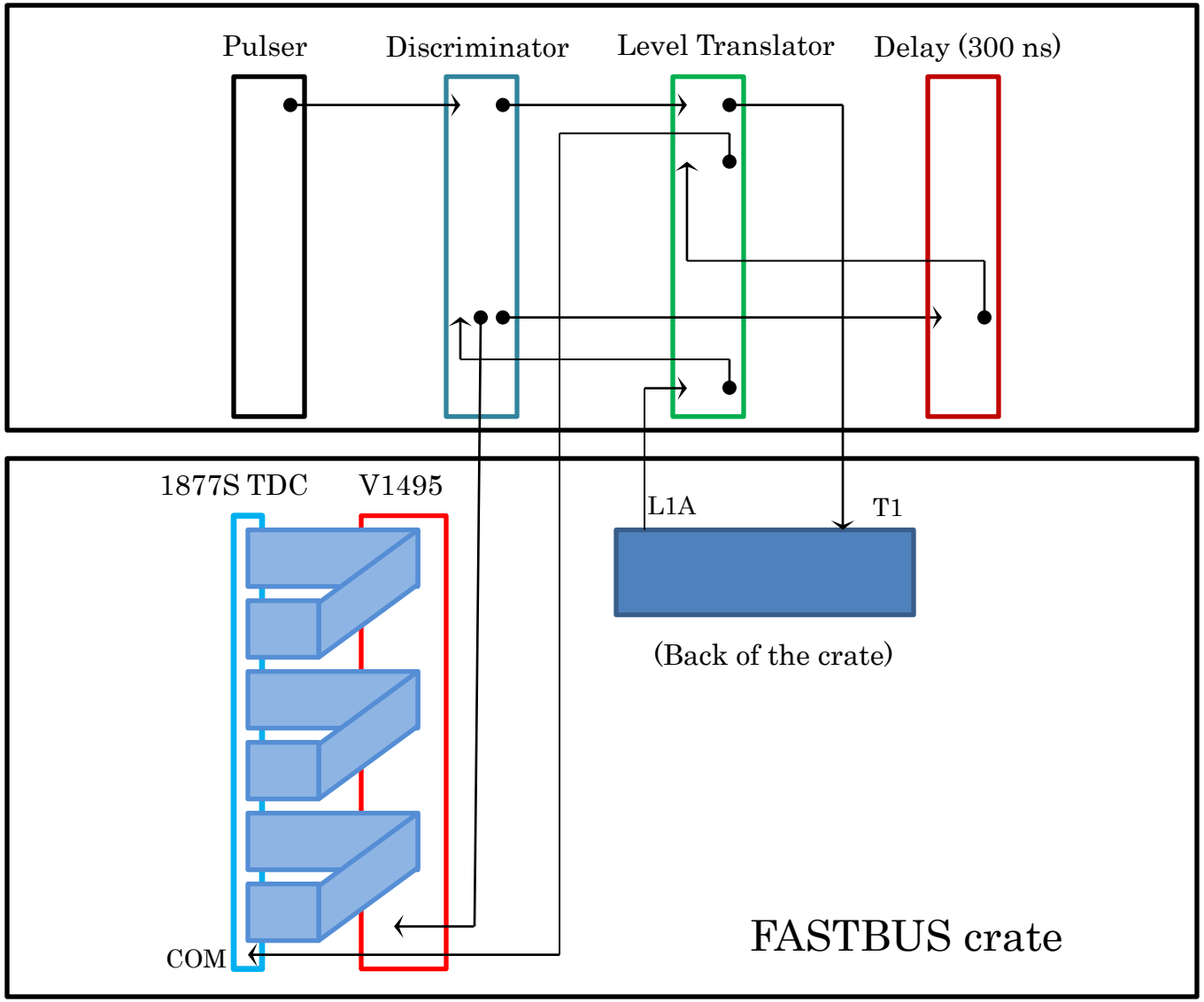


- Reduces deadtime
- Reduces quantity of undesired data

BigBite TDC spectrum is even worse!

Region of interest is only 10% of total spectrum

Test Setup


Pulser
Discriminator
Level Translator
Delay (300 ns)
1877S TDC
V1495
L1A
T1
(Back of the crate)
COM
FASTBUS crate

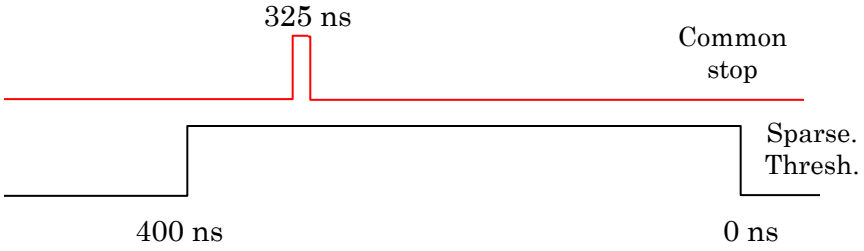
Readout Lists and Configurations

Each TDC is tested with 3 different CRLs (CODA Readout Lists)

Common stop from pulser is delayed by 325 ns

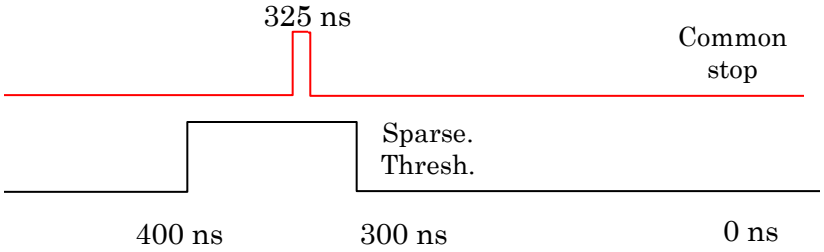
Sparsification CRL #1

Full scale time window = 400 ns
Sparsification threshold = 0 ns



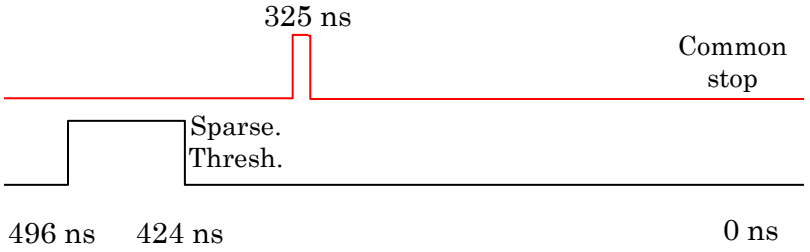
Sparsification CRL #2

Full scale time window = 400 ns
Sparsification threshold = 300 ns



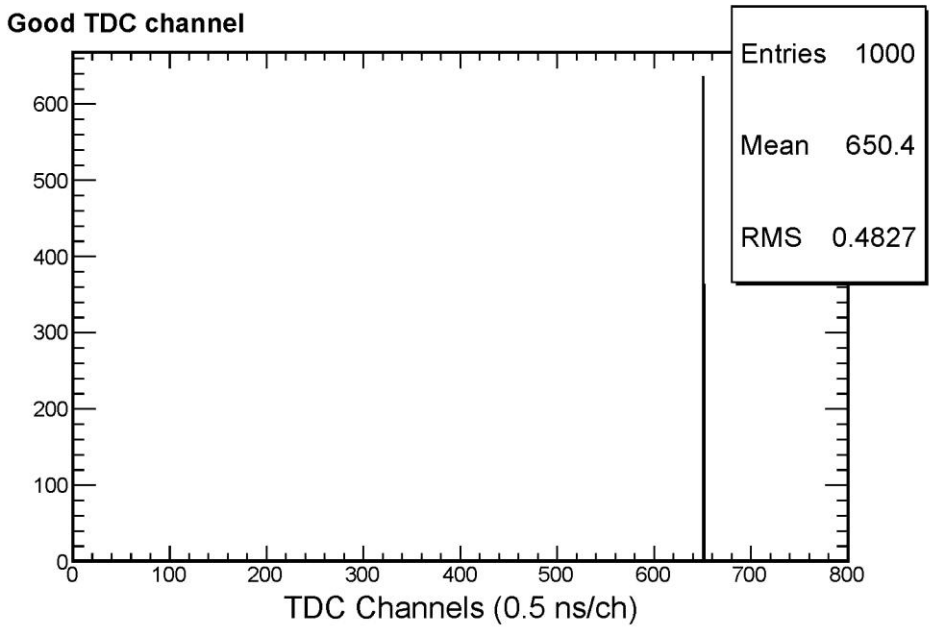
Sparsification CRL #3

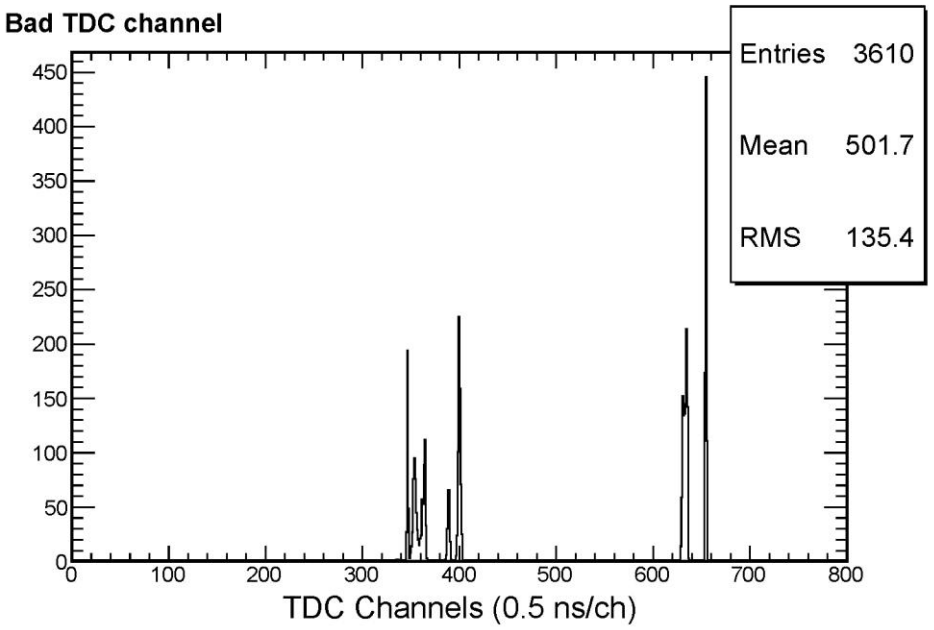
Full scale time window = 496 ns
Sparsification threshold = 424 ns



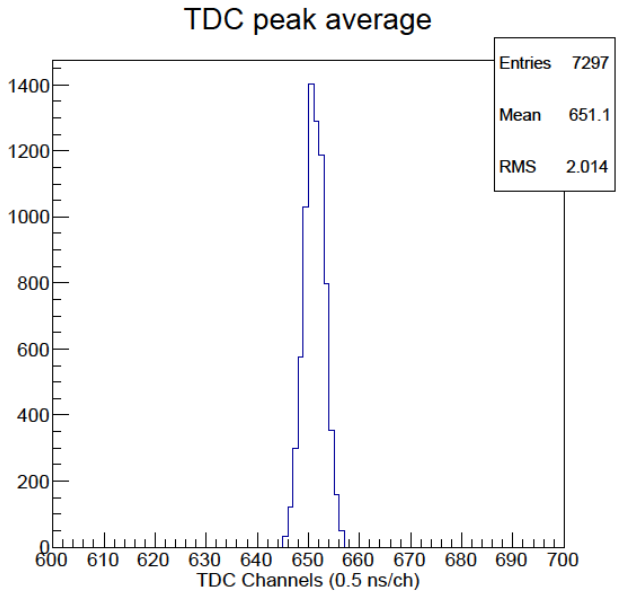
Results

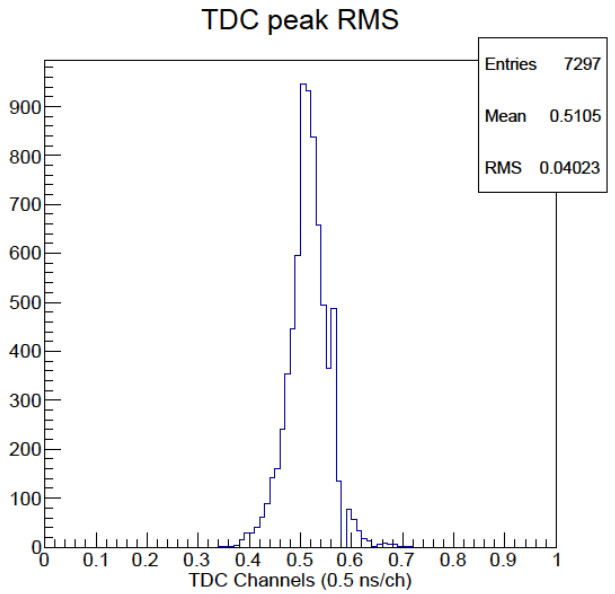
- The first 2 sparsification tests should provide each TDC channel with a sharp peak around 650 (325 ns) containing exactly 1000 events
- A TDC channel is considered to be bad if it has:
  - Extra or missing events
  - An RMS value > 0.8 channels
  - A peak location outside of the range 640-660 channels
- The TDC channels should see 0 hits for the 3rd test
- A total of 42 TDCs have been fully tested, out of which 4 have bad channels





Results





All TDCs that have been tested have been labeled with new barcode labels.

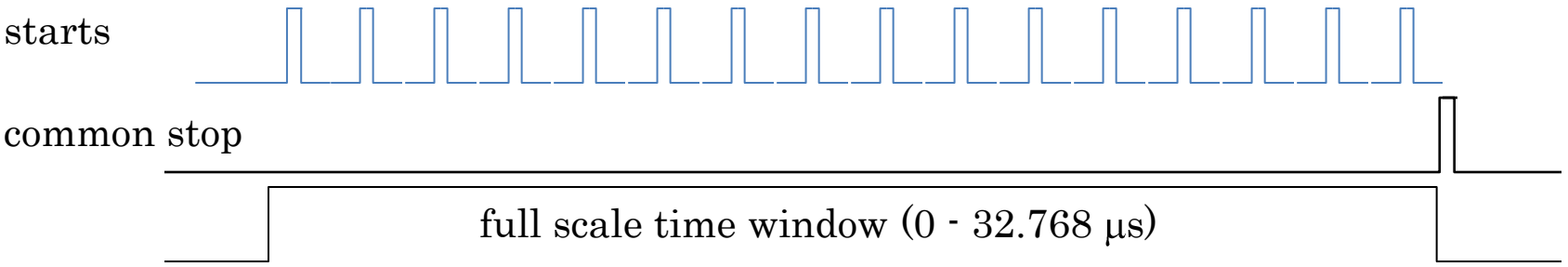
Still have ~100 TDCs that need testing.

Daniel Kirby
Alexandre Camsonne
Ben Raydo
Bogdan Wojtsekhowski

Thank you!

1877S

- Provides 96 channels of time-to-digital conversion
- 0.5 ns least count
- Can be programmed to store 1 - 16 hits per channel within a 0 - 32.768 μs full scale window.
- Selected edges can be detected with as little as 10 ns between them



Capable of running in sparsification mode

V1495 FPGA Output

The FPGA (Field Programmable Gate Array) module accepts a pattern into an internal register

The pattern is then fired according to an incident pulse signal (in our case coming from the pulser)

Using A395C daughtercards to output ECL signals

Ribbon 1/3/5

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Ribbon 2/4/6

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Numerical Value: 65537

After 1000 events

Ribbon 1/3/5

0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Ribbon 2/4/6

0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Numerical Value: 131 074