Flash ADC in HRS

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JLab Pipelined Flash ADC

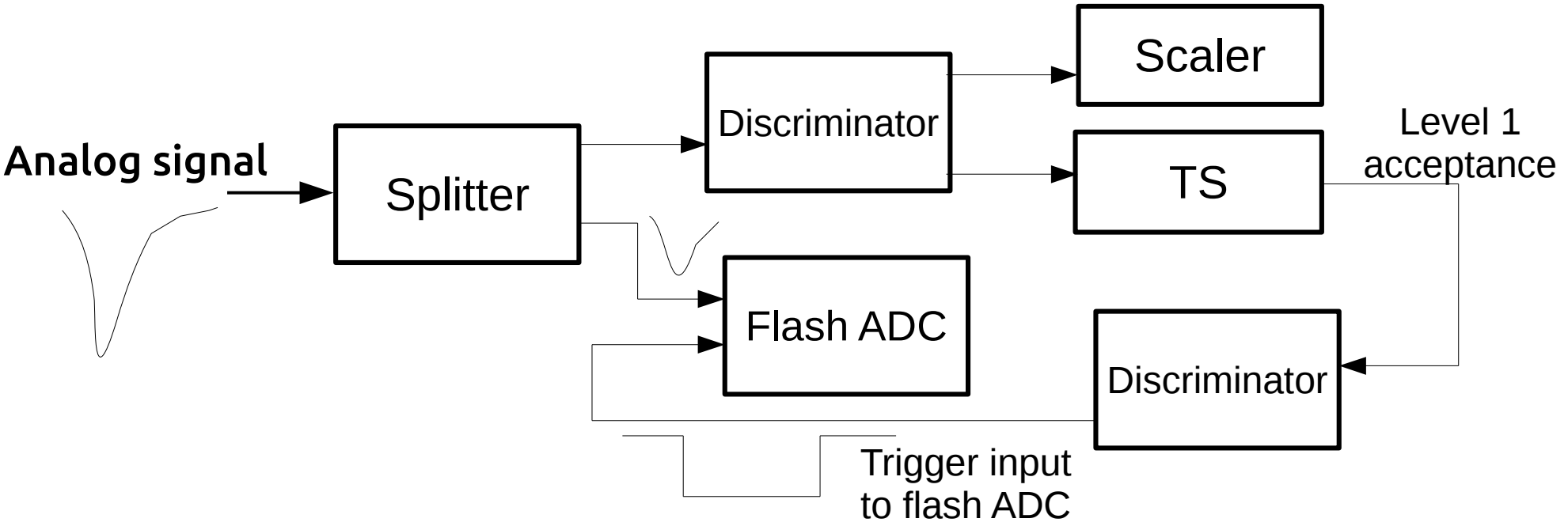
- 16 channel 250 Msps flash ADC
- 8 μs raw sample pipeline
- Can be operated in raw data mode or pulse integral mode

Merits:

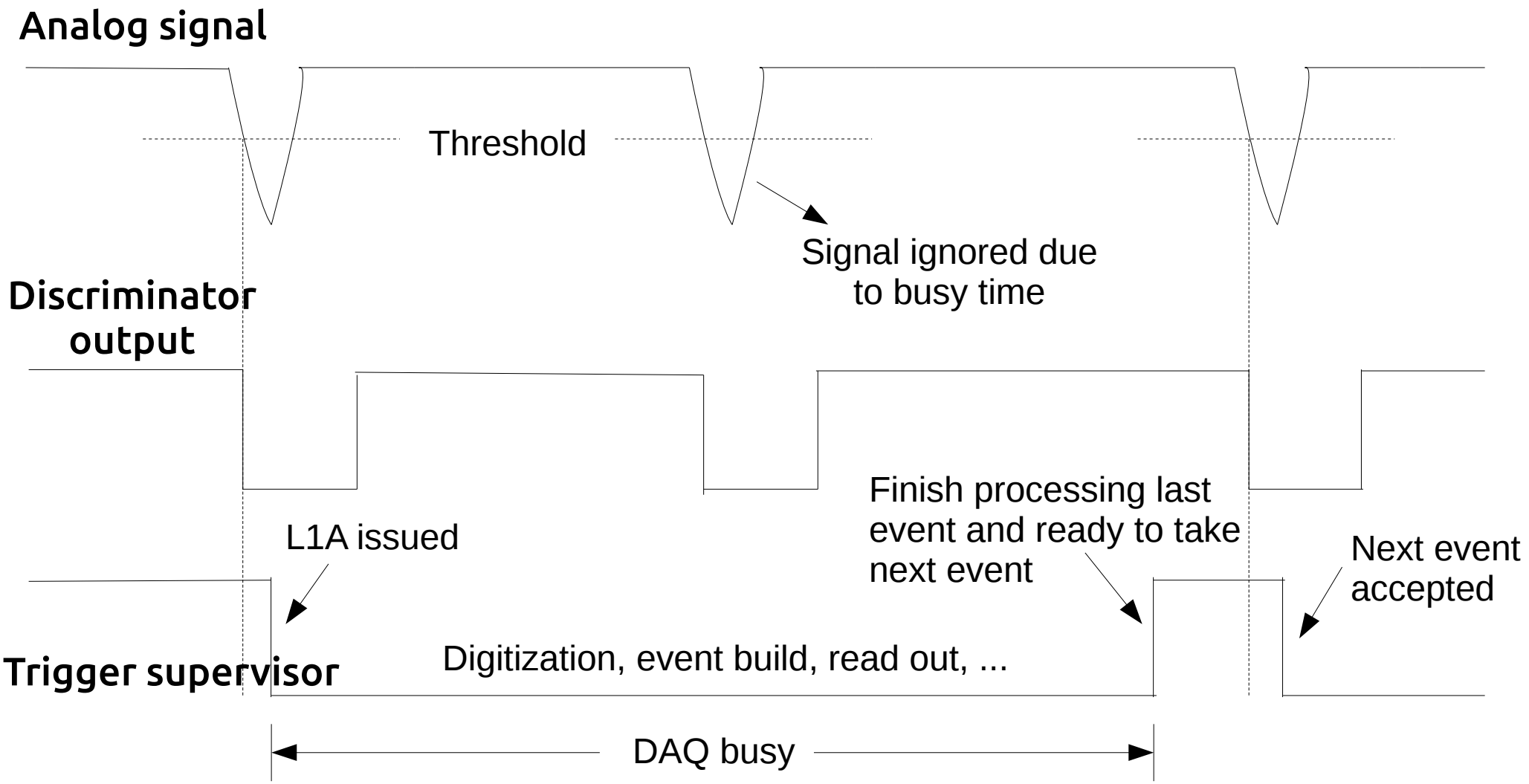
- High rate capability
- Avoid delay cables
- No extra TDC needed for that channel
- Pulse form discrimination
- Incorporate signal processing features, trigger processing, and event buffering ...

Flash ADC Test: Setup

- Two VME crates on each HRS arm: one with TS and scalers; the other one can be used for VME-based ADCs and TDCs
- Flash ADC installed in the second VME crate (ROC 31)
- A CODA configuration was created to include the 2 VME crates and read the flash ADC data and scaler data; TS produces trigger for flash ADC and controls data readout

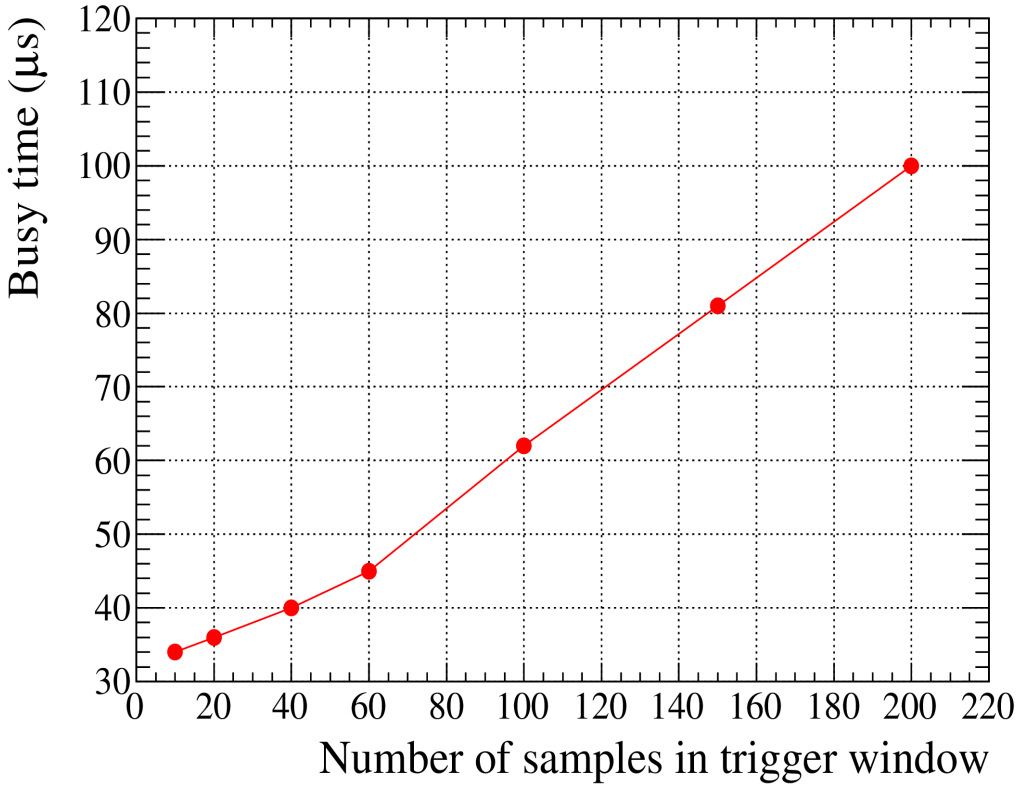


Flash ADC Test: Busy Time

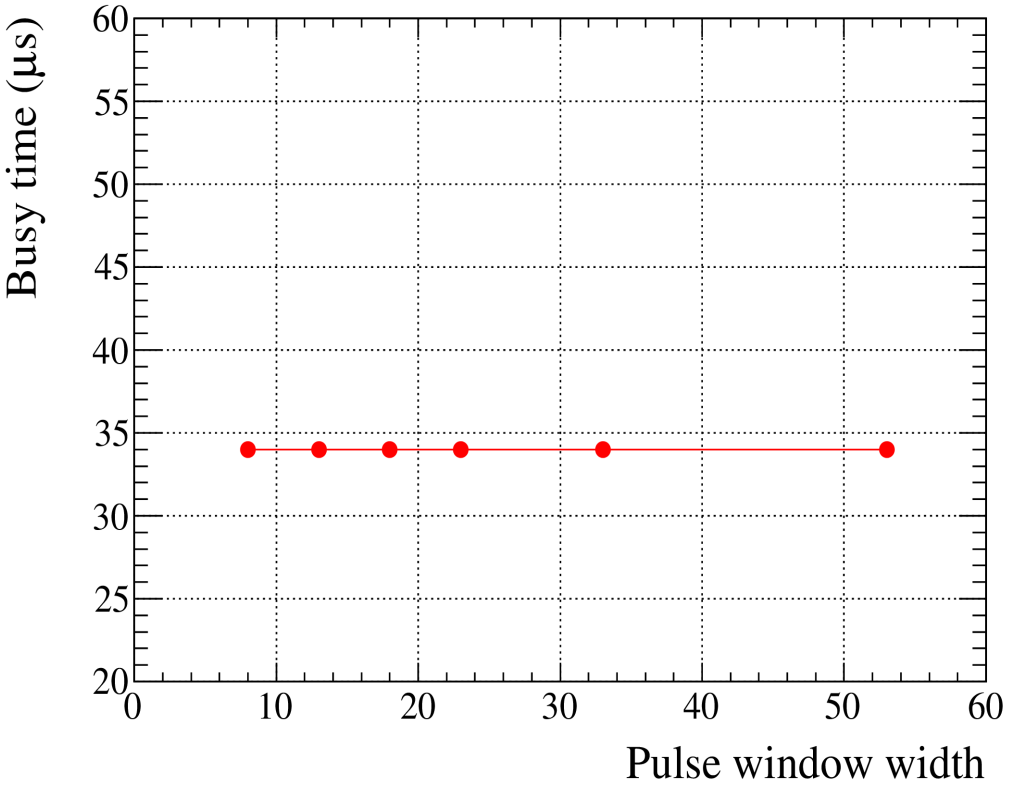


Flash ADC Test: Busy Time

Raw data mode



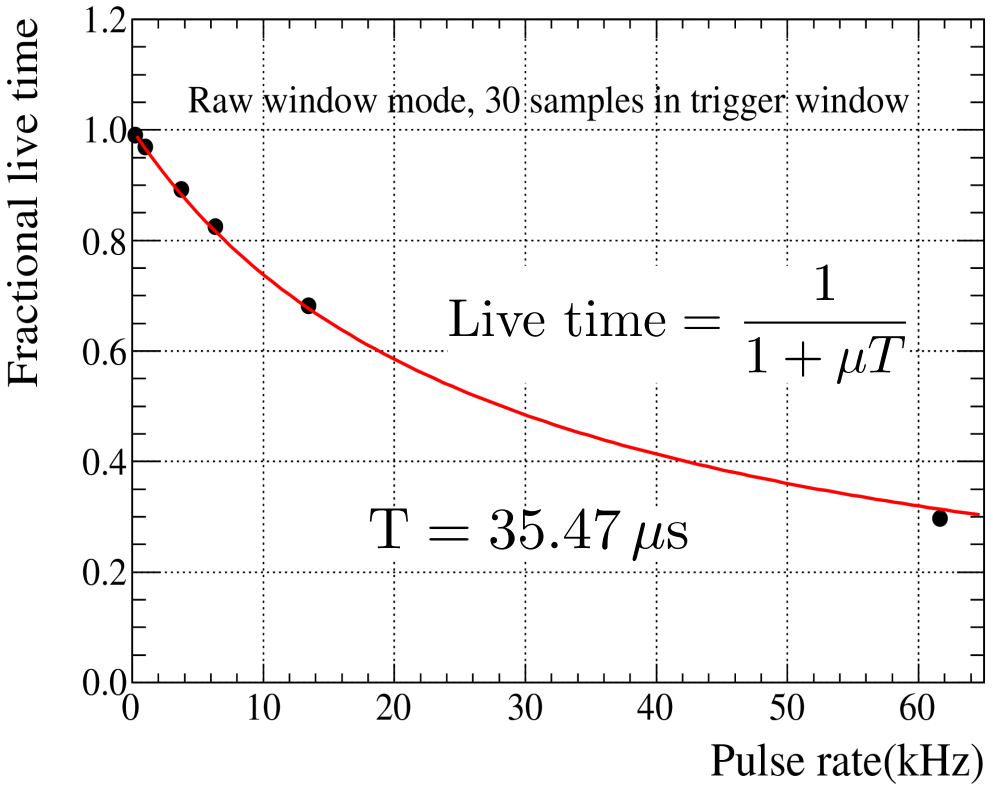
Pulse integral mode



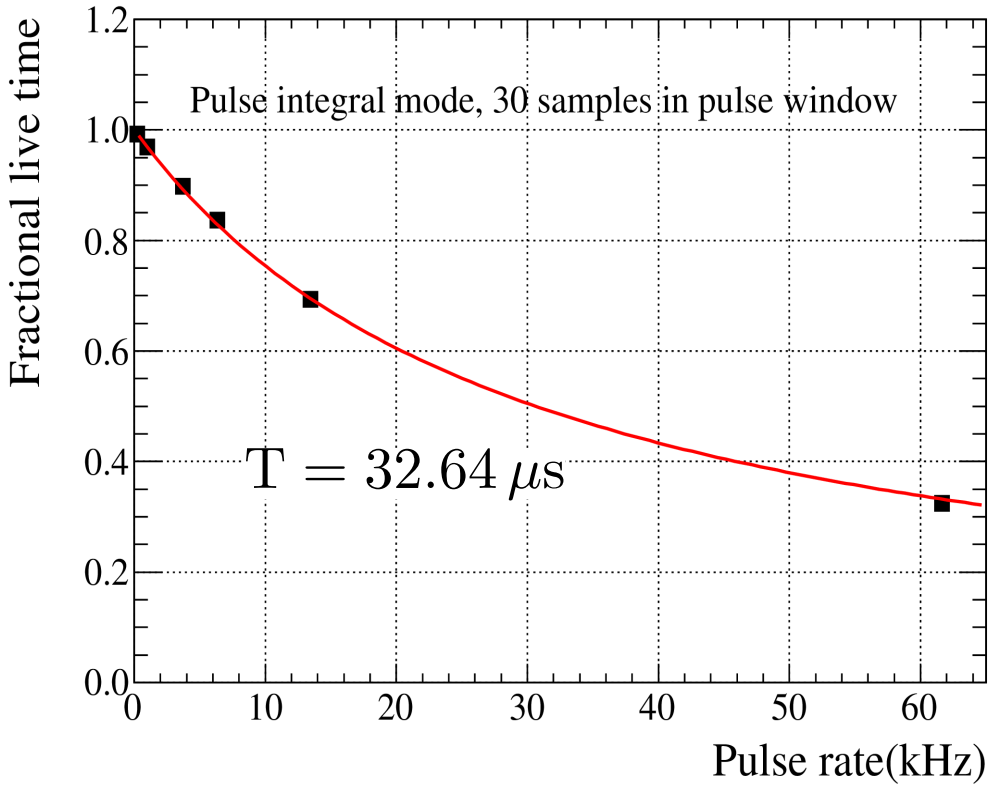
The busy time shown here is from the width of L1A or Busy output signal of TS

Flash ADC Test: Live Time

Raw data mode



Pulse integral mode



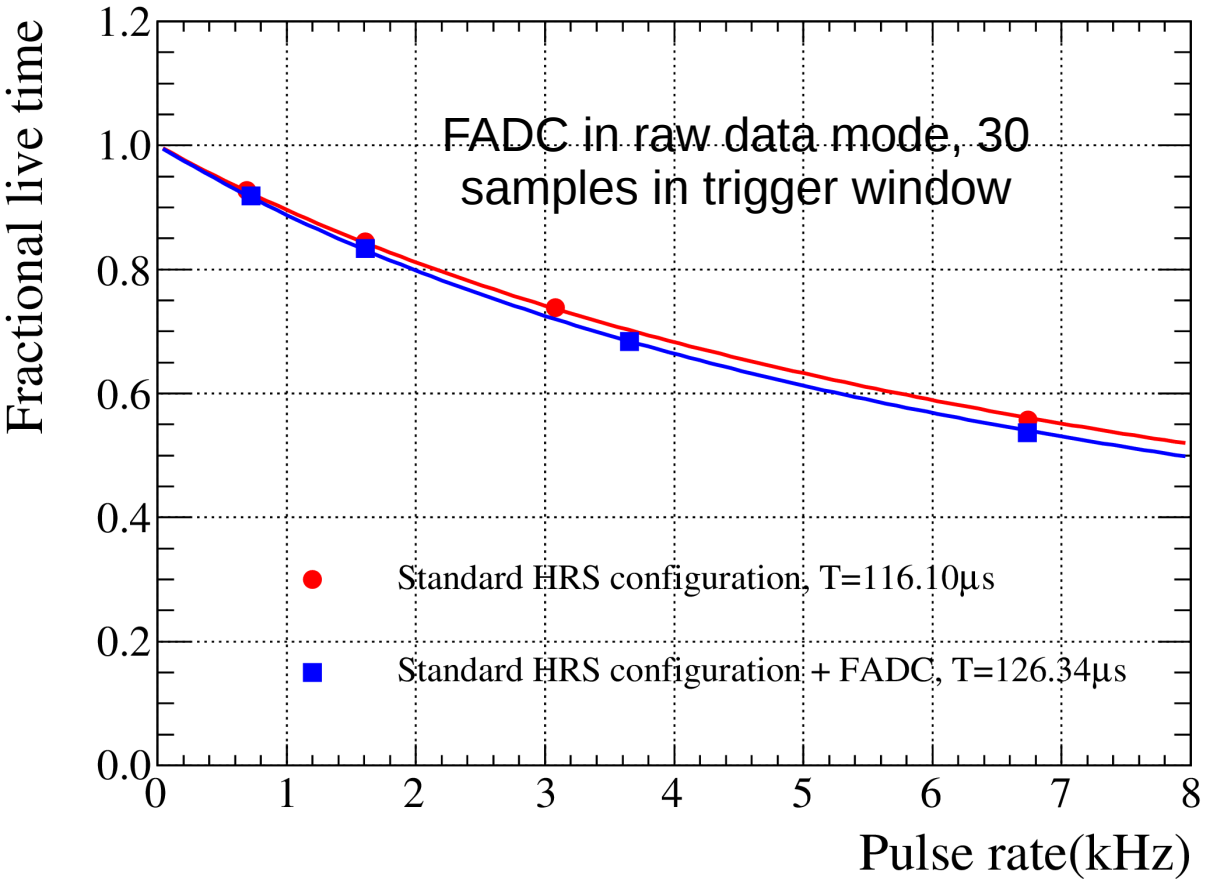
- Fractional live time = #events recorded by CODA / #events in scaler
- Events are generated by random pulse generator

Busy time consistent with visual reading from oscilloscope

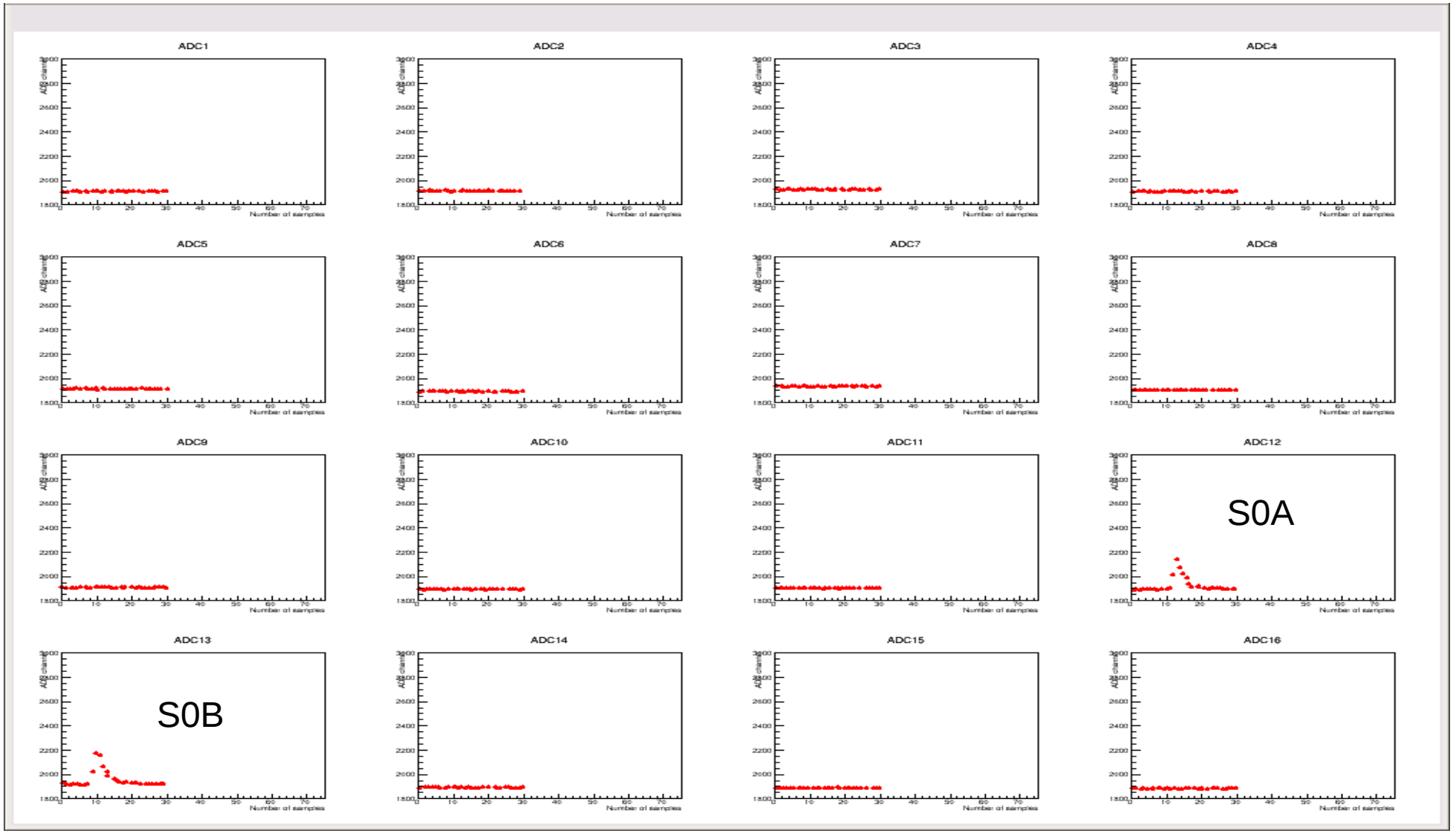
Incorporation of FADC in Standard HRS DAQ

- Detector signals from Cherenkov PMTs and S0 scintillator are fed into flash ADC
- Created a CODA configuration where flash ADC is read in paralell with fastbus ADCs and TDCs

- The addition of flash ADC does not affect the DAQ capability significantly (as we expected)
- The slight increase in busy time can be attributed to the additional data to be processed by EB, ET and read out



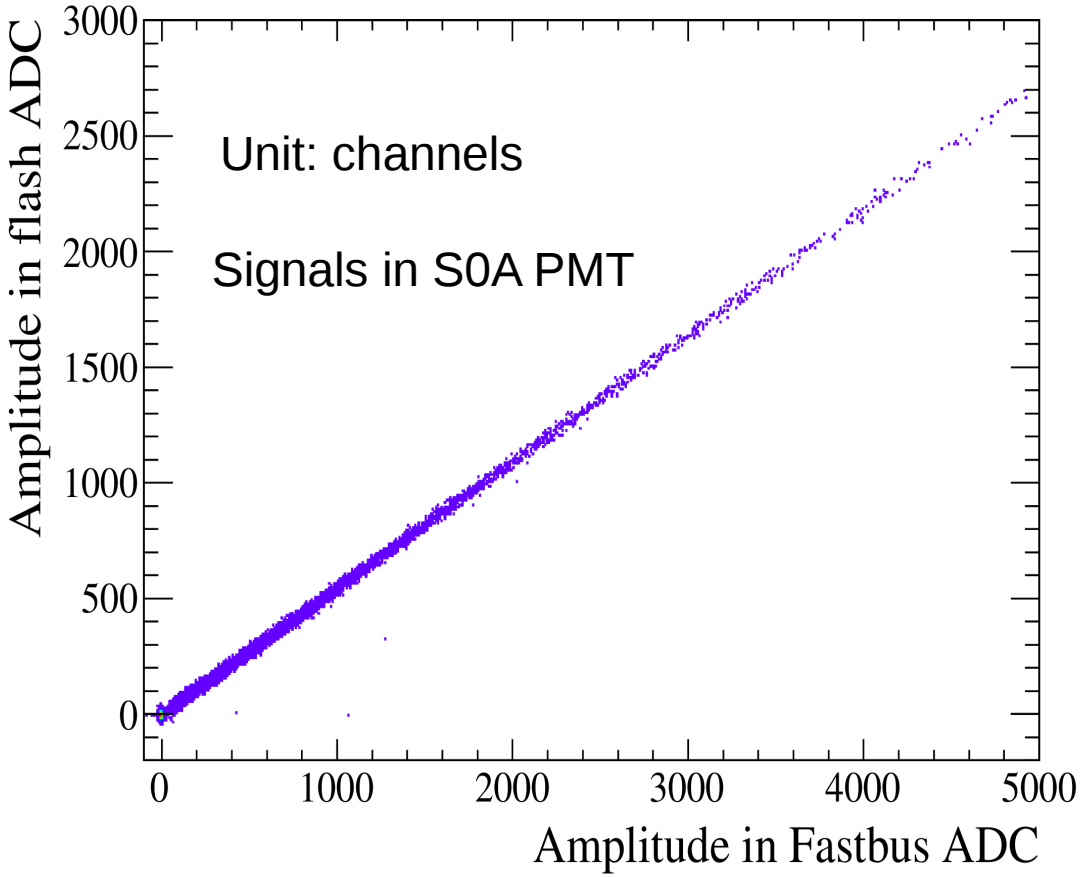
Snapshot



Useful tool for online diagnostics

Fastbus ADC vs. Flash ADC

- Signals from the same detector, but the branch sending to flash ADC is attenuated to 1/6
- Two outputs gives fully correlated result
- Flash ADC has a better sensitivity to signals (about 3 channels/mV)



Conclusions:

- Advantages of flash ADC: pipelined data processing and storage, high rate capability, pulse form visualization, trigger logic implemented, …
- Random pulse study indicates no degradation in capability or performance of HRS DAQ with installation of flash ADC
- A useful tool for GMp experiment and also future high rate experiments

Future work:

- ➔ Check DAQ and flash ADC performance with electron events
- ➔ Develop analyzer-based replay script for flash ADC

HRS DAQ info:
http://hallaweb.jlab.org/12GeV/experiment/E12-07-108/DAQ/HallA_hrs_daq.pdf