Hall A Moller Polarimeter DAQ Upgrade

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PREx Collaboration Meeting Feb. 18–19, 2010

Overview

- What do we gain from the DAQ upgrade?
- What does the DAQ upgrade involve?
 - Hardware description
 - Capabilities
 - Trigger definitions
- What is the present status of the upgrade?
 - Some plots of production data with extracted asymmetries
 - Todo list...

Why do we want the DAQ upgrade?

- Help improve the systematic error from $2\% \rightarrow 1\%$
 - FADC data grants full information about detector systematics/performance
 - Negligible DAQ deadtime (pipelined design)
 - Intrinsic HW deadtime (ie. pile-up) can be trivially identified/measured using sample data
- Replace old/obsolete DAQ hardware
 - existing DAQ is 12 years old, no spares, rate limited
 - FADC design is fast & flexible
- Accommodate the new segmented aperture detector
 - 8 paddles (4 per arm) instead of 2
 - present aperture paddles overload at > luA

What is involved in the DAQ Upgrade?

- System built around a JLab F250 Flash ADC
 - 16 analog inputs (8 calo. blocks, 8 scint. paddles)
 - 4 ns sample time, 12 bits/sample resolution
 - FPGA device → flexibility of software with the speed and response time of hardware
- Custom FADC firmware
 - FADC generates our triggers, no signal splitters, discriminators, or summing modules needed
 - Thresholds, sample windows, trigger prescales all software controlled
 - Fairly straight forward to add new features to the firmware (turn around on the order of a week)

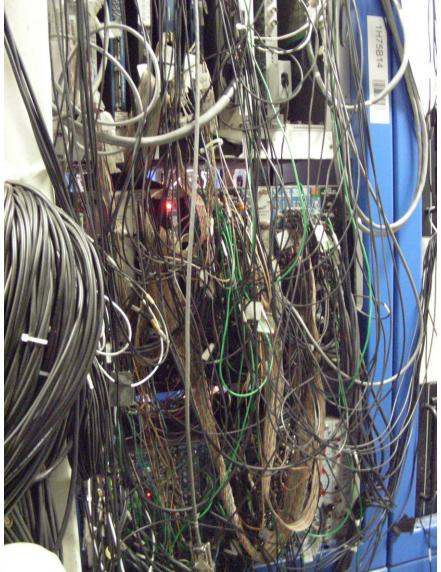
What is involved in the DAQ Upgrade?

- Also some auxiliary support modules (read out during every MPS interval)
 - CAEN v560 scaler (16 channels)
 - BCM, Moller target position, 100 kHz clock
 - (plus redundant counters for cross checks)
 - CAEN v792 QDC (16 channels)
 - MPS, QRT, HEL flags
 - (plus redundant data for cross checks)
 - Easy to add/read other modules if needed

What is involved in the DAQ Upgrade?

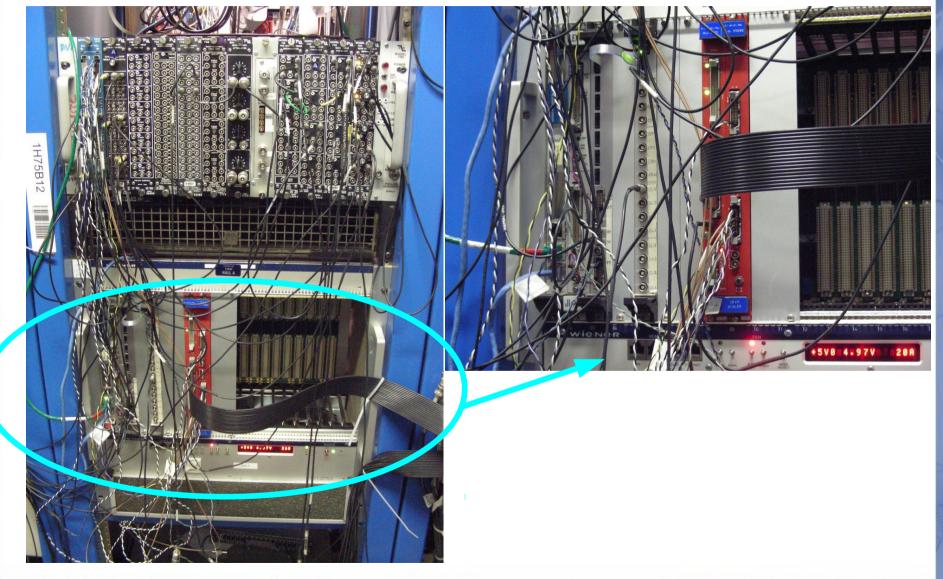
- New dedicated DAQ computer: hamoller.jlab.org
 - fast, modern machine: 4 CPU cores, 2TB of RAID10 storage for local data and scratch
 - shares adaqfs file system, usual accounts
 - goal is to support zero-deadtime streaming data from DAQ at full 160kHz coincidence rate (no prescaling) → sustained ~50 MB/sec
- ROOT-based analyzer using PODD (Hall A analyzer framework)
 - new decoding routines added to handle FADC
 - still a work in progress, but quite functional

Photo of old DAQ electronics



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Photo of new DAQ rack



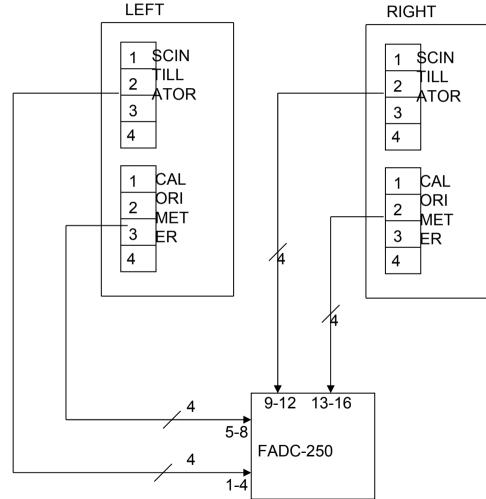
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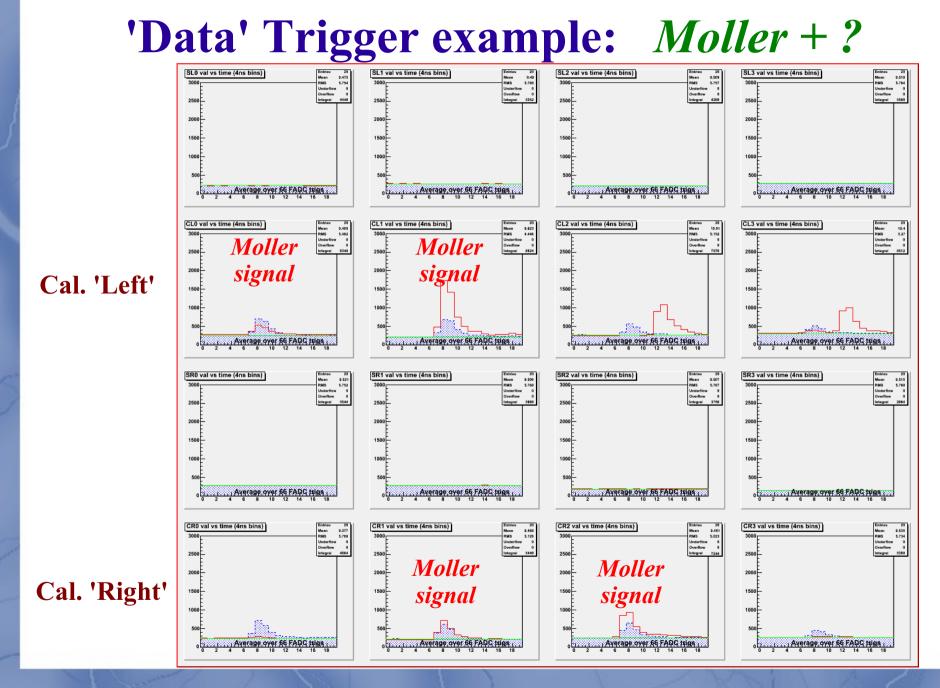
FADC internal trigger criteria:

$CR = \Sigma_{\neq 4} \sum_{j \neq 2} P_{j}^{J} > threshold$	
CL = $\Sigma_{\mu_4} \sum_{j \neq 2} P_j^{J}$ > threshold SL = ($\Sigma_{J \neq 2} S1^{J}$ > thr) or (Σ J=1,2 S2^{J} > thr) or (Σ J=1,2 S3^{J} > thr) or (Σ J=1,2 S4^{J} > thr)	
SR = $(\Sigma_{J=2} S5^{J} > thr)$ or $(\Sigma J=1,2 S6^{J} > thr)$ or $(\Sigma J=1,2 S7^{J} > thr)$ or $(\Sigma J=1,2 S8^{J} > thr)$	
 'DATA' Trigger (OR of 'internal' trigger cond:): CL.AND.CR prescaled from 1 to 2000 CL prescaled from 1 to 2000 CR prescaled from 1 to 2000 <i>Information recorded:</i> digitized waveforms helicity state status counters, etc. 	
 'HELICITY' Trigger (external trigger): MPS leading edge (30 – 2000 Hz) <i>Information recorded:</i> Helicity, MPS, QRT states, BCM, Moller Target ladder position information, 100 kHz clock, status counters, etc. FADC 'Software' scaler data: CL singles, CR singles CL and CR CL and SL CR and SR 	

- CR and SR
- CL and CR and SL and SR
- CL and CR and (SL and SR delayed > 100 ns)

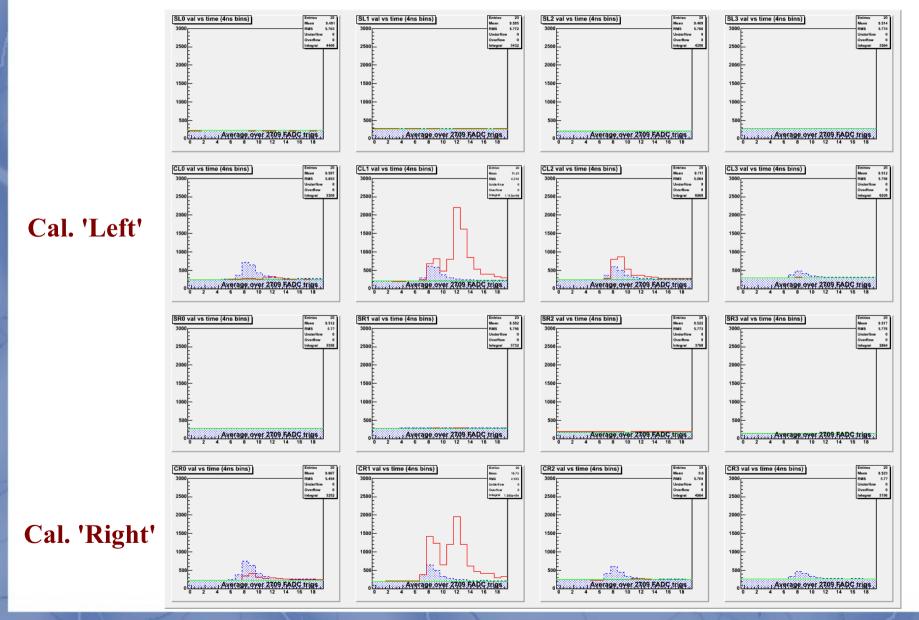
FADC Moller DAQ Trigger Types





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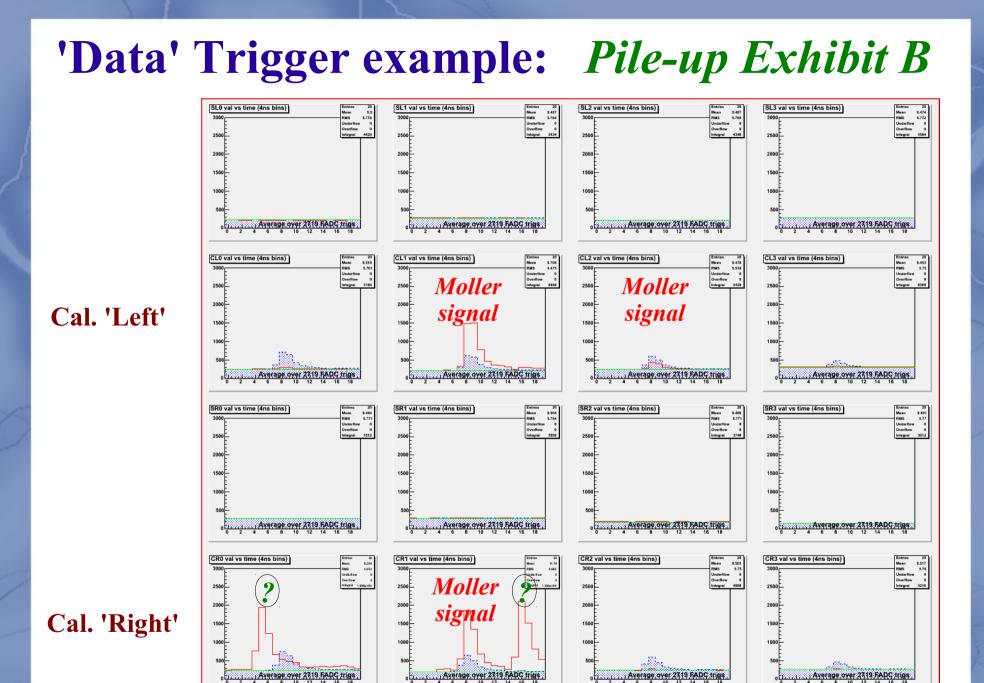
'Data' Trigger example: *Pile-up Exhibit A*



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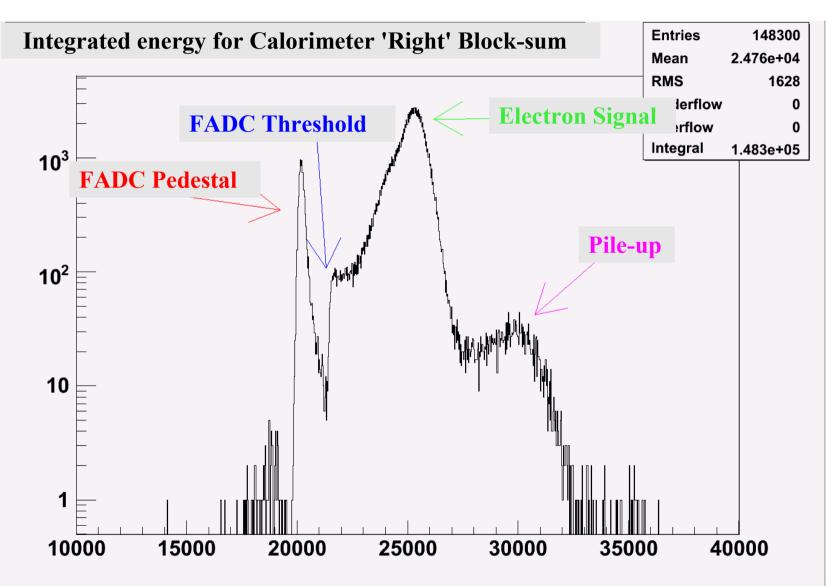
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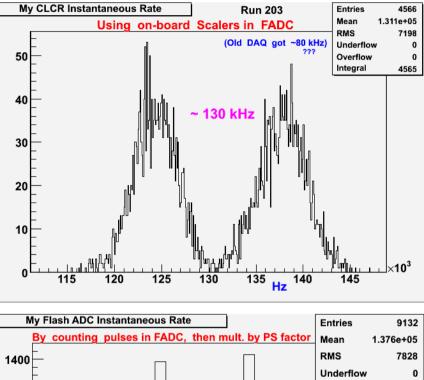


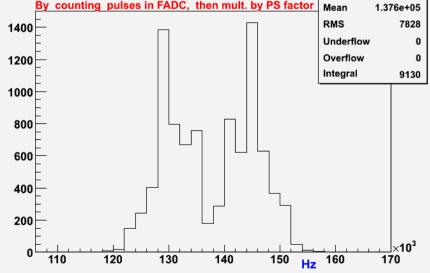
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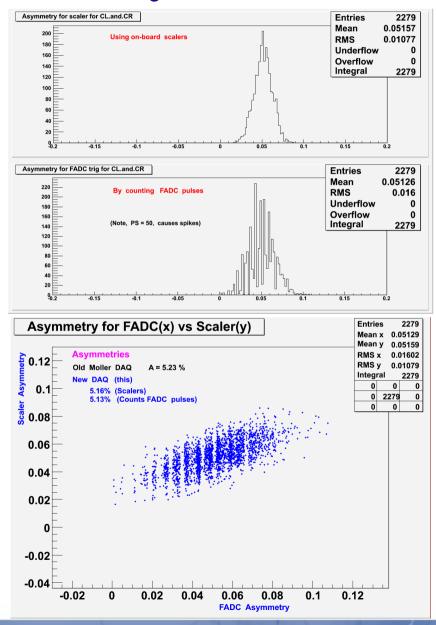
Total Energy Histogram



Rates and Extracted Asymmetries







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To Do List

• Add EPICS logger to CODA data stream

- Moller field status, BPM information, etc...

- Firmware bump w/ modified readout list will grant 50% bump in DAQ throughput ('background' DMA)
- Complete systematic hardware checks

• Ahmed's talk (Saturday)

- Continue to enhance analysis software
 - online data display (i.e. panguin style)
 - finish porting complete analysis algorithm from old PAW analyzer to ROOT analyzer (finalize all corrections, etc.)
 - Mindy's talk (Saturday)