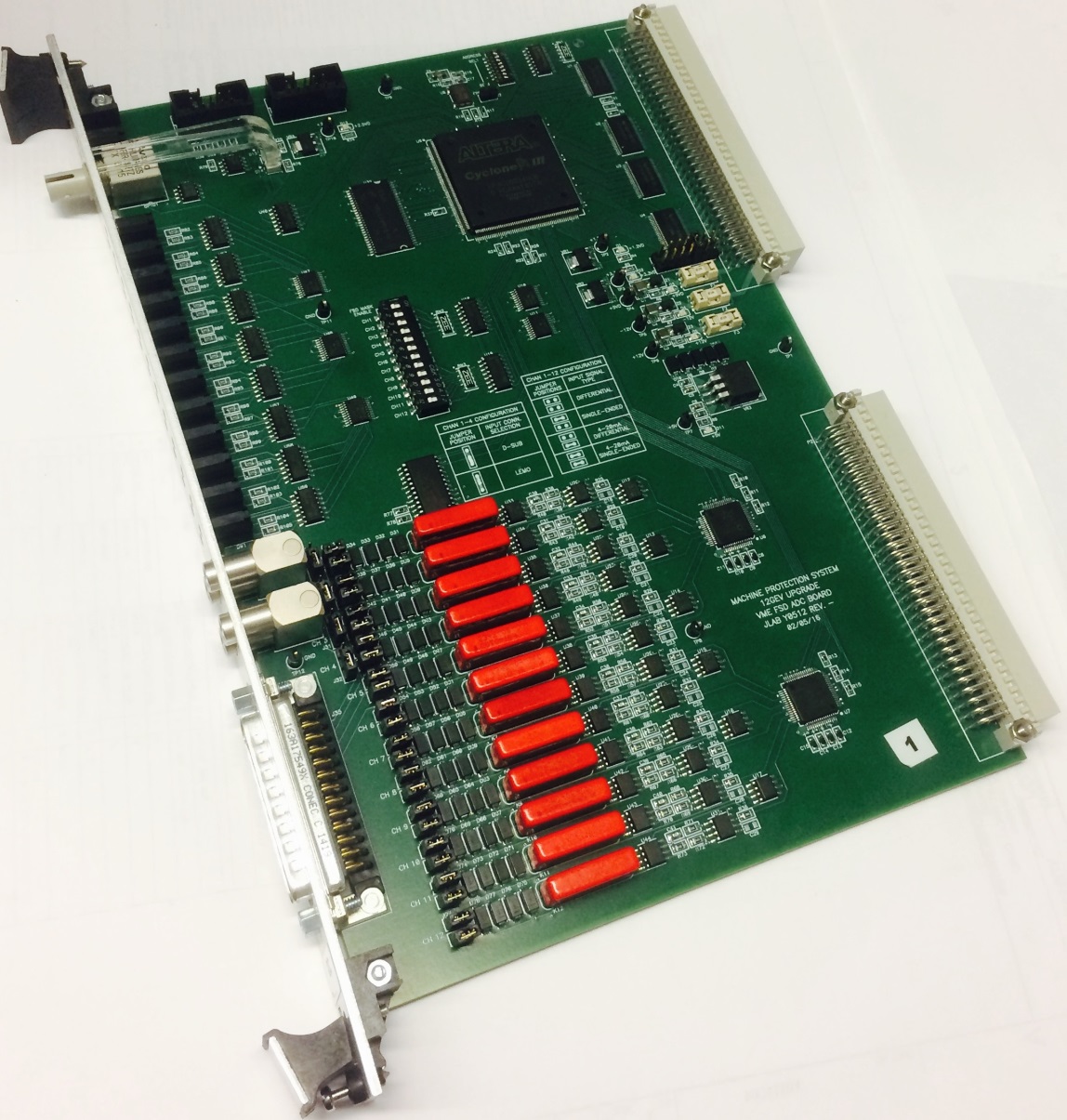
**Y0512 ADC FSD VME Board**

**User Manual**



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## Chapter 1: Introduction

**Description**

The ADC FSD VME board has one D-25 Male connector and 2 dual-LEMO connectors for 12 input channels. The input can be either 4-20mA current input or -10 to +10V voltage input.

## Chapter 2: Functional Descriptions

Two ADCs (AD7656) are used to simultaneously convert the 12-input voltages to digital data with a sample rate of 100K. The data will be compared to a window to generate a FSD signal. There are two kinds of windows: Normal Mode (Window) and Invert Mode (Window). At the Normal Mode, if the input data (RDBKxx) is between the Low Limit (LOLMxx) and High Limit (HILMxx), then there is no FSD (shown as Figure 1). If the data is beyond the Low Limit and High Limit window, then it starts to integrate the difference at an interval of 10 us. When RDBKxx > HILMxx, the equation is Chanx\_int = ; when RDBXxx < LOLMxx, the equation is Chanx\_int = . If Chanx\_int is higher than the Integrating Setting Limit (INLMxx), then it will generate an FSD (shown as Figure 2).

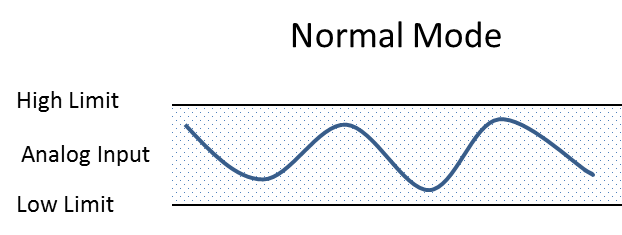


Figure 1 Normal Mode that input data is between the Low Limit and High Limit

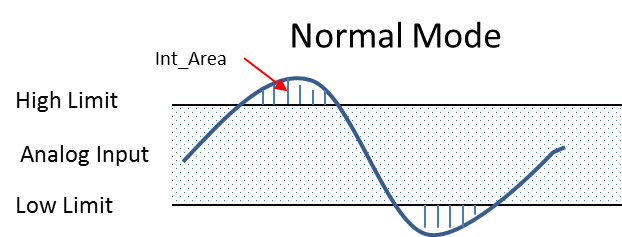


Figure 2 Normal Mode when input data beyond the window

At the Invert Mode, if the input data (RDBKxx) is beyond the Low Limit (LOLMxx) and High Limit (HILMxx), there is no FSD (shown as Figure 3). If the data is between the Low Limit and High Limit window, then it starts to integrate the difference at interval of 10 us. When RDBKxx > LOLMxx and RDBKxx < HILMxx, the equation is Chanx\_int1 = , and Chanx\_int2 = . If either Chanx\_int1or Chanx\_int2 is higher than the Integrating Setting Limit (INLMxx), then it will generate an FSD (shown as Figure 4).

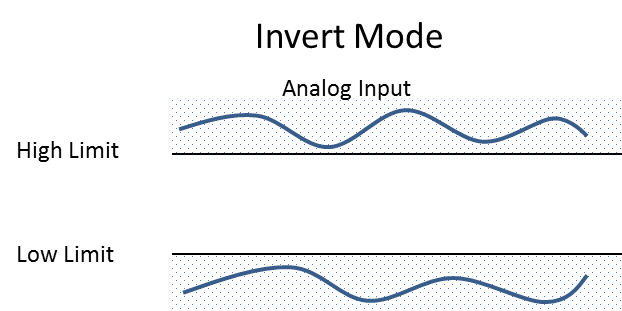


Figure 3 Invert Mode when input data beyond the window

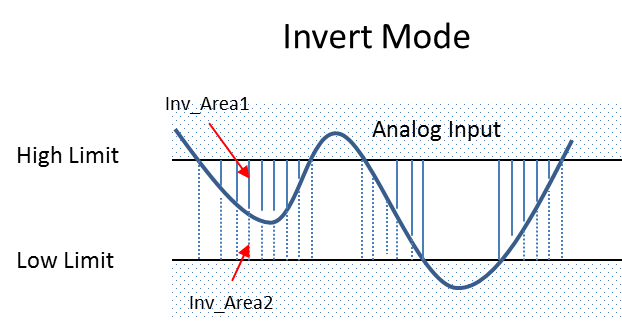


Figure 4 Invert Mode when input date in the window

## Chapter 3: Option Selection

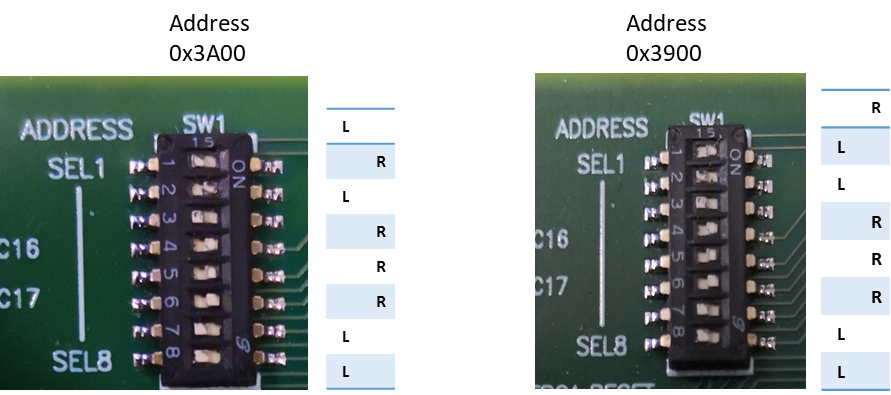
IRQ level jumpers and VME base address switches are available on the board. Current input and voltage input are selected by 12 jumpers

**Address Selection**

The board base address is set by an 8-channel switch SW1. The following shows the board base addresses (both VME short address and standard address) related to the switch (here VME Short Address is 0xFBFF0000). When a switch is OFF, the related address bit will be low (0) and ON will be high (1). The selected range of Short Address is from 0xFBFF0000 to 0xFBFF7F80, and the Standard Address will be from 0xFA000000 to 0xFAF00000.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Switch Pin | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |  |
| Short Address | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 |  |
| Standard  Address | x | x | x | x | A23 | A22 | A21 | A20 |  |
|  | | | | | | | | | |
| Switch State  P[8..1] | OFF | OFF | OFF | OFF | OFF | OFFF | OFF | OFF | Board Address |
| Short Address A[14..7] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0xFBFF0000 |
| Standard  Address[23..20] | x | x | x | x | 0 | 0 | 0 | 0 | 0xFA000000 |
|  | | | | | | | | | |
| Switch State  P[8..1] | OFF | OFF | ON | On | On | OFF | OFF | ON | Board Address |
| Short Address A[14..7] | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0xFBFF3900 |
| Standard  Address[23..20] | x | x | x | x | 1 | 0 | 0 | 1 | 0xFA900000 |

The following shows the switch pin positions for base address 0xFBFF3A00 and 0xFBFF3900.



**IRQ Selection and Interrupt**

The board can generate interrupts on the rising edge of a FSD and the Circular Buffer Done. The IRQ# is selected by jumper J1, IRQ 7 down to 1 from left to right. The Circular Buffer Done interrupt will be generated either by a FSD or setting the Stop Circular Buffer bit at Control Register.

Enable Circular Buffer Stop on FSD, CTRL(2)=1 and FSD, then Circular Buffer Done on Interrupt Status Register, ISTAT(5) = 1.

Stop Circular Buffer, CTRL(3) = 1, then Circular Buffer Done on Interrupt Status Register, ISTAT(5) = 1.

Here is how interrupt generates and Interrupt Service Routine works:

1. Setting bits on Interrupt Control Register (ICTRL), ICTRL(4)=1, ICTRL(5)=1, ICTRL(6)=1.
2. When an interrupt generates, check the bits on the Interrupt Status Register (ISTAT), ISTAT(5) and ISTAT(6); setting ICTRL(4)=0.
3. Run the Interrupt Service Routine, setting the Interrupt Acknowledge bit ICTRL(3) =1 to clear the Interrupt Status Register.
4. Setting ICTRL(4) = 1, waiting for next interrupt.

The following table shows how CTRL and ICTRL control the ISTAT and interrupts.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| When Set the Buffer Stop bit | | | | | |
| CTRL(3) | ICTRL(5) | ICTRL(6) | ISTAT(5) | ISTAT(6) | Interrupt |
| 1 | 1 | x | 1 | 0 | Circular Buffer Done |
| When Trip on an FSD | | | | | |
| CTRL(2) | ICTRL(5) | ICTRL(6) | ISTAT(5) | ISTAT(6) | Interrupts |
| 0 | x | 1 | 0 | 1 | FSD |
| 1 | 0 | 1 | 0 | 1 | FSD |
| 1 | 1 | 0 | 1 | 0 | Circular Buffer Done |
| 1 | 1 | 1 | 1 | 1 | FSD, Circular Buffer |

**Input Selection**

Jumpers J6, J8, J10, J12, J14, J16, J18, J20, J22, J24, J26, J28 are used to select either current inputs or voltage inputs. When jumper is on, it is current input, otherwise voltage input. The first four channels can be selected to input from 4 LEMO connectors. Jumpers J29, J30, J31, J32 are installed for this purpose.

**Input Mode Selection**

Each channel can either work on differential mode or single-end mode. When Jumpers J5, J7, J9, J11, J13, J15, J17, J19, J21, J23, J25, J27 are on, it is single-end mode.

## Chapter 4: Programming

The ADC FSD VME board is controlled by writing and reading 16-bit registers at the FPGA. The following table lists all these registers.

**ADC FSD VME Board Registers**

|  |  |  |  |
| --- | --- | --- | --- |
| Register Name | Address | Read/Write | Function |
| FRMVER | 0x00 | R | Firmware version, 0x5120 |
| CTRL | 0x02 | R/W | Control Register |
| STAT | 0x04 | R | Status Register |
| INST | 0x06 | R | FSD Instant Register |
| LATCH | 0x08 | R | FSD Latch Register |
| MASK | 0x0A | R/W | FSD Mask Register |
| TEST | 0x0C | R/W | FSD Test Register |
| ORDR00 | 0x0E | R | FSD Latch Order 0 |
| ORDR01 | 0x10 | R | FSD Latch Order 1 |
| ORDR02 | 0x12 | R | FSD Latch Order 2 |
| ORDR03 | 0x14 | R | FSD Latch Order 3 |
| ORDR04 | 0x16 | R | FSD Latch Order 4 |
| ORDR05 | 0x18 | R | FSD Latch Order 5 |
| ORDR06 | 0x1A | R | FSD Latch Order 6 |
| ORDR07 | 0x1C | R | FSD Latch Order 7 |
| ORDR08 | 0x1E | R | FSD Latch Order 8 |
| ORDR09 | 0x20 | R | FSD Latch Order 9 |
| ORDR10 | 0x22 | R | FSD Latch Order 10 |
| ORDR11 | 0x24 | R | FSD Latch Order 11 |
| ORDR12 | 0x26 | R | FSD Latch Order 12 |
| NOMASK | 0x28 | R | No FSD Mask Register |
| INVWIN | 0x2A | R/W | Invert Window Compare |
| IVECT | 0x2C | R/W | Interrupt Vector Register |
| ICTRL | 0x2E | R/W | Interrupt Control Register |
| ISTAT | 0x30 | R | Interrupt Status Register |
| ADDRPT | 0x32 | R | SDRAM Address Pointer 16 bit Register |
| BUFDLY | 0x34 | R/W | Buffer Delay Register |
| TSTSET | 0x36 | R/W | DAC Test Setpoint Register |
| PULSOF | 0x38 | R/W | DAC Test Pulse Off Register |
| PULSON | 0x3A | R/W | DAC Test Pulse On Register |
| PULSCN | 0x3C | R/W | 32 bit Test Pulse Count Register |
| RDBK01 | 0x40 | R/O | Channel 1 Readback |
| RDBK02 | 0x42 | R/O | Channel 2 Readback |
| RDBK03 | 0x44 | R/O | Channel 3 Readback |
| RDBK04 | 0x46 | R/O | Channel 4 Readback |
| RDBK05 | 0x48 | R/O | Channel 5 Readback |
| RDBK06 | 0x4A | R/O | Channel 6 Readback |
| RDBK07 | 0x4C | R/O | Channel 7 Readback |
| RDBK08 | 0x4E | R/O | Channel 8 Readback |
| RDBK09 | 0x50 | R/O | Channel 9 Readback |
| RDBK10 | 0x52 | R/O | Channel 10 Readback |
| RDBK11 | 0x54 | R/O | Channel 11 Readback |
| RDBK12 | 0x56 | R/O | Channel 12 Readback |
| LOLM01 | 0x58 | R/W | Channel 1 Low Limit |
| LOLM02 | 0x5A | R/W | Channel 2 Low Limit |
| LOLM03 | 0x5C | R/W | Channel 3 Low Limit |
| LOLM04 | 0x5E | R/W | Channel 4 Low Limit |
| LOLM05 | 0x60 | R/W | Channel 5 Low Limit |
| LOLM06 | 0x62 | R/W | Channel 6 Low Limit |
| LOLM07 | 0x64 | R/W | Channel 4 Low Limit |
| LOLM08 | 0x66 | R/W | Channel 8 Low Limit |
| LOLM09 | 0x68 | R/W | Channel 9 Low Limit |
| LOLM010 | 0x6A | R/W | Channel 10 Low Limit |
| LOLM11 | 0x6C | R/W | Channel 11 Low Limit |
| LOLM12 | 0x6E | R/W | Channel 12 Low Limit |
| HILM01 | 0x70 | R/W | Channel 1 High Limit |
| HILM02 | 0x72 | R/W | Channel 2 High Limit |
| HILM03 | 0x74 | R/W | Channel 3 High Limit |
| HILM04 | 0x76 | R/W | Channel 4 High Limit |
| HILM05 | 0x78 | R/W | Channel 5 High Limit |
| HILM06 | 0x7A | R/W | Channel 6 High Limit |
| HILM07 | 0x7C | R/W | Channel 7 High Limit |
| HILM08 | 0x7E | R/W | Channel 8 High Limit |
| HILM09 | 0x80 | R/W | Channel 9 High Limit |
| HILM10 | 0x82 | R/W | Channel 10 High Limit |
| HILM11 | 0x84 | R/W | Channel 11 High Limit |
| HILM12 | 0x86 | R/W | Channel 12 High Limit |
| INLM01 | 0x88 | R/W | Channel 1 Integrating Setting Limit |
| INLM02 | 0x8C | R/W | Channel 2 Integrating Setting Limit |
| INLM03 | 0x90 | R/W | Channel 3 Integrating Setting Limit |
| INLM04 | 0x94 | R/W | Channel 4 Integrating Setting Limit |
| INLM05 | 0x98 | R/W | Channel 5 Integrating Setting Limit |
| INLM06 | 0x9C | R/W | Channel 6 Integrating Setting Limit |
| INLM07 | 0xA0 | R/W | Channel 7 Integrating Setting Limit |
| INLM08 | 0xA4 | R/W | Channel 8 Integrating Setting Limit |
| INLM09 | 0xA8 | R/W | Channel 9 Integrating Setting Limit |
| INLM10 | 0xAC | R/W | Channel 10 Integrating Setting Limit |
| INLM11 | 0xB0 | R/W | Channel 11 Integrating Setting Limit |
| INLM12 | 0xB4 | R/W | Channel 12 Integrating Setting Limit |

**Register Descriptions**

1. Board Identification or Firmware version (FRMVER), Address 0x00

Value “0x5120”

1. Control Register (CTRL), Address 0x02

Bit 0 – FSD clear, Rising edge trig

Bit 1 – Board Reset

Bit 2 – Enable Circular Buffer Stop on FSD (1=Stop taking data after FSD, 0=Ignore FSD)

Bit 3 – Stop Circular Buffer, for read access (1= stop taking data, 0 = take data)

Bit 4 –15 – Unused

1. Status Register (STAT), Address 0x04

Bit 0 – Heartbeat

Bit 1 - FSD Out Latch

Bit 2 – FSD Out Instant

Bit 3 – Circular Buffer Done (1=stopped taking data, 0 = taking data)

Bit 4-7 – Unused

Bit 8-15 – Base Address Switch Bit 0-7

1. FSD Instant Register (INST), Address 0x06

Bit 0 – Watchdog Timer

Bit 1 – ADC Input 1

Bit 2 – ADC Input 2

Bit 3 – ADC Input 3

Bit 4 – ADC Input 4

Bit 5 – ADC Input 5

Bit 6 – ADC Input 6

Bit 7 – ADC Input 7

Bit 8 – ADC Input 8

Bit 9 – ADC Input 9

Bit 10 – ADC Input 10

Bit 11 – ADC Input 11

Bit 12 – ADC Input 12

1. FSD Latch Register (LATCH), Address 0x08

Bit 0 – Watchdog Timer

Bit 1 – ADC Input 1

Bit 2 – ADC Input 2

Bit 3 – ADC Input 3

Bit 4 – ADC Input 4

Bit 5 – ADC Input 5

Bit 6 – ADC Input 6

Bit 7 – ADC Input 7

Bit 8 – ADC Input 8

Bit 9 – ADC Input 9

Bit 10 – ADC Input 10

Bit 11 – ADC Input 11

Bit 12 – ADC Input 12

1. FSD Mask Register (MASK), Address 0x0A

Bit 0 – Watchdog Timer

Bit 1 – ADC Input 1

Bit 2 – ADC Input 2

Bit 3 – ADC Input 3

Bit 4 – ADC Input 4

Bit 5 – ADC Input 5

Bit 6 – ADC Input 6

Bit 7 – ADC Input 7

Bit 8 – ADC Input 8

Bit 9 – ADC Input 9

Bit 10 – ADC Input 10

Bit 11 – ADC Input 11

Bit 12 – ADC Input 12

1. FSD TEST Register (TEST), Address 0x0C

Bit 0 – Watchdog Timer

Bit 1 – Test Input 1

Bit 2 – Test Input 2

Bit 3 – Test Input 3

Bit 4 – Test Input 4

Bit 5 – Test Input 5

Bit 6 – Test Input 6

Bit 7 – Test Input 7

Bit 8 – Test Input 8

Bit 9 – Test Input 9

Bit 10 – Test Input 10

Bit 11 – Test Input 11

Bit 12 – Test Input 12

Bit 13 – Pulse Test mode enable; 0 for constant-on test (TESTSET), 1 for single pulse test (PULS\_ON/OFF)

Bit 14 – Pulse Go (Rising edge trigger)

1. Watchdog Timer Order Register (ORDR00), Address 0x0E
2. FSD Latch Order Register 1 (ORDR01), Address 0x10
3. FSD Latch Order Register 2 (ORDR02), Address 0x12
4. FSD Latch Order Register 3 (ORDR03), Address 0x14
5. FSD Latch Order Register 4 (ORDR04), Address 0x16
6. FSD Latch Order Register 5 (ORDR05), Address 0x18
7. FSD Latch Order Register 6 (ORDR06), Address 0x1A
8. FSD Latch Order Register 7 (ORDR07), Address 0x1C
9. FSD Latch Order Register 8 (ORDR08), Address 0x1E
10. FSD Latch Order Register 9 (ORDR09), Address 0x20
11. FSD Latch Order Register 10 (ORDR10), Address 0x22
12. FSD Latch Order Register 11 (ORDR11), Address 0x24
13. FSD Latch Order Register 12 (ORDR12), Address 0x26
14. No FSD Mask Register (NOMASK), Address 0x28, 1- No Mask, 0- Mask allowed

Bit 0 – Watchdog Timer ( always No Mask)

Bit 1 – ADC Input 1

Bit 2 – ADC Input 2

Bit 3 – ADC Input 3

Bit 4 – ADC Input 1

Bit 5 – ADC Input 2

Bit 6 – ADC Input 3

Bit 7 – ADC Input 1

Bit 8 – ADC Input 2

Bit 9 – ADC Input 3

Bit 10 – ADC Input 10

Bit 11 – ADC Input 11

Bit 12 – ADC Input 12

1. Invert Window Compare(INVWIN), address 0x2A, (0=Normal Window, 1= Inverter Window compare)

Bit 0 – ADC Input 1

Bit 1 – ADC Input 2

Bit 2 – ADC Input 3

Bit 3 – ADC Input 4

Bit 4 – ADC Input 5

Bit 5 – ADC Input 6

Bit 6 – ADC Input 7

Bit 7 – ADC Input 8

Bit 8 – ADC Input 9

Bit 9 – ADC Input 10

Bit 10 – ADC Input 11

Bit 11 – ADC Input 12

1. Interrupt Vector Register (ivec), address 0x2C (8-bits)
2. Interrupt Control Register (ictrl), address 0x2E

Bit 0-2, Interrupt level 1-7 (Same with the Jumper setting)

Bit 3 – Interrupt Acknowledge (rising edge releases the IRQ and clear Interrupt Status Register)

Bit 4 – Global Interrupt Enable

Bit 5 – Circular Buffer Done

Bit 6 - FSD

1. Interrupt Status Register (ISTAT), address 0x30

Bit 5 – Circular Buffer Done

Bit 6 - FSD

1. Address Pointer for SDRAM (ADDRPT), Address 0x32

Read back of the SDRAM circular buffer ending address (location of the newest piece of data, 0x0000 – 0xFFFF, even number)

1. Buffer delay Register (BUFDLY), Address 0x34

Control the number of data that stored on the ring buffer after the FSD trigger (10usec per count). 0xFFFF

1. DAC Test Setpoint Register(TSTSET), Address 0x036
2. DAC Setpoint Pulse Off Register (PULSOF), Address 0x38
3. DAC Setpoint Pulse On Register (PULSON), Address 0x3A

16-bit data, -10V - +10V, 0x0000-> -10V, 0x8000-> 0V, 0xFFFF-> +10V (20 Volts/65536 ).

1. 32 Bit Pulse Count Register (pulscn), Address 0x3C

10 us per count

1. Channel 1 Data (rdbk01), Address 0x40
2. Channel 2 Data (rdbk02), Address 0x42
3. Channel 3 Data (rdbk03), Address 0x44
4. Channel 4 Data (rdbk04), Address 0x46
5. Channel 5 Data (rdbk05), Address 0x48
6. Channel 6 Data (rdbk06), Address 0x4A
7. Channel 7 Data (rdbk07), Address 0x4C
8. Channel 8 Data (rdbk08), Address 0x4E
9. Channel 9 Data (rdbk09), Address 0x50
10. Channel 10 Data (rdbk10), Address 0x52
11. Channel 11 Data (rdbk11), Address 0x54
12. Channel 12 Data (rdbk12), Address 0x56

100Ksps for each ADC channels, signed 16-bit, -10 - +10V (20Volts/65536)

-10V – 0V -> 0x8000-0xFFFF, 0V – 10V -> 0x0000 – 0x7FFFF

1. Channel 1 Low Limit Setting (lolm01), Address 0x58
2. Channel 2 Low Limit Setting (lolm02), Address 0x5A
3. Channel 3 Low Limit Setting (lolm03), Address 0x5C
4. Channel 4 Low Limit Setting (lolm04), Address 0x5E
5. Channel 5 Low Limit Setting (lolm05), Address 0x60
6. Channel 6 Low Limit Setting (lolm06), Address 0x62
7. Channel 7 Low Limit Setting (lolm07), Address 0x64
8. Channel 8 Low Limit Setting (lolm08), Address 0x66
9. Channel 9 Low Limit Setting (lolm09), Address 0x68
10. Channel 10 Low Limit Setting (lolm10), Address 0x6A
11. Channel 11 Low Limit Setting (lolm11), Address 0x6C
12. Channel 12 Low Limit Setting (lolm12), Address 0x6E
13. Channel 1 High Limit Setting (hilm01), Address 0x70
14. Channel 2 High Limit Setting (hilm02), Address 0x72
15. Channel 3 High Limit Setting (hilm03), Address 0x74
16. Channel 4 High Limit Setting (hilm04), Address 0x76
17. Channel 5 High Limit Setting (hilm05), Address 0x78
18. Channel 6 High Limit Setting (hilm06), Address 0x7A
19. Channel 7 High Limit Setting (hilm07), Address 0x7C
20. Channel 8 High Limit Setting (hilm08), Address 0x7E
21. Channel 9 High Limit Setting (hilm09), Address 0x80
22. Channel 10 High Limit Setting (hilm10), Address 0x82
23. Channel 11 High Limit Setting (hilm11), Address 0x84
24. Channel 12 High Limit Setting (hilm12), Address 0x86

Signed 16-bit, -10 - +10V (20Volts/65536)

1. Channel 1 Integrating Setting Limit (inlM01), Address 0x88
2. Channel 2 Integrating Setting Limit (inlM02), Address 0x8C
3. Channel 3 Integrating Setting Limit (inlM03), Address 0x90
4. Channel 4 Integrating Setting Limit (inlM04), Address 0x94
5. Channel 5 Integrating Setting Limit (inlM05), Address 0x98
6. Channel 6 Integrating Setting Limit (inlM06), Address 0x9C
7. Channel 7 Integrating Setting Limit (inlM07), Address 0xA0
8. Channel 8 Integrating Setting Limit (inlM08), Address 0xA4
9. Channel 9 Integrating Setting Limit (inlM09), Address 0xA8
10. Channel 10 Integrating Setting Limit (inlM10), Address 0xAC
11. Channel 11 Integrating Setting Limit (inlM11), Address 0xB0
12. Channel 12 Integrating Setting Limit (inlM12), Address 0xB4

Unsigned 32-bit, Volt \* Seconds (ASLO = 0.00001 sec \* 20V/65536)

**SDRAM Memory**

The SDRAM write rate is same as the ADC sample rate, 100ksps and signed 16-bit (20V/65536cnt). The ADC FSD Board has 640K bytes standard address space, 64K bytes for each channel (32K words).

SDRAM memory allocation for each channel:

0x00000 – 0x0FFFF Channel 1

0x10000 – 0x1FFFF Channel 2

0x20000 – 0x2FFFF Channel 3

0x30000 – 0x3FFFF Channel 4

0x40000 – 0x4FFFF Channel 5

0x50000 - 0x5FFFF Channel 6

0x60000 – 0x6FFFF Channel 7

0x70000 – 0x7FFFF Channel 8

0x80000 – 0x8FFFF Channel 9

0x90000 – 0x9FFFF Channel 10

0xA0000 – 0xAFFFF Channel 11

0xB0000 – 0xBFFFF Channel 12

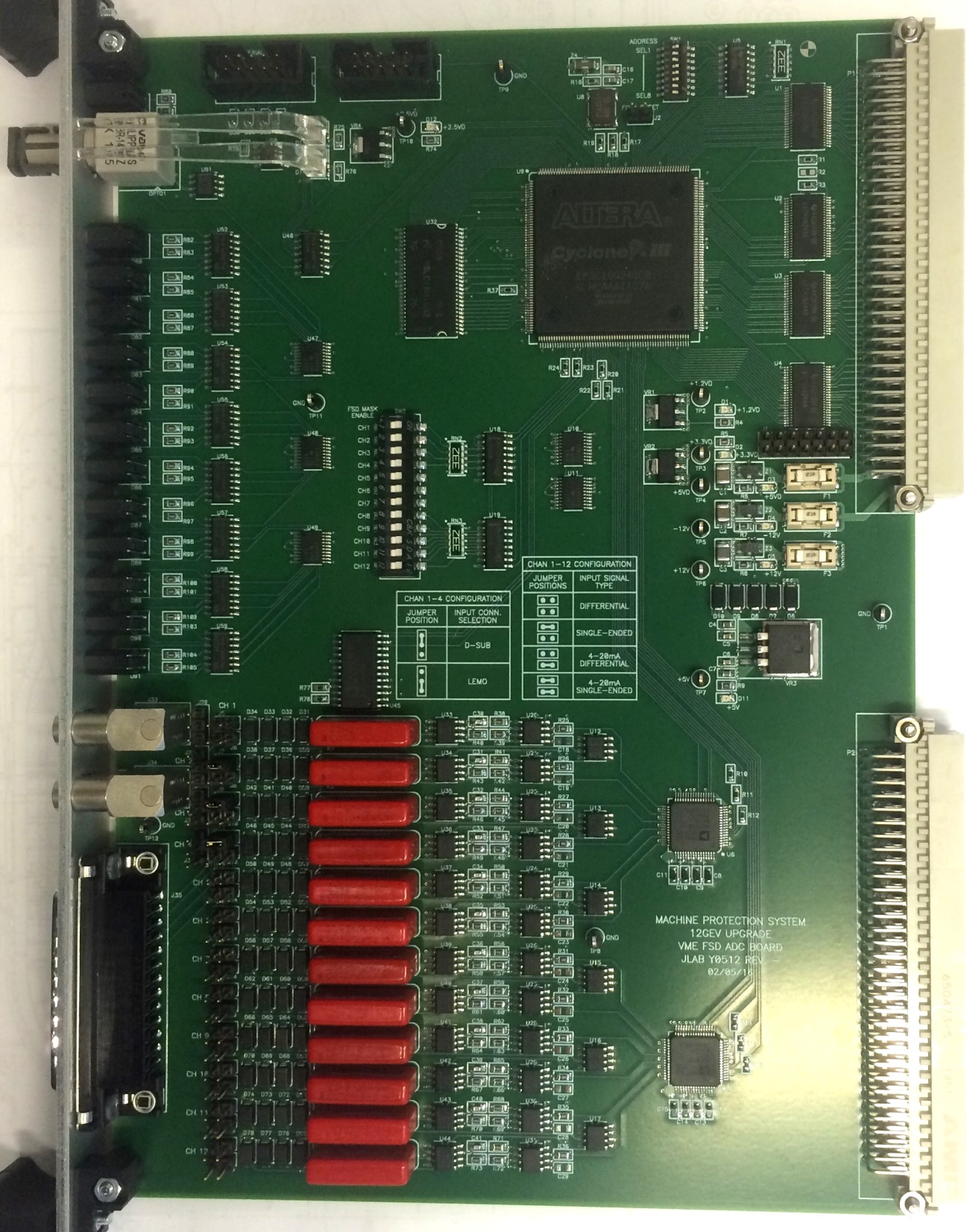
# Front Panel & Connectors

The front panel has one Power LED, one Heartbeat LED, one fiber output connector, one light pipe, 12 dual LEDs for 12 ADC channels, 4 LEMO connectors, and one D-25 male connector. The first 4 ADC channels can input from either D-25 connector or 4 LEMO connectors, and they are jumper selectable. The inputs of the D-25 connector can be selected as differential mode or single-end mode. The pin layout of the D-25 connector is shown as the following.

D-25 Male Connector

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin #** | **Channel #** | **Input** | |
|  |  | Diff. Mode | Single-End Mode |
| 1 | 1 | Positive + | Positive + |
| 2 | 2 | Positive + | Positive + |
| 3 | 3 | Positive + | Positive + |
| 4 | 4 | Positive + | Positive + |
| 5 | 5 | Positive + | Positive + |
| 6 | 6 | Positive + | Positive + |
| 7 | 7 | Positive + | Positive + |
| 8 | 8 | Positive + | Positive + |
| 9 | 9 | Positive + | Positive + |
| 10 | 10 | Positive + | Positive + |
| 11 | 11 | Positive + | Positive + |
| 12 | 12 | Positive + | Positive + |
| 13 |  | GND | GND |
| 14 | 1 | Negative - | GND |
| 15 | 2 | Negative - | GND |
| 16 | 3 | Negative - | GND |
| 17 | 4 | Negative - | GND |
| 18 | 5 | Negative - | GND |
| 19 | 6 | Negative - | GND |
| 20 | 7 | Negative - | GND |
| 21 | 8 | Negative - | GND |
| 22 | 9 | Negative - | GND |
| 23 | 10 | Negative - | GND |
| 24 | 11 | Negative - | GND |
| 25 | 12 | Negative - | GND |

**Pictures of the ADC FSD Board and the Front Panel**



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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| HRT   |  | | --- | | { "", "FRMVER", 0x000, U16, RO, CXX, " 0 Firmware Version" }, | | { "", "CTRL", 0x002, U16B, RW, CXX, " 1 Control Bits " }, | | { "", "STAT", 0x004, U16B, RO, CXX, " 2 Status Bits" }, | | { "", "INST", 0x006, U16B, RO, CXX, " 3 FSD Instant " }, | | { "", "LATCH", 0x008, U16B, RO, CXX, " 4 FSD Latch" }, | | { "", "MASK", 0x00A, U16B, RW, CXX, " 5 FSD Mask" }, | | { "", "TEST", 0x00C, U16B, RW, CXX, " 6 FSD Test" }, | | { "", "ORDR00", 0x00E, U16, RO, CXX, " 7 FSD Latch Order 0" }, | | { "", "ORDR01", 0x010, U16, RO, CXX, " 8 FSD Latch Order 1" }, | | { "", "ORDR02", 0x012, U16, RO, CXX, " 9 FSD Latch Order 2" }, | | { "", "ORDR03", 0x014, U16, RO, CXX, " 10 FSD Latch Order 3" }, | | { "", "ORDR04", 0x016, U16, RO, CXX, " 11 FSD Latch Order 4" }, | | { "", "ORDR05", 0x018, U16, RO, CXX, " 12 FSD Latch Order 5" }, | | { "", "ORDR06", 0x01A, U16, RO, CXX, " 13 FSD Latch Order 6" }, | | { "", "ORDR07", 0x01C, U16, RO, CXX, " 14 FSD Latch Order 7" }, | | { "", "ORDR08", 0x01E, U16, RO, CXX, " 15 FSD Latch Order 8" }, | | { "", "ORDR09", 0x020, U16, RO, CXX, " 16 FSD Latch Order 9" }, | | { "", "ORDR10", 0x022, U16, RO, CXX, " 17 FSD Latch Order 10" }, | | { "", "ORDR11", 0x024, U16, RO, CXX, " 18 FSD Latch Order 11" }, | | { "", "ORDR12", 0x026, U16, RO, CXX, " 19 FSD Latch Order 12" }, | | { "", "NOMASK", 0x028, U16B, RO, CXX, " 20 No FSD Mask " }, | | { "", "INVWIN", 0x02A, U16B, RW, CXX, " 21 Invert Window Compare" }, | | { "", "IVECT", 0x02C, U16, RW, CXX, " 22 Interrupt Vector" }, | | { "", "ICTRL", 0x02E, U16B, RW, CXX, " 23 Interrupt Control" }, | | { "", "ISTAT", 0x030, U16B, RO, CXX, " 24 Interrupt Status" }, | | { "", "ADDRPT", 0x032, U16, RO, CXX, " 25 SDRAM Address Pointer" }, | | { "", "BUFDLY", 0x034, U16, RW, CXX, " 26 Buffer Delay" }, | | { "", "TSTSET", 0x036, S16, RW, CXX, " 27 DAC Test Setpoint" }, | | { "", "PULSOF", 0x038, S16, RW, CXX, " 28 Test Pulse Off " }, | | { "", "PULSON", 0x03A, S16, RW, CXX, " 29 Test Pulse On" }, | | { "", "PULSCN", 0x03C, U32L, RW, CXX, " 30 Test Pulse Count" }, | | { "", "RDBK01", 0x040, S16, RO, CSO, " 31 Channel 1 Readback" }, | | { "", "RDBK02", 0x042, S16, RO, CSO, " 32 Channel 2 Readback" }, | | { "", "RDBK03", 0x044, S16, RO, CSO, " 33 Channel 3 Readback" }, | | { "", "RDBK04", 0x046, S16, RO, CSO, " 34 Channel 4 Readback" }, | | { "", "RDBK05", 0x048, S16, RO, CSO, " 35 Channel 5 Readback" }, | | { "", "RDBK06", 0x04A, S16, RO, CSO, " 36 Channel 6 Readback" }, | | { "", "RDBK07", 0x04C, S16, RO, CSO, " 37 Channel 7 Readback" }, | | { "", "RDBK08", 0x04E, S16, RO, CSO, " 38 Channel 8 Readback" }, | | { "", "RDBK09", 0x050, S16, RO, CSO, " 39 Channel 9 Readback" }, | | { "", "RDBK10", 0x052, S16, RO, CSO, " 40 Channel 10 Readback" }, | | { "", "RDBK11", 0x054, S16, RO, CSO, " 41 Channel 11 Readback" }, | | { "", "RDBK12", 0x056, S16, RO, CSO, " 42 Channel 12 Readback" }, | | { "", "LOLM01", 0x058, S16, RW, CSO, " 43 Channel 1 Low Limit Setting" }, | | { "", "LOLM02", 0x05A, S16, RW, CSO, " 44 Channel 2 Low Limit Setting" }, | | { "", "LOLM03", 0x05C, S16, RW, CSO, " 45 Channel 3 Low Limit Setting" }, | | { "", "LOLM04", 0x05E, S16, RW, CSO, " 46 Channel 4 Low Limit Setting" }, | | { "", "LOLM05", 0x060, S16, RW, CSO, " 47 Channel 5 Low Limit Setting" }, | | { "", "LOLM06", 0x062, S16, RW, CSO, " 48 Channel 6 Low Limit Setting" }, | | { "", "LOLM07", 0x064, S16, RW, CSO, " 49 Channel 7 Low Limit Setting" }, | | { "", "LOLM08", 0x066, S16, RW, CSO, " 50 Channel 8 Low Limit Setting" }, | | { "", "LOLM09", 0x068, S16, RW, CSO, " 51 Channel 9 Low Limit Setting" }, | | { "", "LOLM10", 0x06A, S16, RW, CSO, " 52 Channel 10 Low Limit Setting" }, | | { "", "LOLM11", 0x06C, S16, RW, CSO, " 53 Channel 11 Low Limit Setting" }, | | { "", "LOLM12", 0x06E, S16, RW, CSO, " 54 Channel 12 Low Limit Setting" }, | | { "", "HILM01", 0x070, S16, RW, CSO, " 55 Channel 1 High Limit Setting" }, | | { "", "HILM02", 0x072, S16, RW, CSO, " 56 Channel 2 High Limit Setting" }, | | { "", "HILM03", 0x074, S16, RW, CSO, " 57 Channel 3 High Limit Setting" }, | | { "", "HILM04", 0x076, S16, RW, CSO, " 58 Channel 4 High Limit Setting" }, | | { "", "HILM05", 0x078, S16, RW, CSO, " 59 Channel 5 High Limit Setting" }, | | { "", "HILM06", 0x07A, S16, RW, CSO, " 60 Channel 6 High Limit Setting" }, | | { "", "HILM07", 0x07C, S16, RW, CSO, " 61 Channel 7 High Limit Setting" }, | | { "", "HILM08", 0x07E, S16, RW, CSO, " 62 Channel 8 High Limit Setting" }, | | { "", "HILM09", 0x080, S16, RW, CSO, " 63 Channel 9 High Limit Setting" }, | | { "", "HILM10", 0x082, S16, RW, CSO, " 64 Channel 10 High Limit Setting" }, | | { "", "HILM11", 0x084, S16, RW, CSO, " 65 Channel 11 High Limit Setting" }, | | { "", "HILM12", 0x086, S16, RW, CSO, " 66 Channel 12 High Limit Setting" }, | | { "", "INLM01", 0x088, U32L, RW, CSO, " 67 Channel 1 Integrate Setting Limit" }, | | { "", "INLM02", 0x08C, U32L, RW, CSO, " 68 Channel 2 Integrate Setting Limit" }, | | { "", "INLM03", 0x090, U32L, RW, CSO, " 69 Channel 3 Integrate Setting Limit" }, | | { "", "INLM04", 0x094, U32L, RW, CSO, " 70 Channel 4 Integrate Setting Limit" }, | | { "", "INLM05", 0x098, U32L, RW, CSO, " 71 Channel 5 Integrate Setting Limit" }, | | { "", "INLM06", 0x09C, U32L, RW, CSO, " 72 Channel 6 Integrate Setting Limit" }, | | { "", "INLM07", 0x0A0, U32L, RW, CSO, " 73 Channel 7 Integrate Setting Limit" }, | | { "", "INLM08", 0x0A4, U32L, RW, CSO, " 74 Channel 8 Integrate Setting Limit" }, | | { "", "INLM09", 0x0A8, U32L, RW, CSO, " 75 Channel 9 Integrate Setting Limit" }, | | { "", "INLM10", 0x0AC, U32L, RW, CSO, " 76 Channel 10 Integrate Setting Limit" }, | | { "", "INLM11", 0x0B0, U32L, RW, CSO, " 77 Channel 11 Integrate Setting Limit" }, | | { "", "INLM12", 0x0B4, U32L, RW, CSO, " 78 Channel 12 Integrate Setting Limit" }, | |
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