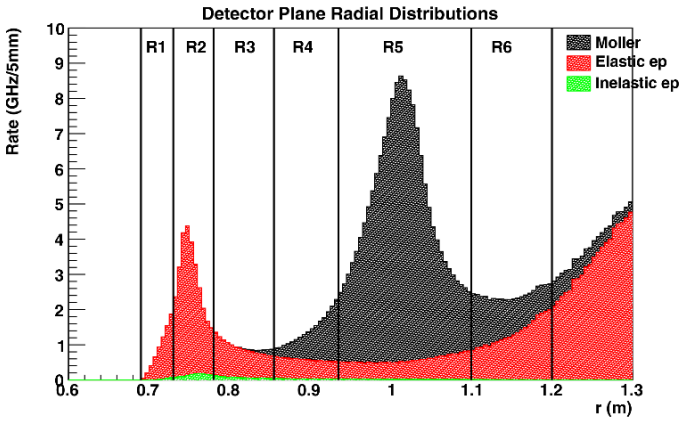
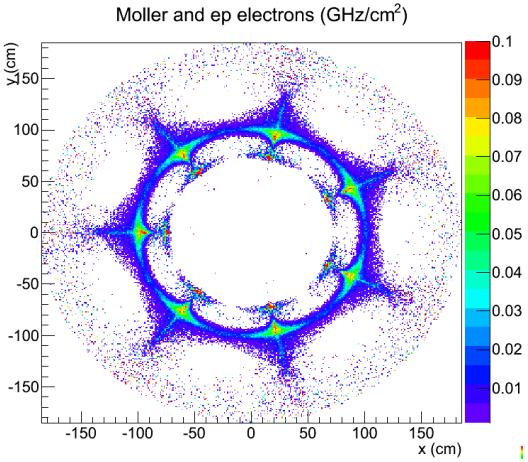
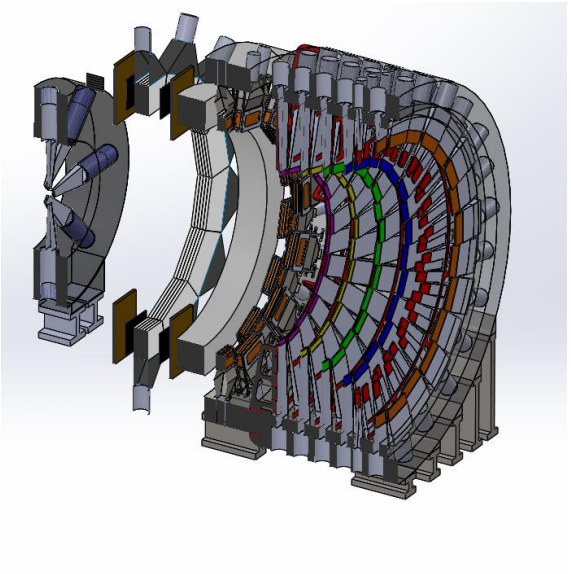
WBS 1.3: Integrating Detector Subsystem

Michael Gericke, University of Manitoba







Integrating Detector Requirements

1. Full coverage of $e + e \rightarrow e + e$ events
2. Radial binning to understand backgrounds: $e + p \rightarrow e + p$ and $e + p \rightarrow e + X$
3. Azimuthal binning to understand e+e signal systematics and get additional handle on $e + p \rightarrow e + p$ and $e + p \rightarrow e + X$ background
4. Low excess noise
5. Good linearity with respect to charge sensitivity
6. Suppression of soft backgrounds (photons and neutrons)
7. Radiation hard to ~50 Mrad
8. No false asymmetries

Purpose of the Integrating Detectors

The integrating detectors are used to measure the flux (Y±) of scattered electrons as a function of initial electron helicity (±)

The measured asymmetry is formed from this flux:

$$A_{expt} = \frac{Y^+ - Y^-}{Y^+ + Y^-} = P_{beam}\left(\left(1 - f_{bkgd}\right)A_{PV} + \sum_{bkgd} A_{bkgd} f_{bkgd}\right) + A_{beam} + A_{inst}$$

P_{beam}	=	**electron polarization**
f_{bhgd}	=	**fraction of flux from background signal**
A_{PV}	=	**physics asymmetries**
A_{bkgd}	=	**background asymmetries**
A_{inst}	=	**instrumental (false) asymmetries**
A_{beam}	=	**beam asymmetries**

High event rate requires signal integration (spatial and timing).

Integrating Detector Dependencies

The measured flux: $$y^{\pm} = \mathcal{L}\sigma\, G^{\pm}\left(1 \pm P_{\text{beam}}\sum_n f_n A_n \pm A_{\text{beam}} \pm A_{\text{inst}}\right) + y^{\pm}_{\text{ped}}$$

Detector gain: $$G^{\pm} \equiv \Gamma^{\pm}_{C}\, Q_{PE}\, g_{PMT}\, g^{\pm}_{\text{amp}}\left(1 + \varepsilon\,\Gamma^{\pm}_{C} + \ldots\right)$$

- Light yield: $\Gamma^{\pm}_{C}$ -maximize, based on geometry and materials (possibly helicity dependent)
- Quantum efficiency: Q_{PE} -UV sensitive, long terms stability, high cathode current
- PMT Gain: g_{PMT} -flexible base design, good linearity at low and high gain
- Preamp gain: $g^{\pm}_{\text{amp}}$ -flexible gain, high bandwidth capable, low noise (possibly helicity dependent)
- Non-linearity: ε -precisely measure PMT non-linearity

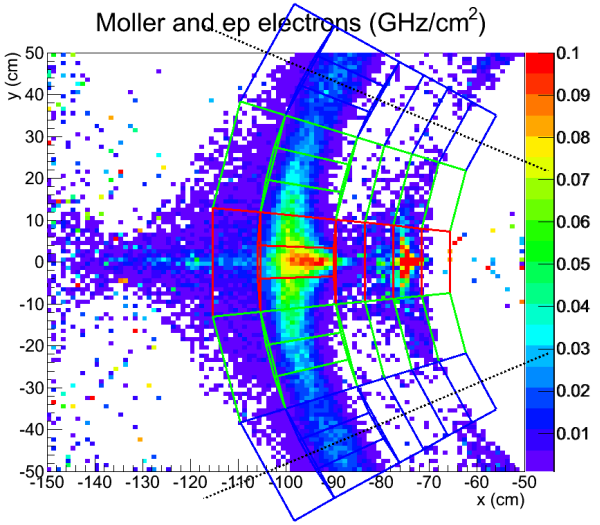
Electronic Pedestal: $y^{\pm}_{\text{ped}}$ -keep small and remove/suppress false asymmetries

ADC Properties: High bandwidth, high sampling rate, linear, low noise

Thin Quartz Detectors

Focal Plane Event Distribution and detector geometry:

$$G^{\pm} \equiv \Gamma_c^{\pm} Q_{PE}\, g_{PMT}\, g_{amp}^{\pm} \left(1 + \varepsilon \Gamma_c^{\pm} + \ldots\right)$$

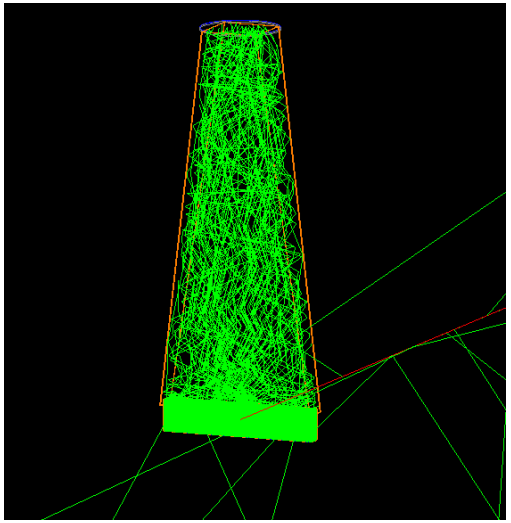


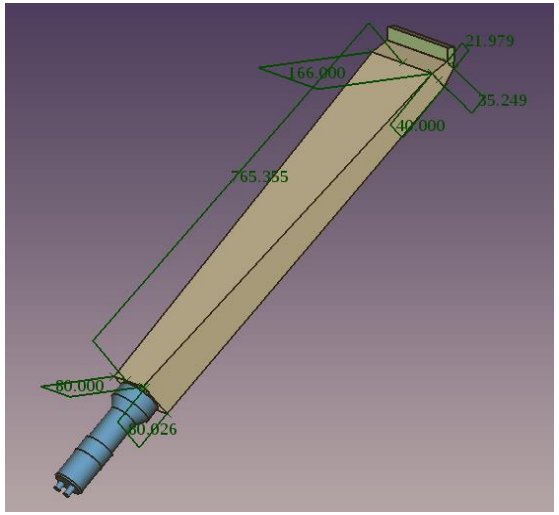
- Current design has for 224 detector tiles
- Rate per tile: ~few MHz to 5 GHz (up to 1 MHz / mm²)
- Acquisition mode: Flux Integrating
  - No event cuts possible
  - Low background by design

- Design based on DIRC with air-core light guide:

  Synthetic Quartz:
  - Radiation hard
  - High threshold for hadrons
  - No scintillation

  Air-Core light guides:
  - Drastically reduce background

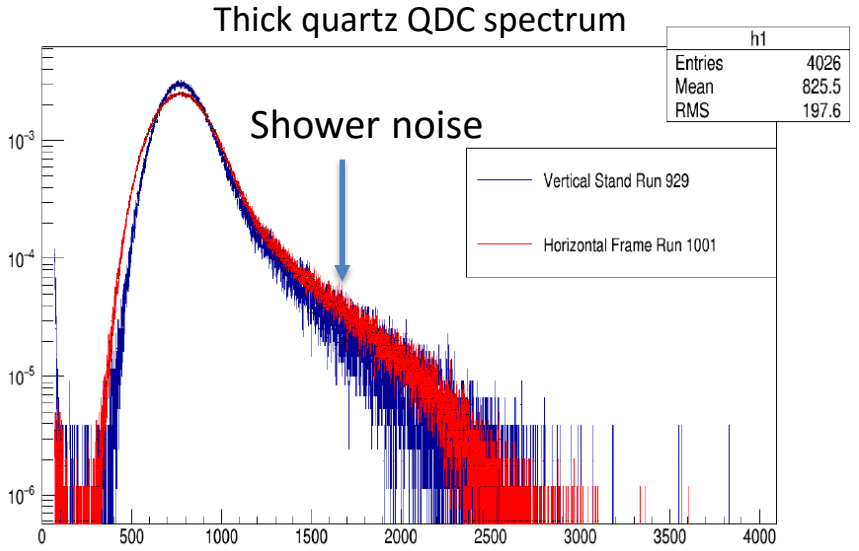




Thin Quartz Detectors

Focal Plane Event Distribution and detector geometry:

$$G^{\pm} \equiv \Gamma_c^{\pm} Q_{PE}\, g_{PMT}\, g_{amp}^{\pm} \left(1 + \varepsilon \Gamma_c^{\pm} + \ldots\right)$$



- Detector rotation and geometry determines light yield and excess noise:
  - High PE mean / low RMS

    ⟹ good resolution: $\frac{\sigma}{\langle n \rangle} \leq 25\%$

  - Shower noise leads to excess noise beyond photoelectron counting statistics:

$$\frac{1}{\sqrt{N_i}} \sqrt{1 + \left(\sigma/\langle n \rangle\right)^2} - \frac{1}{\sqrt{N_i}} \leq 4\%$$

(additionally have PMT gain noise and electronic noise – see later)

Requires optimization of detector thickness

Thin Quartz Detectors

PMT choice:

$$G^{\pm} \equiv \Gamma_C^{\pm} Q_{PE}\, g_{PMT}\, g_{amp}^{\pm} \left(1 + \varepsilon \Gamma_C^{\pm} + \ldots\right)$$

Prototype Tests Done with Electron 9305QKB Candidate

- For current mode PMT operation in the linear thermionic diode region statistics manifest as cathode shot noise:

$$\sigma_{C,shot} = \sqrt{2 Q_{PE}\, i_C}$$

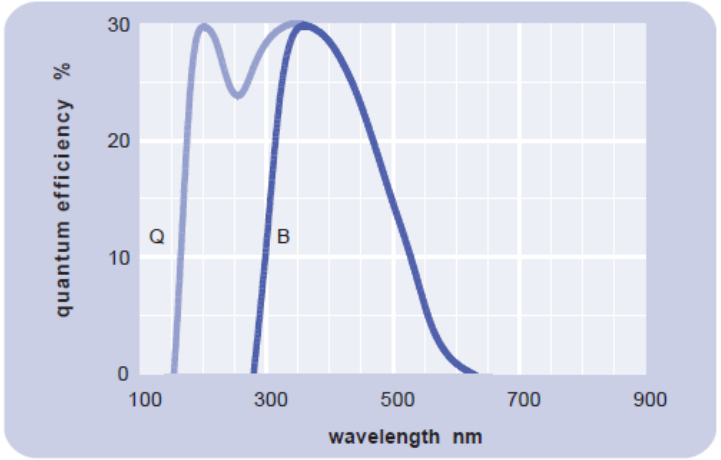
- Only approximately true

$$\frac{1}{\sqrt{N}} \simeq \frac{\sigma_{C,shot}}{i_C}$$

- dynode fluctuations add noise beyond detector resolution

$$\frac{\sigma_n}{\langle n \rangle} \rightarrow \frac{\sigma_n}{\langle n \rangle} \sqrt{\frac{\langle n \rangle}{\langle n \rangle - 1}}$$

- Depends on gain at each dynode: Higher PE numbers are better, but anything above ~15 will do.



maximum ratings:				
anode current	µA			100
cathode current	nA			500
gain	x 10^6			150
sensitivity	A/lm			10000
temperature	°C	-30		60
V (k-a)(1)	V			2500
V (k-d1)	V			650
V (d-d)(2)	V			300
ambient pressure (absolute)	kPa			202

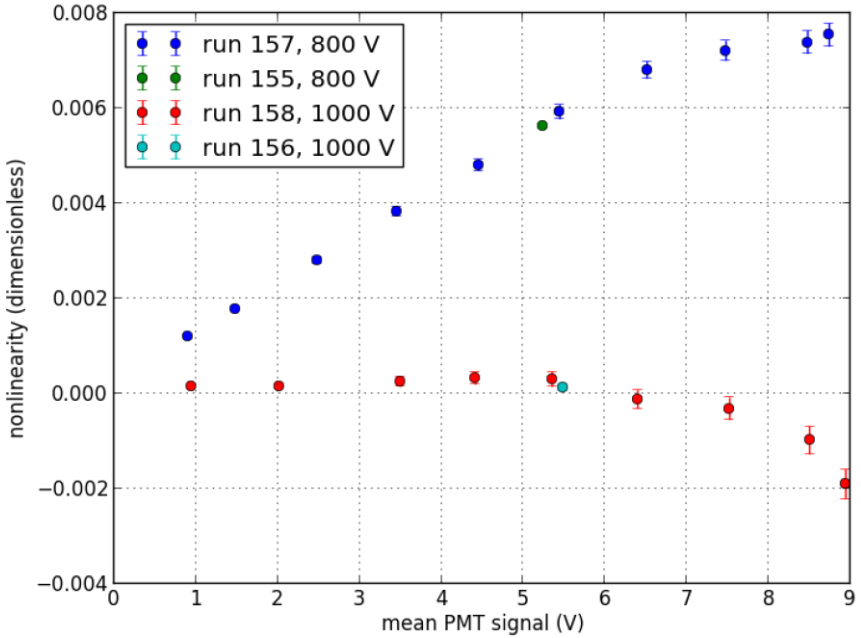
Thin Quartz Detectors

PMT choice:

$$G^{\pm} \equiv \Gamma_c^{\pm} Q_{PE}\, g_{PMT}\, g_{amp}^{\pm} \left(1 + \varepsilon \Gamma_c^{\pm} + \ldots\right)$$

Non-Linearity:

- It will be there, so we need to know it
- Measured during Qweak
- New/more precise tests are underway using actual parity DAQ

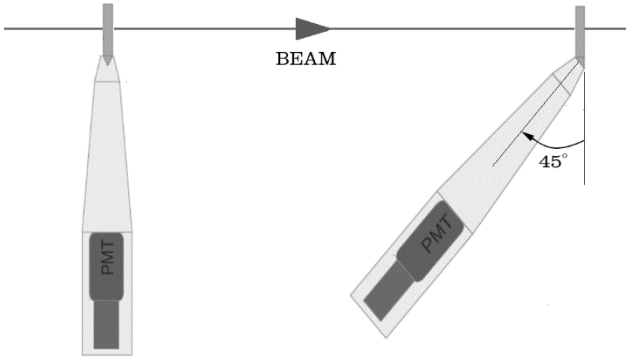


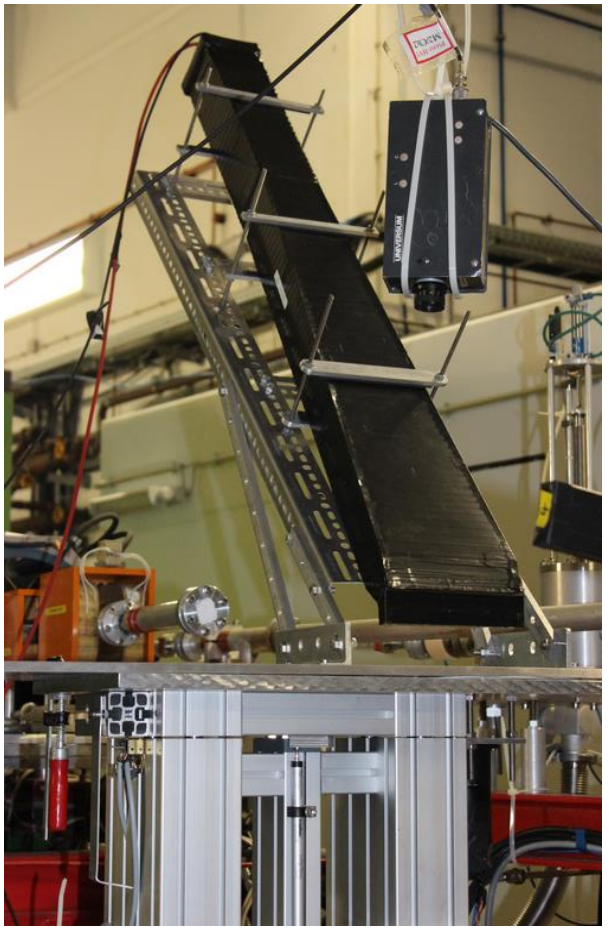
Non-linearity depends both on the signal level and the PMT gain.

The linearity requirements for MOLLER are modest: $\varepsilon \leq 10^{-3}$ or measured to that precision. Higher gains are better, but need to balance with PMT maximum currents.

Thin Quartz Detectors

Multiple beam times at the MAMI facility in Mainz, in 2013,2014,2015, and 2016:





Performed many different tests with various prototype variations and test conditions, including:

- quartz tile geometry
- light guide geometry
- light guide material
- wrapping materials
- hit position/angle dependence
- background from light guides
- photon background studies

Integrating Detector Electronics

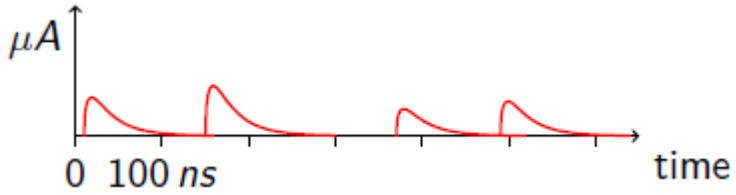
Main test results so far:

Test condition	Results
1.0 cm thick Møller quartz, Miro-Silver guide	Mean yield = 25 pe , RMS = 7.1, 4% excess noise
1.0 cm thick Møller quartz, Mylar guide	Mean yield = 30 pe , RMS = 8.7, 4% excess noise
1.5 cm thick Møller quartz, Miro-Silver guide	Mean yield = 33 pe , RMS = 8.5, 3% excess noise
2.0 cm thick Møller quartz, Mylar guide	Mean yield = 61 pe , RMS = 15.9, 4% excess noise
2.5 cm thick Møller quartz, Miro-Silver guide	Mean yield = 55 pe , RMS = 17.6, 5% excess noise
1.0 cm thick super-elastic quartz, mylar guide	Mean yield = 18 pe , RMS = 6.1, 6% excess noise
1.5 cm thick super-el. quartz, Miro-Silv. guide	Mean yield = 21 pe , RMS = 8.9, 9% excess noise
2.0 cm thick super-el. quartz, mylar guide	Mean yield = 36 pe , RMS = 14, 7% excess noise
Yield tests with diff. quartz wrapping mat.	Millipore incr = fac. 3, mylar incr. = fac. 2 (w.r.t. to no wrapping)
Hit position scans	Only small variations ($\leq$ 8%)
Electron events in light guides	Contribute at the fractional PE level at $\leq$ 0.1% eff.

Integrating Detector Electronics

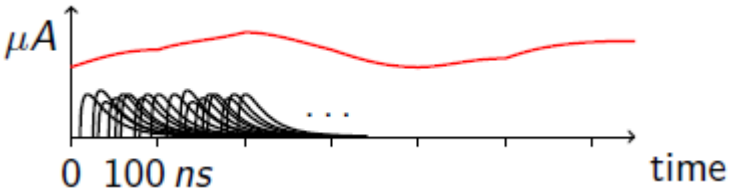
Event mode:

- ❑Each event individually registered
- ❑Event selection / rejection is possible (either PID or discrimination)



Current mode:

- ❑ Very high event rates possible (one every nanosecond)
- ❑ No event selection / background rejection (experiment must be designed to suppress backgrounds and this must be verified with dedicated measurements)

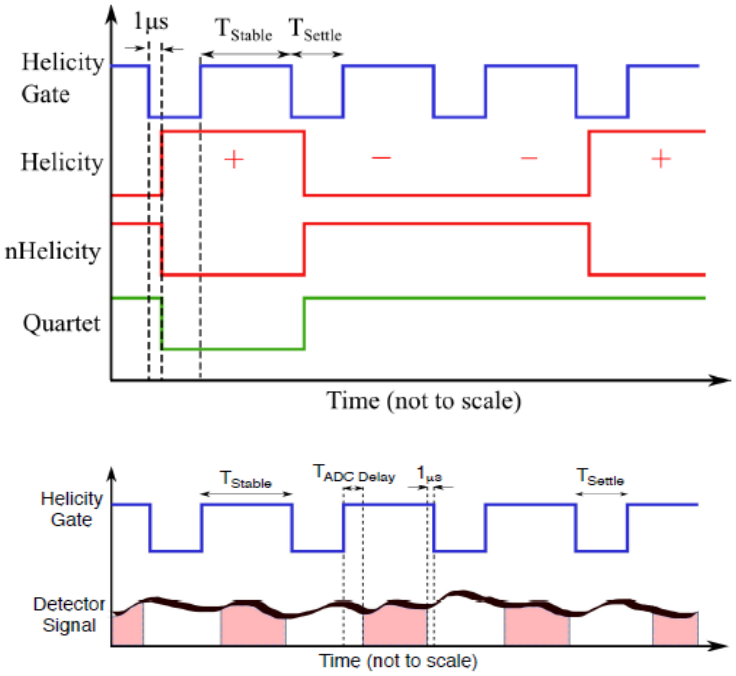


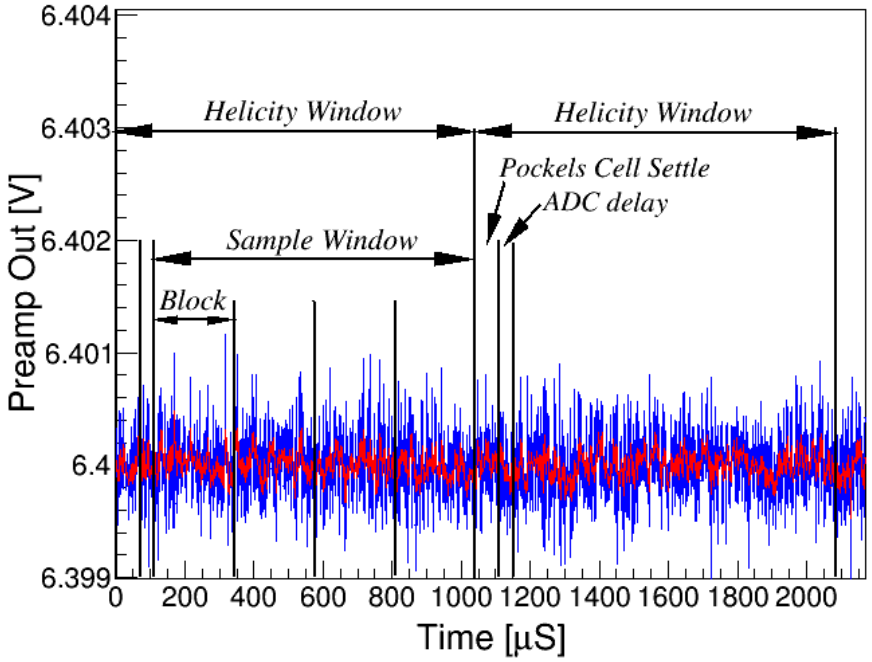
Integrating Detector Electronics

Electronics choices:

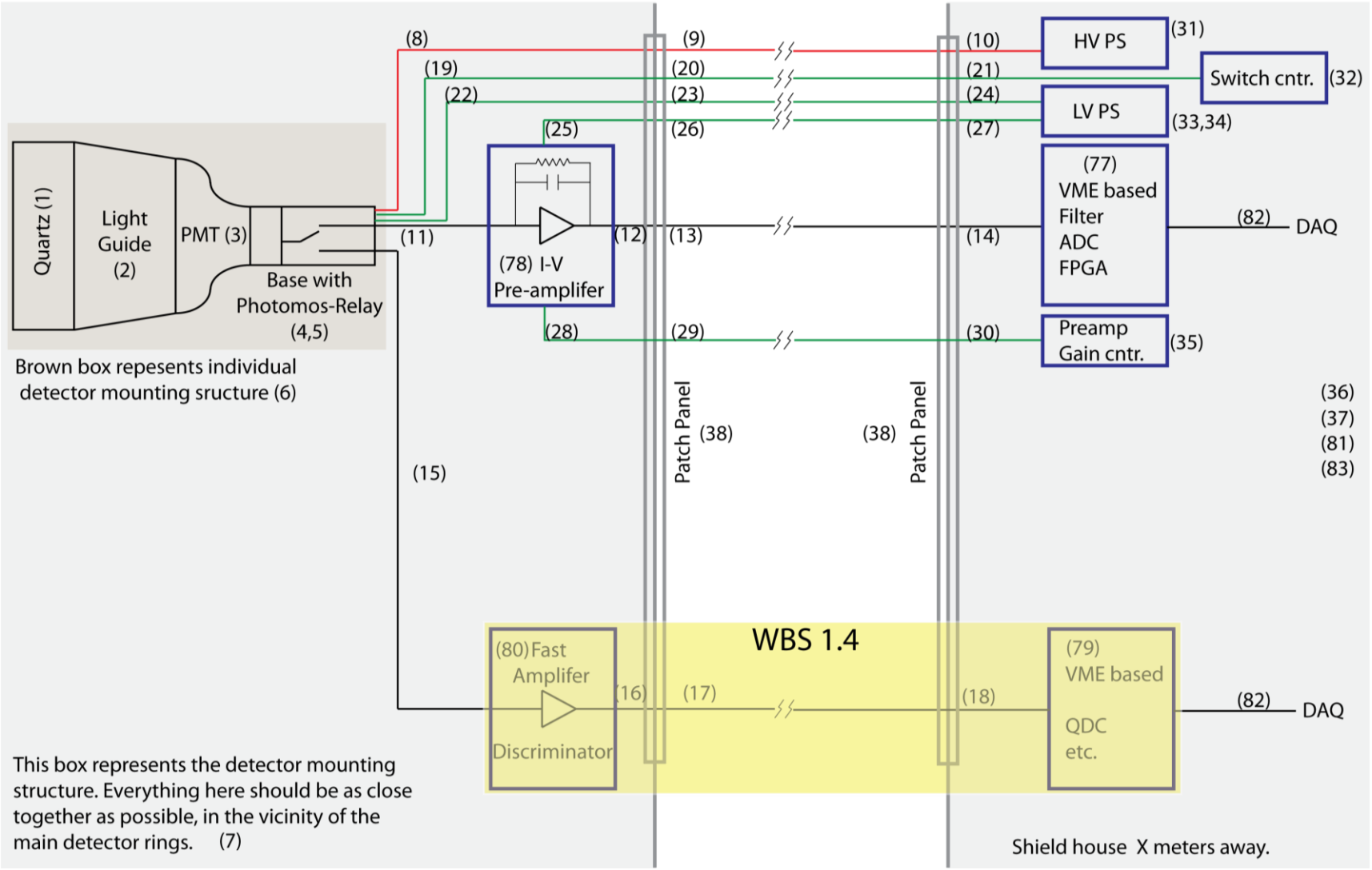
$$G^{\pm} \equiv \Gamma_C^{\pm} Q_{PE}\, g_{PMT}\, g_{amp}^{\pm} \left(1 + \varepsilon \Gamma_C^{\pm} + \ldots\right)$$ plus ADC

Detector yields are integrated (summed) over each helicity state
Raw asymmetries are formed from differences between positive and negative helicity states within a quartet

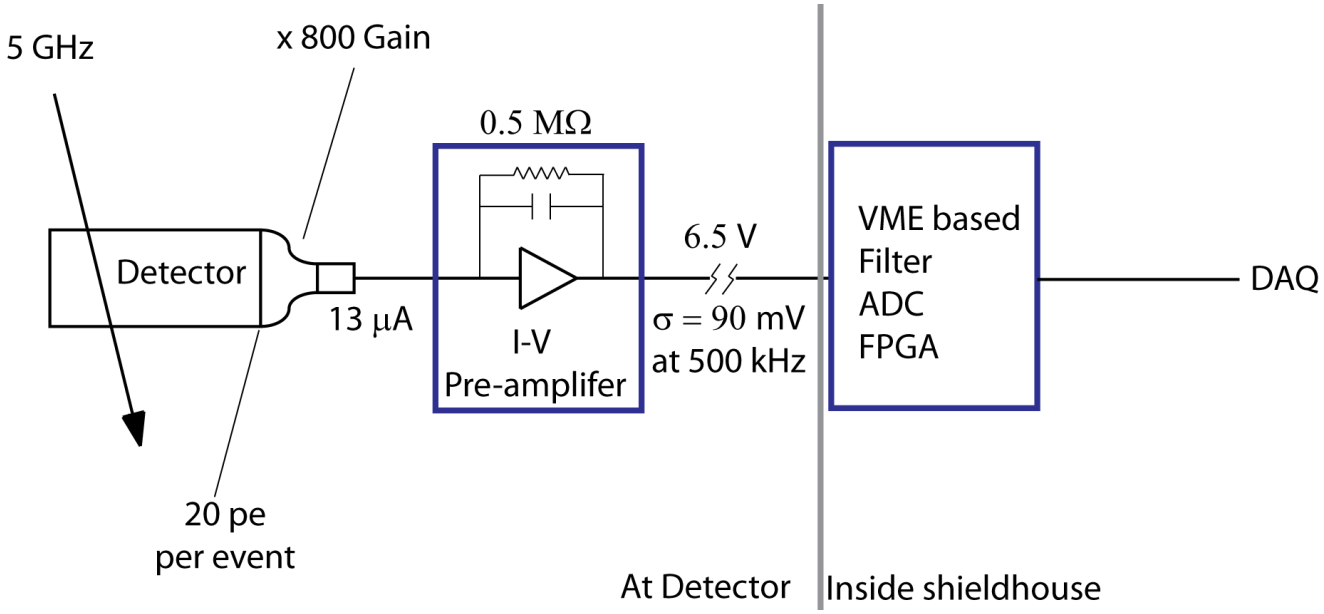




Integrating Detector Electronics



Integrating Detector Electronics



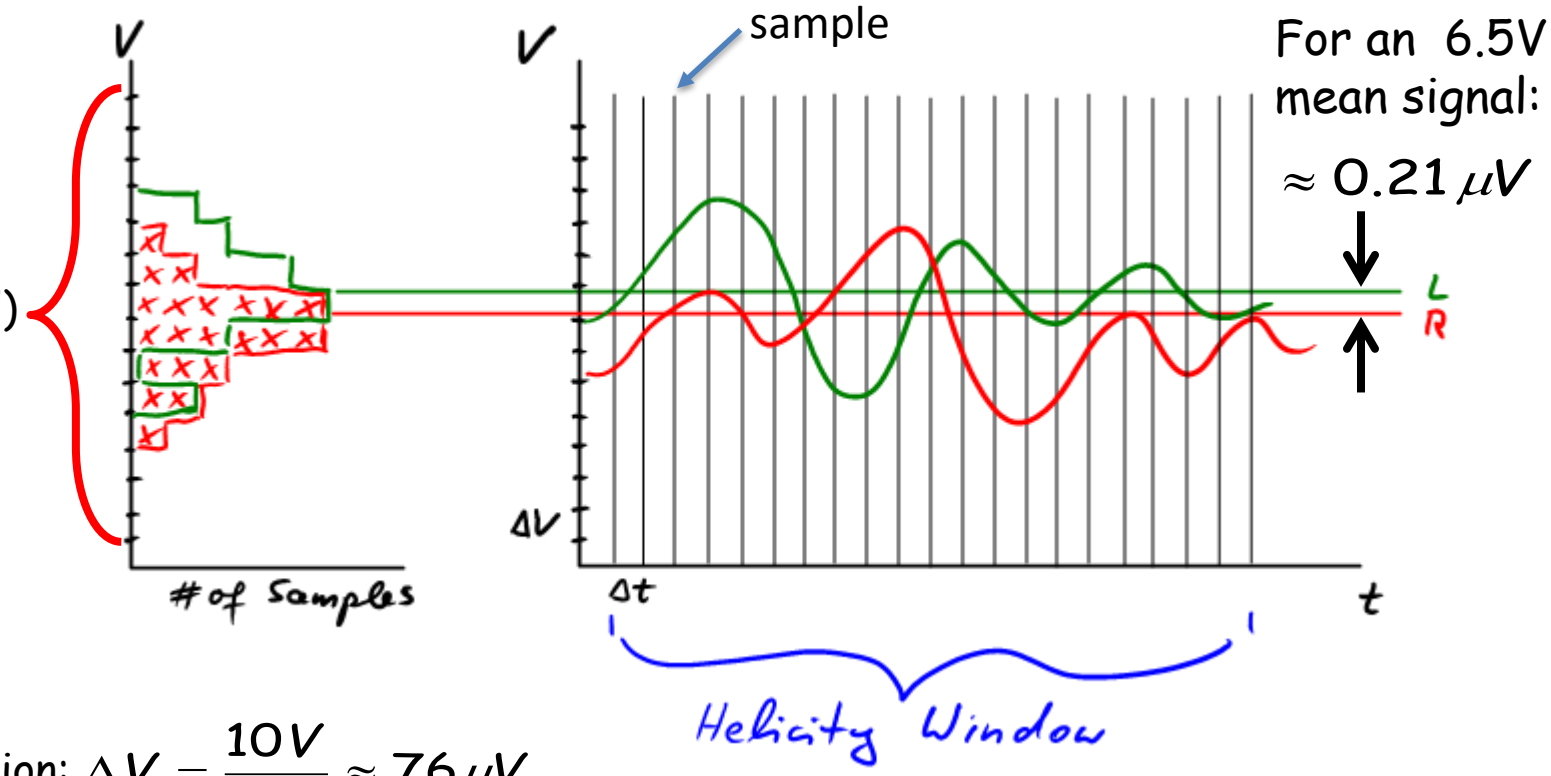
At full rate, mean signal will be about 6.5 V

with RMS of 90 mV (for a bandwidth of 500 kHz)

Integrating Detector Electronics

Digitization:

ADC range and resolution (0 suppressed)



18 bit Resolution: $\Delta V = \frac{10V}{2^{17}} \approx 76\mu V$

So the signal is spread over about 1180 ADC bins.
This suppresses ADC bit noise and non-linearities.

Integrating Detector Electronics

Electronics design constraints:

- Higher frequency helicity reversal requires a higher ADC sampling rate
- Higher frequency helicity reversal requires a shorter Pockels cell transition
- Helicity correlated and uncorrelated changes in beam position, angle, energy and current require the detector signal to be normalized to the beam monitors, so the beam monitors must be read out with the same electronics, at the same sampling rate. RF down-conversion and monitor analysis is practical down to certain bandwidths – so we need to accommodate those bandwidths.
- Electronics must see helicity transition, requiring higher sampling rate and larger bandwidth

More details in backup slides.

Integrating Detector Electronics

These were the Qweak preamps and ADC boards that were developed at TRIUMF

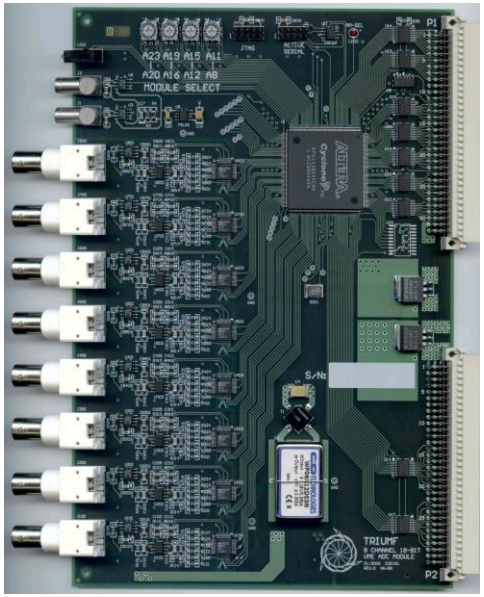
These will be redesigned for MOLLER

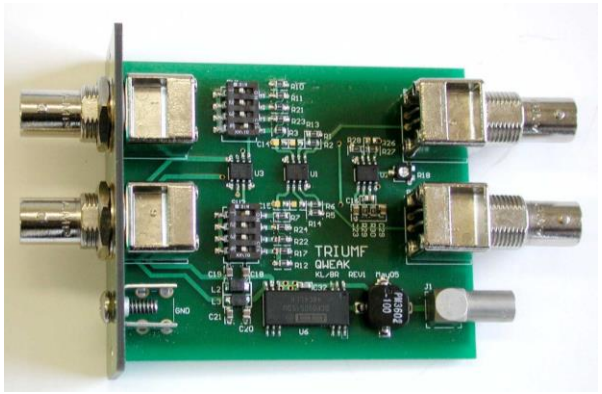
The analog side will be left almost as it was for QWeak, except:

- Higher time resolution ADC
- Higher bandwidth input

Digital side and readout redesign will change to:

- accommodate higher data bandwidth
- modernize the readout infrastructure





Integrating Detector Electronics

Changes needed for MOLLER module (w.r.t. QWeak module):

- Higher bandwidth (~500 kHz)
- Higher sampling rate (≥ 2 Msps)
- ADC resolution (same at 18 bit)
- High ADC linearity
- Small signal delay
- FPGA capability:
  - Read out additional information (mean, RMS, min, max, etc.)
  - Block readout phase shift
  - "Waveform Digitization"
  - Accumulation start-stop times readout

- Improve data readout speed (crate format, protocol, etc.)

Integrating Detector Electronics

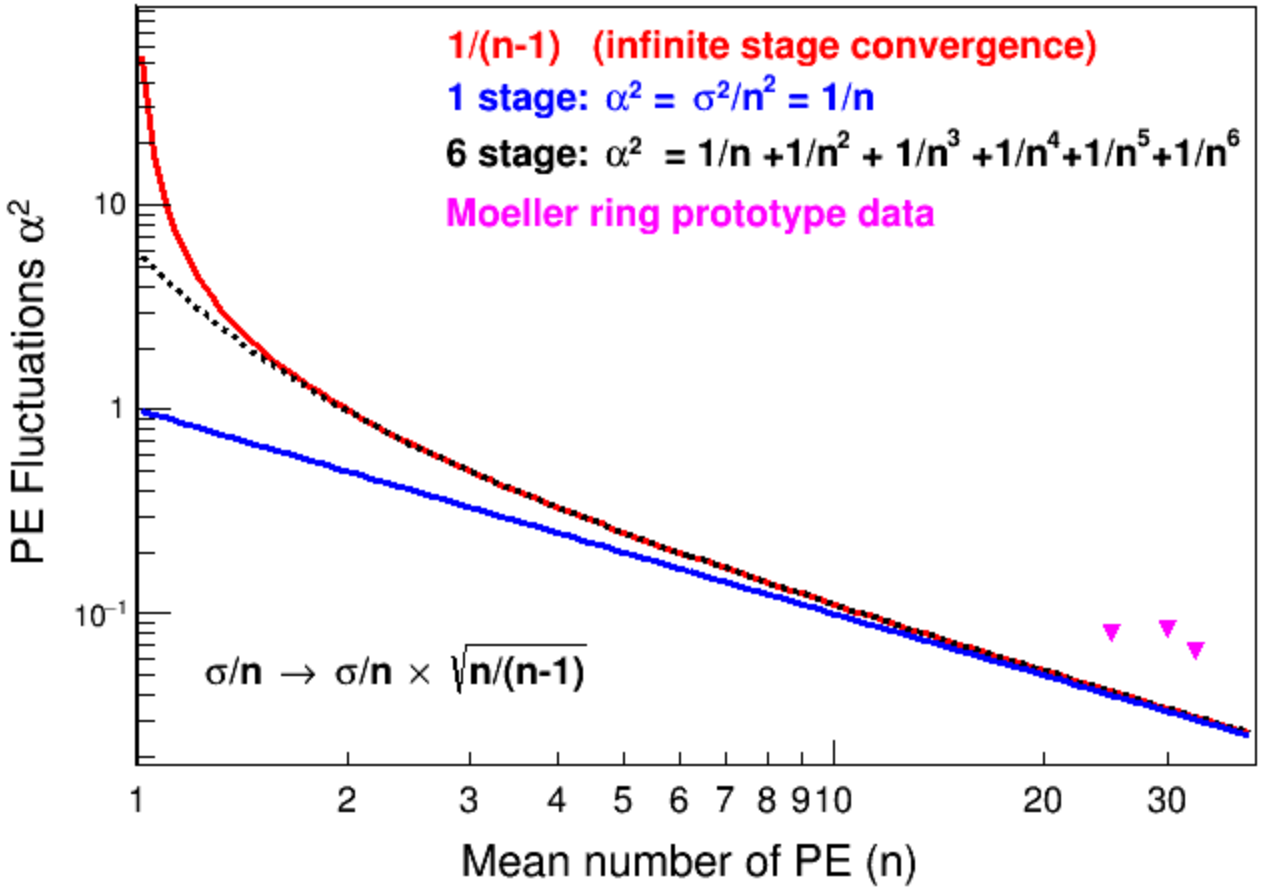
Status:

- Electronics part of a CAD 3.2M CFI (Canada Foundation for Innovation) request submitted for the whole integrating detector array.
- TRIUMF adopted MOLLER as an off-site overseas project and is committed to the electronics development (with or without the CFI success)
- Engineers seem to strongly prefer to move away from VME bus readout
- We can easily go to higher sampling rate and keep or increase resolution without technical drawbacks
- Streaming readout and/or Gigabit Ethernet with CODA (see backup slides).
- We have to develop an initial design or determine specific design changes in the next few months.
- I think we would want to implement the possibility to install new FPGA firmware ourselves … early training for expertise should happen at TRIUMF and if CFI successful hire technician to support this at Jlab.

Integrating Detector Electronics

Backups

Backup


1/(n-1) (infinite stage convergence)
1 stage: $\alpha^2 = \sigma^2/n^2 = 1/n$
6 stage: $\alpha^2 = 1/n + 1/n^2 + 1/n^3 + 1/n^4 + 1/n^5 + 1/n^6$
Moeller ring prototype data
$\sigma/n \rightarrow \sigma/n \times \sqrt{n/(n-1)}$
PE Fluctuations α^2
Mean number of PE (n)
10
1
10^{-1}
1 2 3 4 5 6 7 8 9 10 20 30

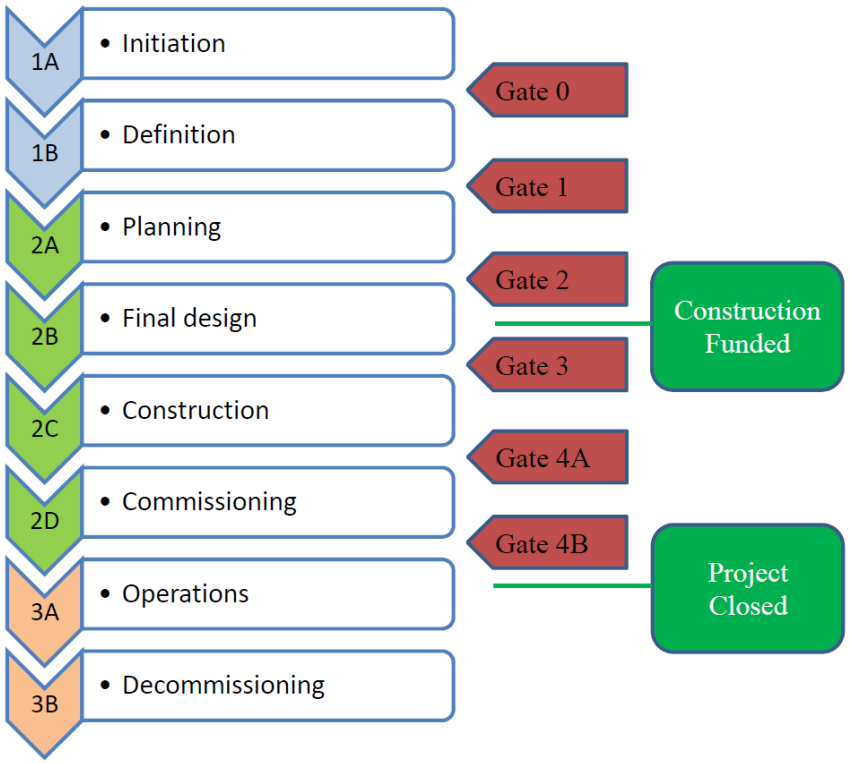
Backup

Project status at TRIUMF:

- Gate 0 (done March 2016)
- Gate 1 (done July 2016)
- Gate 2 (sometime early 2017…)

Gate 2 review documents:

- Initial technical design
- Detailed initial project plan
- Resource loaded schedule (WBS) for two scenarios (w/wo CFI)
- Specify requirements (for TRIUMF) for commissioning and operation
- Specify future FW support needs



Backup

TRIUMF Gate 1 review questions / results:

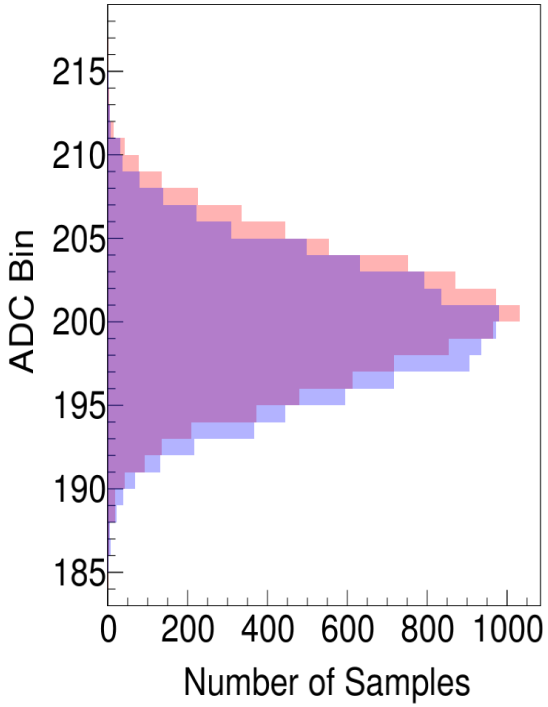
- We have a TRIUMF team:
  - Fabrice Retiere (contact and project manager)
  - Daryl Bishop (lead engineer)
  - Additional (Leonid Kuchaninov, Doug Bryman)

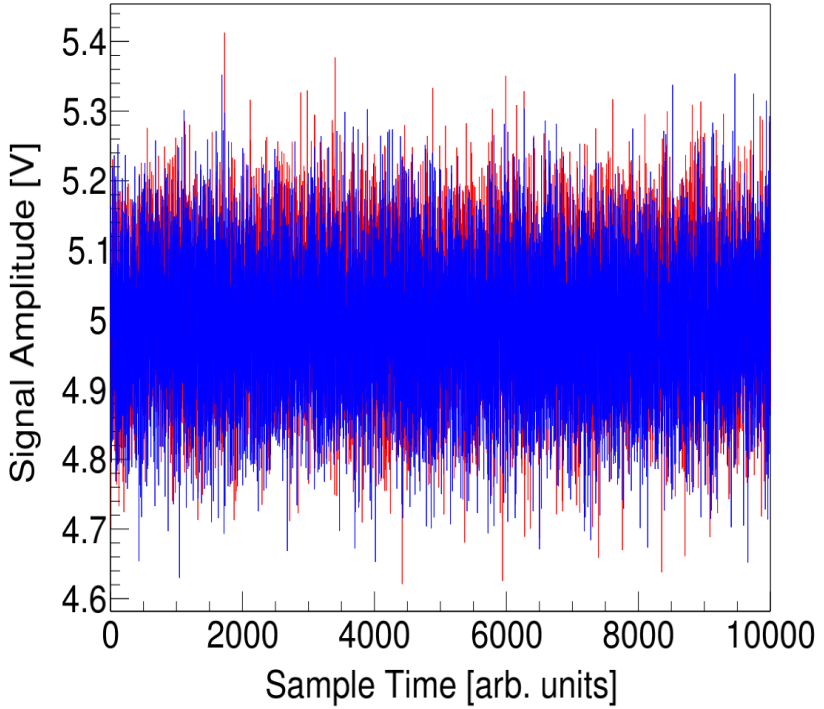
- Requires a full work breakdown structure (WBS) and resource estimate
- Requires project management
- Specific technical questions/suggestions that came up:
  - Do we need BNC format at input
  - FPGA supported data preformatting or direct streaming of ADC data
  - Move away from readout via VME bus – use Gigabit Ethernet
  - If FPGA is used, do we require frequent changes of FW – can we do it ourselves?
  - Suggesting new 18 bit, 15 Msps ADC – facilitates some form of waveform digitization if quartz detectors are slow …
  - Full or semi differential signal ?

Backup

Digitization:

ADC range and resolution (0 suppressed)





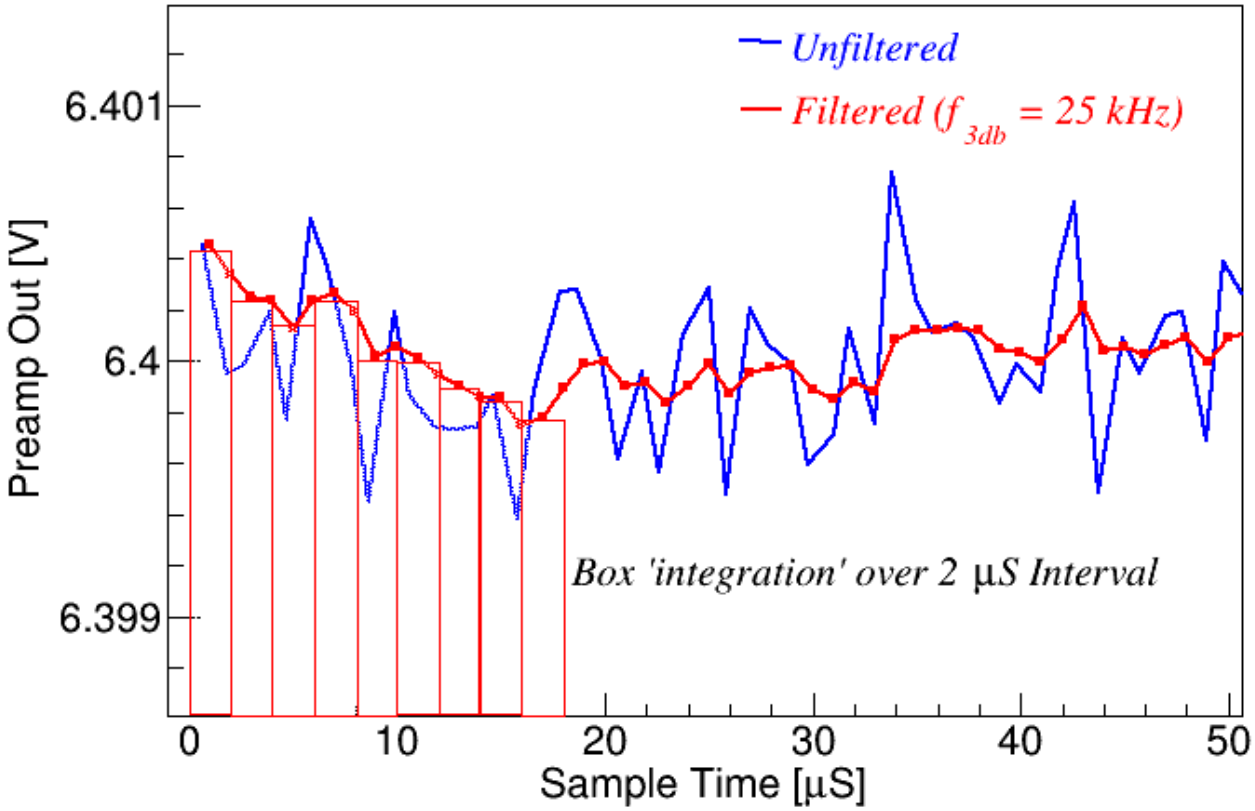
18 bit Resolution:

$$\Delta V = \frac{10V}{2^{17}} \approx 76\mu V$$

Backup

QWeak ADC integration scheme:

- at highest rate samples every 2 μs
- filtering should be consistent with sampling rate, bit noise, and ADC non-linearity
- higher helicity reversal would mean smaller number of samples per window
- unless we increase the sampling rate



Backup

Example Detector Signal:

$$G_{PMT} = 800 \qquad G_{AMP} = 0.5\ M\Omega \qquad R_e = 5\ GHz$$

$$N_{pe} \approx 20 \quad \Rightarrow \quad q_{cath} \approx 32 \times 10^{-19}\ C\ /\ track$$

$$i_C = 1.6 R_e N_{pe} \times 10^{-10}\ nA \simeq 16\ nA$$

$$i_A = i_C G_{PMT} \simeq 13\ \mu A$$

$$S = i_A G_{AMP} = 6.5\ V$$ at the ADC input

$$B = 500\ kHz$$ equivalent noise bandwidth

$$\sigma_{Shot} = \sqrt{2 q_{cath} i_C} \cdot \sqrt{B} \cdot G_{PMT} \approx 180\ nA \quad \Rightarrow \quad \approx 90\ mV$$

Backup

- The rate varies by a factor of 100 across the detector tiles
- Signal range will be about
  - Cathode current $\langle i_c \rangle \simeq 0.1 \rightarrow 50 \ \ nA$
  - RMS $\sigma_{i_c} \simeq 25 \rightarrow 570 \ \ pA$
- ADC ranges ~ 0 to 10V so we don't have a factor of 500 in range
  - Have to play with PMT gain and preamp gain
  - PMT gain has a lower limit because of non-linearity effects
  - Different preamp gains means different noise behavior
  - Design of signal electronics (PMT to ADC board output) from here on out requires knowledge of rates and detector properties

Backup

- Higher frequency helicity reversal requires a higher ADC sampling rate
- Higher frequency helicity reversal requires a shorter Pockels cell transition
- Helicity correlated and uncorrelated changes in beam position, angle, energy and current require the detector signal to be normalized to the beam monitors, so the beam monitors must be read out with the same electronics, at the same sampling rate. RF down-conversion and monitor analysis is practical down to certain bandwidths – so we need to accommodate those bandwidths.

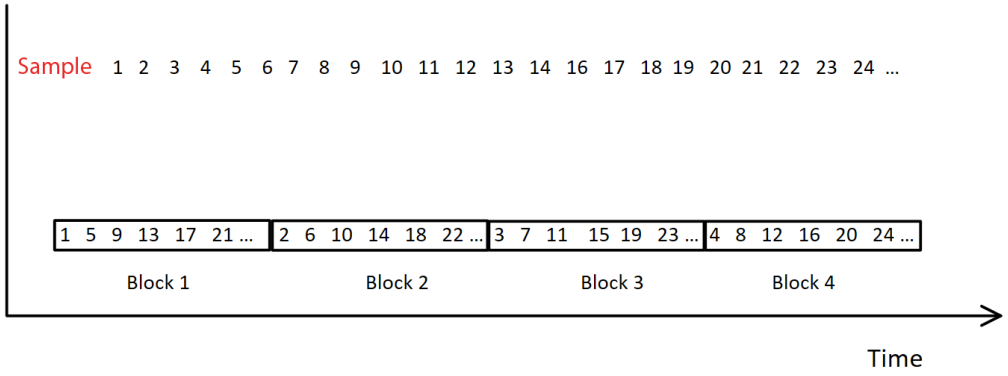
- Electronics must see helicity transition, requiring higher sampling rate and larger bandwidth

  - Goal transition time: $t_{set} = 10\,\mu s$
  - Settle to 0.01% of final value corresponds to 9 time constants or a 1.1 μs time constant
  - Minimum bandwidth is then $f_{3db} = 0.35 / \left(2.2 \times 1.1\ \mu S\right) \simeq 150\,kHz$
  - The noise equivalent bandwidth is $\frac{\pi}{2} f_{3db} \simeq 240\,kHz$ ⇒ $B = 500\,kHz$

Backup

- Higher frequency helicity reversal requires higher ADC sampling rate
  - Helicity window at 2 kHz reversal : $\Delta t = 500\,\mu s$
  - Subtract Pockels cell settle and electronics delays : $\Delta t = 460\,\mu s$ (?)
  - Divide window into 4 blocks to do systematic analysis : $\Delta t_B = 115\,\mu s$
  - To get a reasonable number of samples per block take a sample every μs

    ≥ 1 *Msps*
  - Already more or less dictated by Pockels cell settle anyway.



Backup

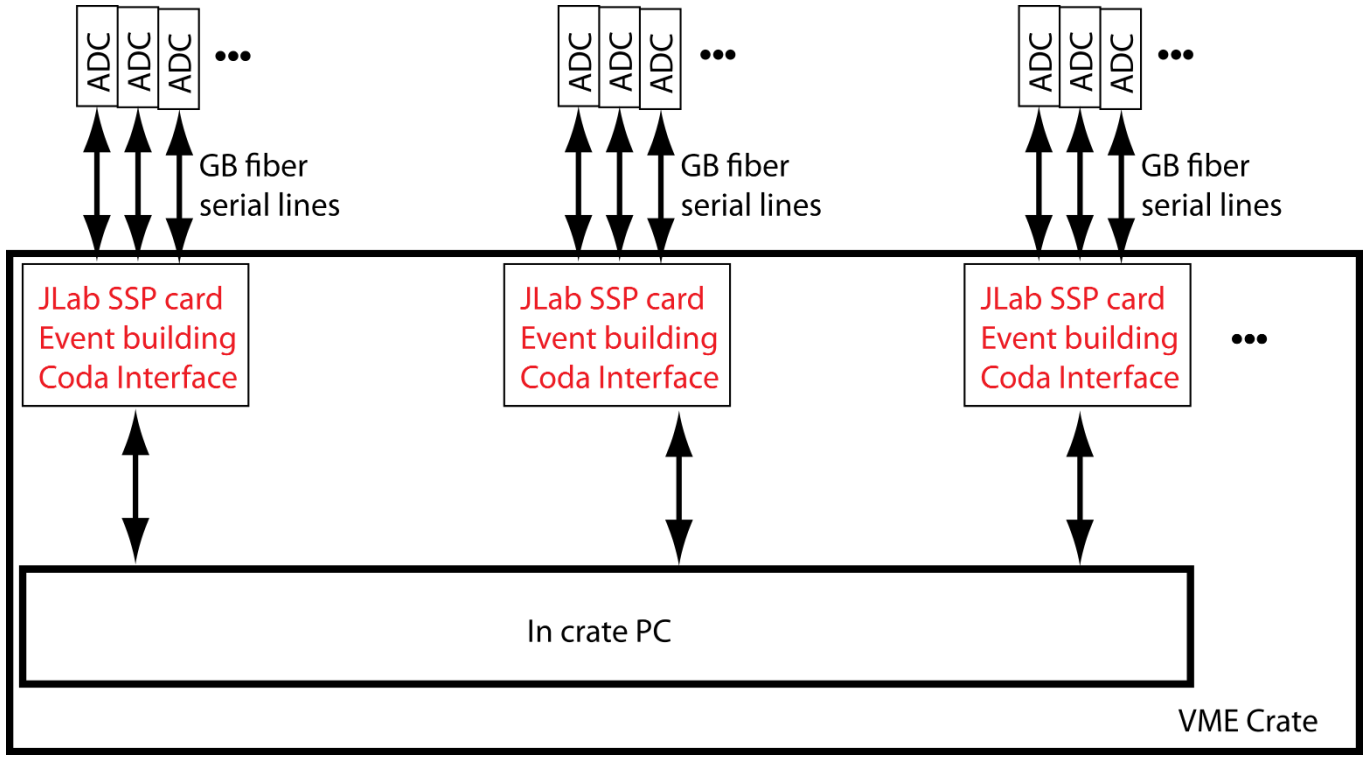
- Use continuous sampling of filtered preamp signal with gated collection of data
  - Currently considering a 15 Msps, 18 bit ADC
  - At production helicity rate: Read out data for each helicity window separated into 4 blocks and all together = 5 data units
    - Each data unit consists of 4 items: The mean, minimum, maximum, and rms of the collected samples (calculating these is done in the FPGA)
    - At 15 Mbits ~6900 ADC samples per block from which to calculate these
    - 4 bytes for each data item in 5 data units = 80 bytes / channel / window
    - 8 bytes for one timestamp per helicity window -> 88 bytes / channel /window
    - 8 channels per board with one readout link -> < 1kB / helicity window per board
  - For diagnostic purposes readout every ADC sample
    - Data link and protocol determine the maximum "event" rate …

Backup

ADC FPGA Interface options to JLab system:

Synchronization taken care off by SSP module and TS

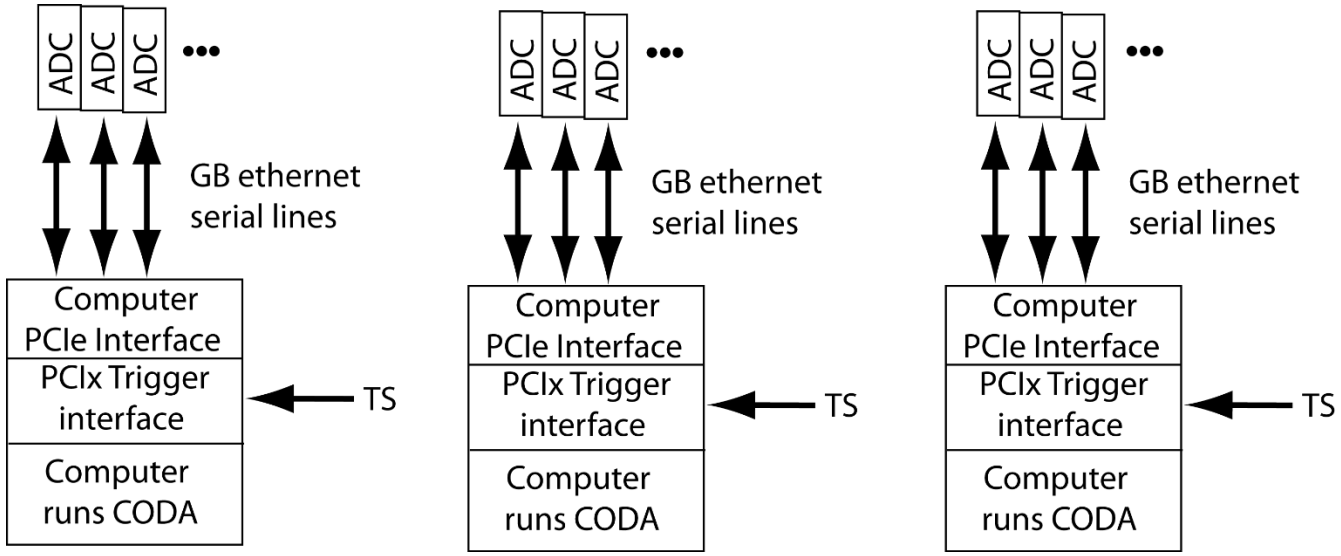
Computers need to be synchronized by a common clock



Backup

ADC FPGA Interface options to JLab system:

Separate PCs with PCIe interfaces (no VME):



Backup

LINEAR TECHNOLOGY

LTC2387-18

18-Bit, 15Msps SAR ADC

FEATURES

- **15Msps Throughput Rate**
- **No Pipeline Delay, No Cycle Latency**
- **95.7dB SNR (Typ) at f_{IN} = 1MHz**
- **102dB SFDR (Typ) at f_{IN} = 1MHz**
- **Nyquist Sampling Up to 7.5MHz Input**
- Guaranteed 18-Bit, No Missing Codes
- ±3LSB INL (Max)
- 8.192V_{P-P} Differential Inputs
- 5V and 2.5V Supplies
- Internal 20ppm/°C (Max) Reference
- Serial LVDS Interface
- 125mW Power Dissipation
- 32-Pin (5mm × 5mm) QFN Package

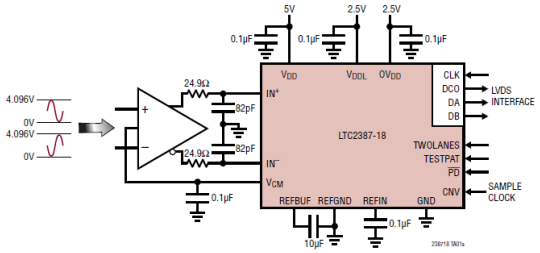
APPLICATIONS

- High Speed Data Acquisition
- Imaging
- Communications
- Control Loops
- Instrumentation
- ATE

DESCRIPTION

The LTC®2387-18 is a low noise, high speed, 18-bit 15Msps successive approximation register (SAR) ADC ideally suited for a wide range of applications. The combination of excellent linearity and wide dynamic range makes the LTC2387-18 ideal for high speed imaging and instrumentation applications. No latency operation provides a unique solution for high speed control loop applications. The very low distortion at high input frequencies enables communications applications requiring wide dynamic range and significant signal bandwidth.

To support high speed operation while minimizing the number of data lines, the LTC2387-18 features a serial LVDS digital interface. The LVDS interface has one-lane and two-lane output modes, allowing the user to optimize the interface data rate for each application.



Jefferson Lab