Manual for the UMD-built AMPLIFIER/SUMMER NIM modules and details of the CEBAF Hall A shower counter electronics.

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(1) SPECIFICATIONS FOR AMPLIFIER/SUMMER NIM MODULE

(1.1) Purpose of device

The module amplifies photo-multiplier signals (50 ohm Lemo inputs) for processing by ADCs via 100 ohm twisted-pair cables as pseudo-ECL signals or by 50 ohm coaxial ribbon cables. The module also adds (multiplexes) two groups of up to seven amplified signals each and supplies the result in three parallel 50 ohm Lemo front panel outputs each for subsequent processing via commercial NIM modules.

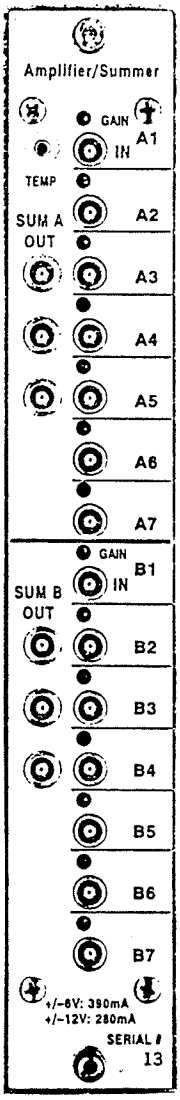


FIG.1:
Front Panel

(1.2) Inputs (Fig. 1)

14 channels in 2 module-sections of 7 inputs each;
front panel 50 ohm Lemo inputs;
negative or positive signals of up to +/- 5 V amplitude;
each input protected after input attenuator via diodes
at +/-6 volt.

- individual channel gains of 25/2.0 [high gain/low gain version]
- summed channel gains at half individual channel gains;

the "standard" front panel setting is 40% of maximum (overall gain of 10/0.8).

(1.8) Cross talk

Below 2% between adjacent channels and less between non-adjacent channels for 5 ns rise-time signals, if all outputs are terminated; decreases with increasing rise-time of signal.

(1.9) Random high frequency noise

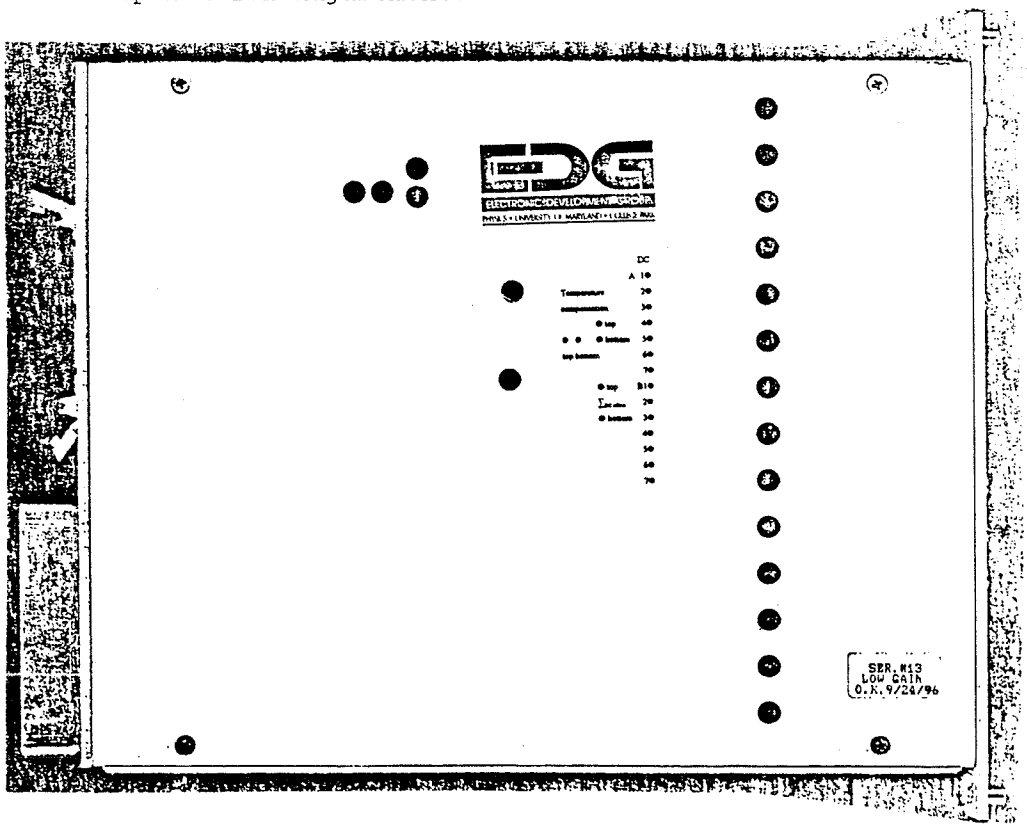
~ 0.2 mV peak-to-peak non-attenuated-input equivalent for individual channels at ~100 MHz;

~< 0.2 mV input-equivalent for summed channels at 30 ns output rise time [from ADC: summed channel: 2 mV at maximum-gain setting of 15].

(1.10) DC offset control (Fig. 3)

Side panel accessible control for each channel;
side panel accessible additional control for each summed output;
side panel accessible adjustable temperature drift compensation for each summed output;
temperature sensor output at front panel;
DC offset will change slightly with front panel gain setting;
DC offset and temperature compensation setting needs to be readjusted after any internal gain change;
for count rates below ~ 100 KHz external AC coupling can be used to eliminate any DC offsets and offset drifts.

FIGURE 3: Side panel with access holes for DC and temperature compensation adjustment.



total gain is G = F * G1 * G2 * 0.5. The "standard" gain is G=10, with F=0.4, G1=5.0, and G2=10.0, providing a gain range of G = 0...25 with F varied from 0 to 1.0. If 100 ohm back-termination is desired, the circuit-board trace parallel to R78 can be cut to provide 100 ohm pseudo-differential termination on the amplifier output.

(2.3) Summing branch (Figs. 4,5)

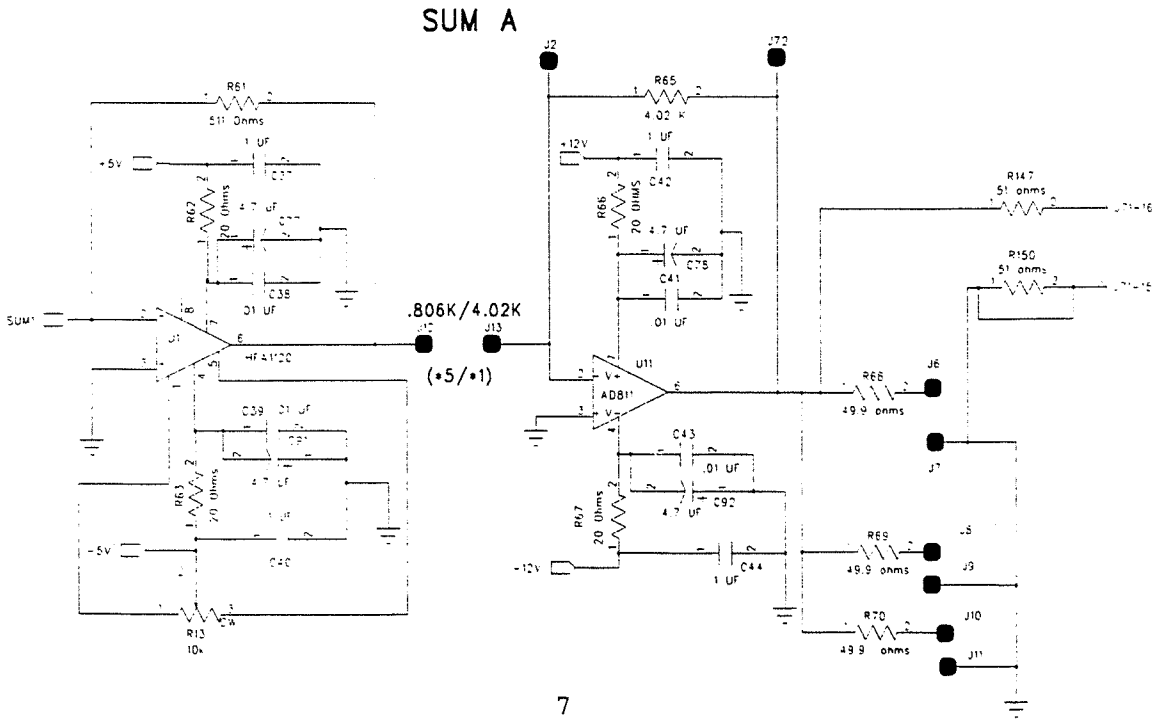
The second output of U4 goes via R14,18 and R9 to ground through a total of 100 ohm (the SUM1 input from R9 is at virtual ground). Half the signal - to minimize cross talk between channels - is summed through R9, along with channels A2 to A7 and the temperature compensation output, into the inverting input of U1. The gain G3 of U1 in the inverting configuration is G3 = -R61/R9. A fixed gain of -2.0 (R9 = 255 ohm) is chosen to compensate for the R18,R14,R9 signal attenuation.

U11 provides the final summed-signal amplification, with the output rise time controlled by the feedback resistors R65 and any resistor placed between J2 and J72 (call it R65'). The gain resistor (Rg), placed between J12 and J13, should be chosen so that
Gain = -1.[(1/R65+1/R65') * Rg]. The default values are R65 = 4020 ohm, Rg = 806 ohm for a gain of -5.0 and a rise time of at least 30 ns. Measured rise-time and random-noise total-amplitude values for a gain of -5.0 in U11 with an overall gain of 100 are (R65' = 0 ohm):

		rise time (ns)		
R65(ohm)	Rg(ohm)	10/90%	10/80%	noise (mV)
511	102.5	<10	7.5	44
1100	222	19	14	27
1960	392	28	21	17
5460	1100	74	53	14

The output is deliberately slowed down to make the summed output less sensitive to mismatches in input signal arrival times. It also makes timing of subsequent multiplexer modules easier. In addition, the

FIGURE 5: Summing circuit, channel A.



at the sensor.

A second amplifier (U35B) provides an identical output of opposite polarity. A potentiometer (R316) between the two amplifier outputs allows to select the desired temperature sensitivity; a test point (use high impedance) (J31-1) is provided for monitoring the adjustment. At 0 mV test point value there is no temperature compensation. Potentiometer and test point are accessible through holes in the module's side cover.

The potentiometer output feeds into the summing input of the first summing amplifier (U1) via a 5.1 kohm resistor (R322); together with the 511 feedback resistor (R61) this results in a gain of 0.1. The second summing amplifier (U11) gain resistor (between J12 and J13) is normally set to 806 ohm or 4.02 kohm, resulting in a GAIN of 5.0 or 1.0 (assuming the normal 4.02 kohm feedback resistor R65). Thus the test point value is normally attenuated by a factor of ATTEN = 0.5 or 0.1 when viewed at the front panel summed output (using >1 Mohm instrument).

The temperature compensation adjustment is accompanied by a DC offset which has to be removed with the summed signal DC offset potentiometer (R13), accessible through the side panel.

EXAMPLE (all measurements with a >1 Mohm voltmeter):
An increase of temperature of 30 degF from 90 to 120 degF will result in a front panel voltage change from 1.80V to 2.40V, i.e. by +0.60V (20 mV/degF). If the potentiometer was set to yield a test point value of -225 mV at 90 degF, its value will change by 0.60/1.80*(-225mV)= -75 mV to -300 mV, or by -2.5 mV per degF at the test point.
At the front panel summed output this translates into

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      -2.5 mV * ATTEN * temperature-change,
i.e., -2.5 mV * 0.5   * 30 = -37.5 mV at GAIN=5.0
or                         = - 7.5 mV at GAIN=1.0.
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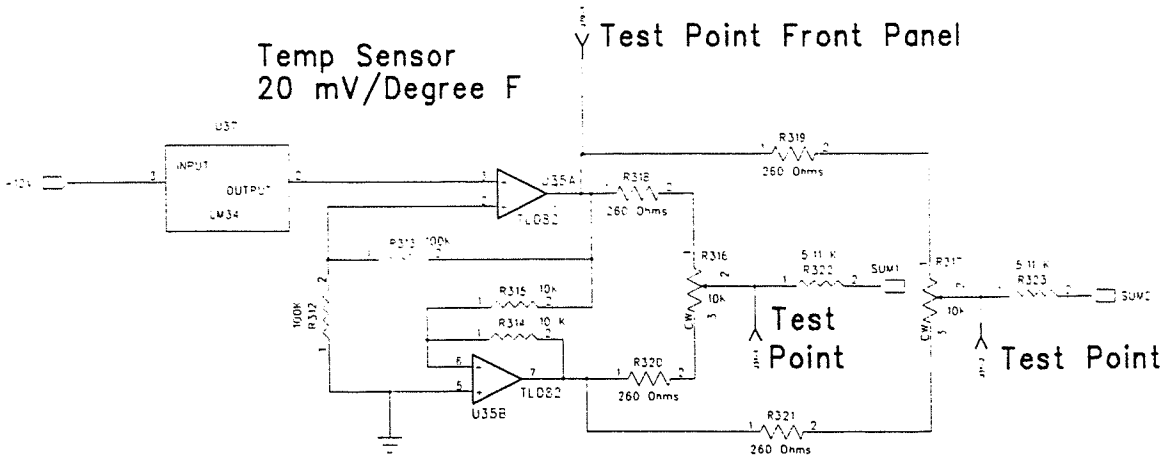
FIGURE 6: Temperature compensation circuit.



Note: all measurements are assumed to be made with high-ohm voltmeter;
if a 50 ohm instrument is used, the summed output values are
attenuated by a factor of 0.5.

(1) Make sure that the internal amplifier gains have been set to the desired values. First-stage gain changes (white potentiometers) require new temperature compensation settings; front panel gain changes do not.
(2) Determine the summed output gain, defined by the removable gain resistor (4.02 kohm: gain of 1.0; 804 ohm: gain of 5.0).
(3) - Insert insulated leads (modified Lemo cables) into testpoints to allow voltmeter measurement.
- Place unit into a NIMBIN with forced air flow (fans) with space for potentiometer adjustment through the side panel from the left.
- Turn on NIM power and wait at least 15-30 minutes for temperature equilibrium (temperature sensor is much faster than amplifiers!).
- Keep forced air flow (fans) on at all times.
(4) Turn temperature compensation (TC) potentiometers to achieve 0 +/-1 mV reading at test point through side panel opening.
(5) Measuring at front-panel Lemo summed-output, adjust the DC level to 0 mV offset.
(6) Measure and record
- the front panel TEMP value and
- the summed output DC-offset value.
(7) Use a space heater or similar device to increase the air temperature which is drawn through the unit, to simulate an environmental temperature change. (Note: blocking air flow to increase the internal temperature instead of changing the temperature of the forced air flow does not yield adequate results.)
(8) After 30 to 60 minutes equilibrium should be achieved. Measure and record the TEMP and summed-output DC values for this temperature.
(9) Remove heater, let cool down, measure TEMP and DC-offsets again.
(10) Determine the change in testpoint value needed by:
NEEDED = -10.0 * delta-DC / delta-TEMP * TEMP / GAIN , where
- = want to compensate, not enhance;
10.0 = 1/gain of first amplifier stage for temperature stabilization circuit;
delta-DC = change in summed output DC value (into 1 Mohm);
delta-TEMP = change in front panel TEMP test point value;
TEMP = Value of TEMP output at the time of potentiometer adjustment;
GAIN = second summing amplifier gain (see above), 5.0 or 1.0;
(12) Measure side panel test point value, add "NEEDED" to value, and adjust potentiometer to the new value (test-point + NEEDED).
(13) Adjust summed-output DC offset to 0 mV.
(14) If desired, further iterations ((6) to (13)) can be done.

Note: At an internal gain of 12.5 into 50 ohm for the summed output (i.e., "HIGH GAIN" setting), typical drift values are 0.3 mV/degF. Compensation reduces this to about 0.05 mV/degF.
Individual channels drifts at the same "HIGH GAIN" internal setting of 25.0 have been measured for four modules, with an average of 0.11 mV/degF into 50 ohm. The individual results are:

Module 3: A1-7: +0.07, 0.12, 0.01, 0.07, 0.16,-0.07, 0.12 mV/degK
B1-7: +0.32, 0.15, 0.11, 0.17, 0.05, 0.15,-0.07 mV/degK
4: A1-7: +0.08, 0.16, 0.17, 0.16,-0.01, 0.16, 0.16 mV/degK
B1-7: +0.07, 0.19, 0.26, 0.18, 0.17, 0.17,-0.03 mV/degK
5: A1-7: +0.07, 0.06, 0.05, 0.03, 0.21, 0.09, 0.13 mV/degK
B1-7: +0.02, 0.08, 0.19, 0.14,-0.01, 0.02, 0.08 mV/degK
6: A1-7: +0.19, 0.24, 0.07, 0.20, 0.19, 0.06,-0.02 mV/degK
B1-7: +0.16,-9,12,-0.02, 0.01, 0.10, 0.01, 0.18 mV/degK

(6) USE OF SUMMING FEATURE FOR HALL-A SHOWER COUNTER

(6.1) Shower counter and signal cable details

The CEBAF Hall-A Electron Spectrometer Shower-Counter consists of an array of 2x24 = 48 preshower lead-glass detectors (area of 35x10 cm**2 each) and an array of 6x16 = 96 total absorption detectors (15x15 cm**2 each).

The two arrays are placed behind each other and can be viewed as 8 identical SEGMENTs in which preraditors (2x3 detectors = 70x30 cm**2) and total absorption detectors (6x2 detectors = 90x30 cm**2) exactly overlap, with an extra 10 cm of total absorption counter on each side to contain the expanding shower. Detectors and signal cables are numbered as given in Table 2.

TABLE 2: Relative location and cable numbering scheme for HALL A shower counter detectors. Orientation shown is as seen from the target (along the spectrometer z-direction), with the low momentum region at the top (low detector numbers).

Preradiator	total Absorber	
1L 1R	6 5 4 3 2 1	
2L 2R	12 11 10 9 8 7	= SEGMENT 1
3L 3R		
4L 4R	18 17 16 15 14 13	
5L 5R	24 23 22 21 20 19	= SEGMENT 2
6L 6R		
7L 7R	30 29 28 27 26 25	
8L 8R	36 35 34 33 32 31	= SEGMENT 3
9L 9R		
10L 10R	42 41 40 39 38 37	
11L 11R	48 47 46 45 44 43	= SEGMENT 4
12L 12R		
13L 13R	54 53 52 51 50 49	
14L 14R	60 59 58 57 56 55	= SEGMENT 5
15L 15R		
16L 16R	66 65 64 63 62 61	
17L 17R	72 71 70 69 68 67	= SEGMENT 6
18L 18R		
19L 19R	78 77 76 75 74 73	
20L 20R	84 83 82 81 80 79	= SEGMENT 7
21L 21R		
22L 22R	90 89 88 87 86 85	
23L 23R	96 95 94 93 92 91	= SEGMENT 8
24L 24R		

FIG. 7: Circuit diagram showing the summing of shower counter detector analog signals from the preradiator (Pre-rad) and total absorber (Tot-abs) to form logic signals in the discriminators (dis-cri-min.) to be used for time-to-digital converters (TDC) and as input to trigger logic decisions in the Logic unit. For details see text.

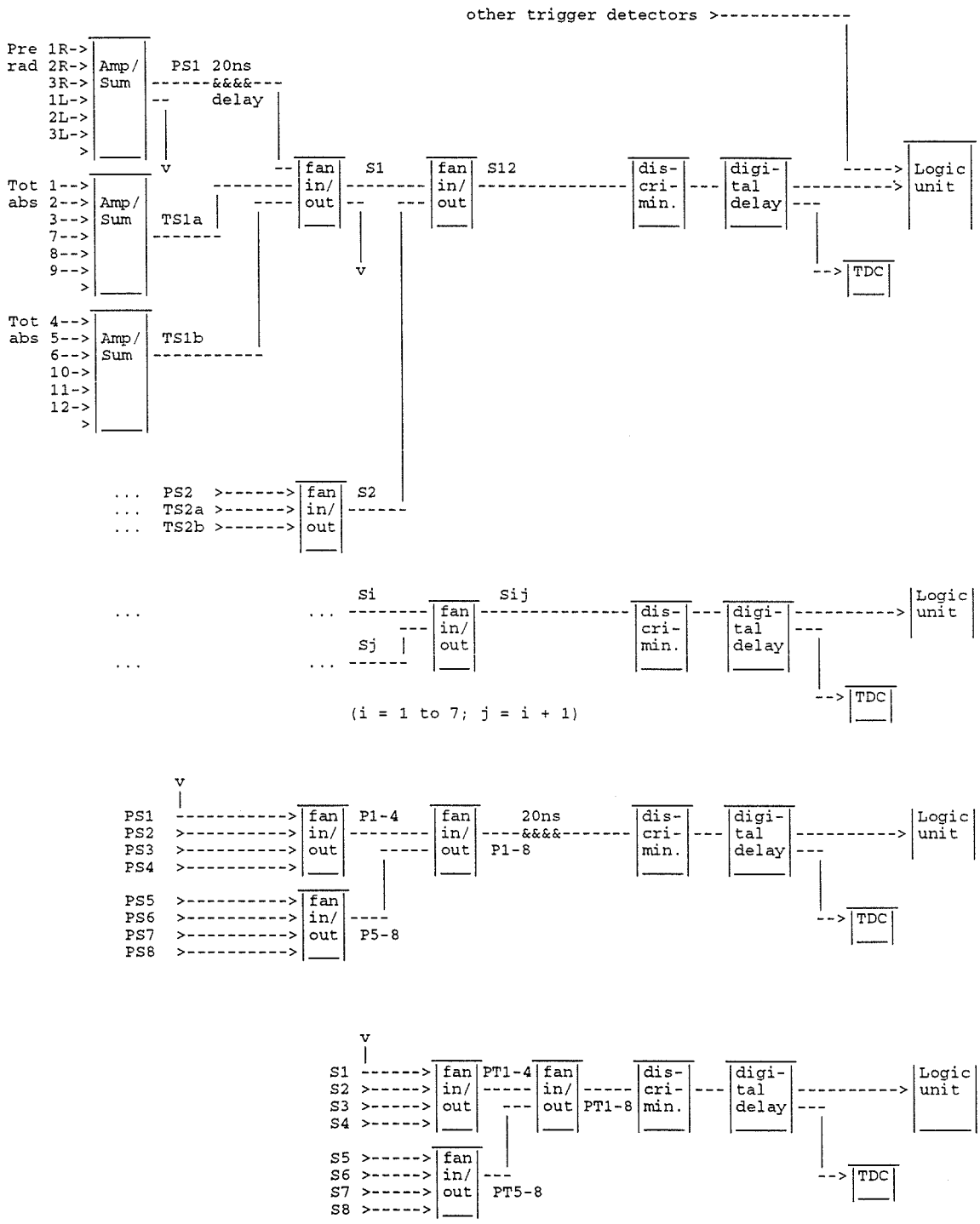


FIGURE 8: NIM-Bin slot population with Amplifier/Summer modules and with fan-in/out modules for the two NIM-Bins in use.
The output signals of the module-sections are given with the notations used in Fig. 7.
The connections are made with cables as indicated.
The discriminators are located in a separate Camac crate.

slot # 1	2	3	4	5	6	7	8	9	10	11	12
Amp/ Sum	Amp/ Sum	spare	Amp/ Sum	Amp/ Sum	Amp/ Sum	Amp/ Sum	spare	fan i/o	fan i/o	fan i/o	spare
PS1	PS3		TS1a	TS1b	TS3a	TS3b		S1	S12	spare	
								S2	S23	P1-4	
PS2	PS4		TS2a	TS2b	TS4a	TS4b		S3	S34	P5-8	
								S4	S45	P1-8	
PS5	PS7		TS5a	TS5b	TS7a	TS7b		S5	S56	PT1-4	
								S6	S67	PT5-8	
PS6	PS8		TS6a	TS6b	TS8a	TS8b		S7	S78	PT1-8	
								S8	spare	spare	

cables lengths used, in nanoseconds:
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for i = 1 to 7; j = i + 1:
  PSi -- 24ns -- Si
  TSia -- 4ns -- Si -- 1ns (2ns @ i+1=5) -- Sij -- 9ns --- Discriminator # i
  TSib -- 4ns -- Si

for i = 1 to 4; j = 5 to 8:
  Si -- 4ns -- PT1-4 -- 1ns -- PT1-8
  Sj -- 4ns -- PT5-8 -- 1ns -- PT1-8 -- 1ns -- Capacitor -- 8ns -- Discr. # 8

  PSi -- 4ns -- P1-4 -- 1ns -- P1-8
  PSj -- 4ns -- P5-8 -- 1ns -- P1-8 -- (20ns) ------ 9ns -- Discriminator # 9

Note that some cables are color coded with a permanent marker
(sequence: red, green, blue, black) and then tied into bundles.

[above is as cabled on December 17, 1997]