Manual for the UMD-built AMPLIFIER/SUMMER NIM modules and details of the CEBAF Hall A shower counter electronics.

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(June 30, 1998)

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CONTENTS
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(1) SPECIFICATIONS FOR AMPLIFIER/SUMMER NIM MODULE

(1.1) Purpose of device

The module amplifies photo-multiplier signals (50 ohm Lemo inputs) for processing by ADCs via 100 ohm twisted-pair cables as pseudo-ECL signals or by 50 ohm coaxial ribbon cables. The module also adds (multiplexes) two groups of up to seven amplified signals each and supplies the result in three parallel 50 ohm Lemo front panel outputs each for subsequent processing via commercial NIM modules.

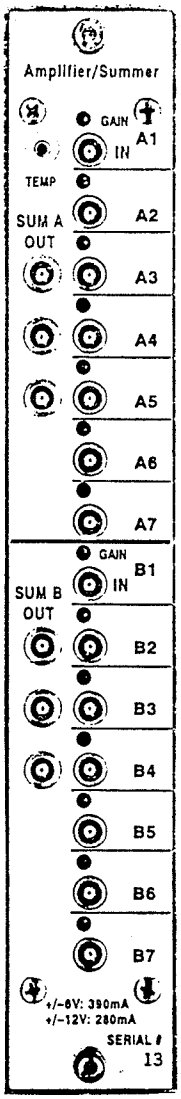


FIG.1:
Front Panel

(1.2) Inputs (Fig. 1)

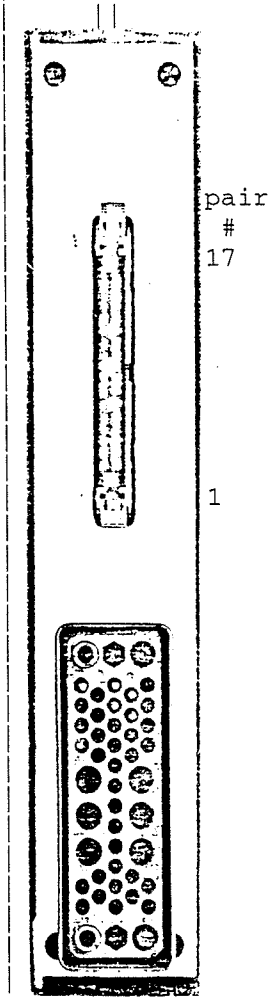
14 channels in 2 module-sections of 7 inputs each;
front panel 50 ohm Lemo inputs;
negative or positive signals of up to +/- 5 V amplitude;
each input protected after input attenuator via diodes
at +/-6 volt.

(1.3) Ribbon cable output (Fig.2)

Located on back panel of module;
back-terminated at output:
- set to 50 ohm for use with 50 ohm coaxial or 100 ohm ribbon cable;
- easy (permanent) change to 100 ohm pseudo-differential possible;

maximum output amplitude approx. +/-4.5 V into 50 ohm (can be increased by changing back-term. resistor);
rise time for individual outputs: about 5 ns;
rise time for summed outputs (pair 8, 16) set to about 30 ns; rise time can be shortened by changing internal resistor);
pair 1-7: amplified input signals A1-A7,
pair 8: sum of signals A1-A7,
pair 9-15: amplified input signals B1-B7,
pair 16: sum of signals B1-B7,
pair 17: ground.

FIG.2:
Back Panel



(1.4) Summed outputs, front panel Lemo connectors

Located on front panel as 50 ohm Lemo outputs (Fig. 1);
3 parallel, individually back-terminated outputs for each of the two sections;
maximum output amplitude: about +/- 4.5 V into 50 ohm, limited by maximum output current of 100 mA if more than one output per section are used;
rise time: ~30 ns (reducible via changes of internal resistors).

(1.5) Input-Output transit time

Amplified single-channel outputs <~ 10 ns;
summed outputs about 2-3 ns later than single-channels.

(1.6) Power requirements

+/- 6 V: 350 mA each (+/-10%)
+/- 12 V: 250 mA each (+/-10%)
+/- 24 V: 0 mA each

Note 1: these currents exceed the standard NIM-bin crate standards, but are compatible with proper load distribution or high-power NIM bins.
Note 2: NIM bins tend to drop +12 V or -12 V when power is turned on with more than 6 modules inserted. Check NIM voltage after each power cycle. The modules can be pulled out and reseated with NIM power on to restore the low 12V supply.
Two HALL-A Ortec NIM bins have been modified to avoid this problem.
Note 3: a fan for forced air circulation is recommended.

(1.7) Gain control

Via 15 turn potentiometer (attenuator) accessible at front panel (Fig.1);
front panel potentiometer controls gain from 0.0 to 1.0 times internal gain setting;
additional internal gain control via potentiometers and replaceable resistors (some are on back of circuit board) from about 2.0 to 150. into 50 ohm;
the "standard" internal gain settings (front panel potentiometer at maximum) for output into 50 ohm are:

- individual channel gains of 25/2.0 [high gain/low gain version]
- summed channel gains at half individual channel gains;

the "standard" front panel setting is 40% of maximum (overall gain of 10/0.8).

(1.8) Cross talk

Below 2% between adjacent channels and less between non-adjacent channels for 5 ns rise-time signals, if all outputs are terminated; decreases with increasing rise-time of signal.

(1.9) Random high frequency noise

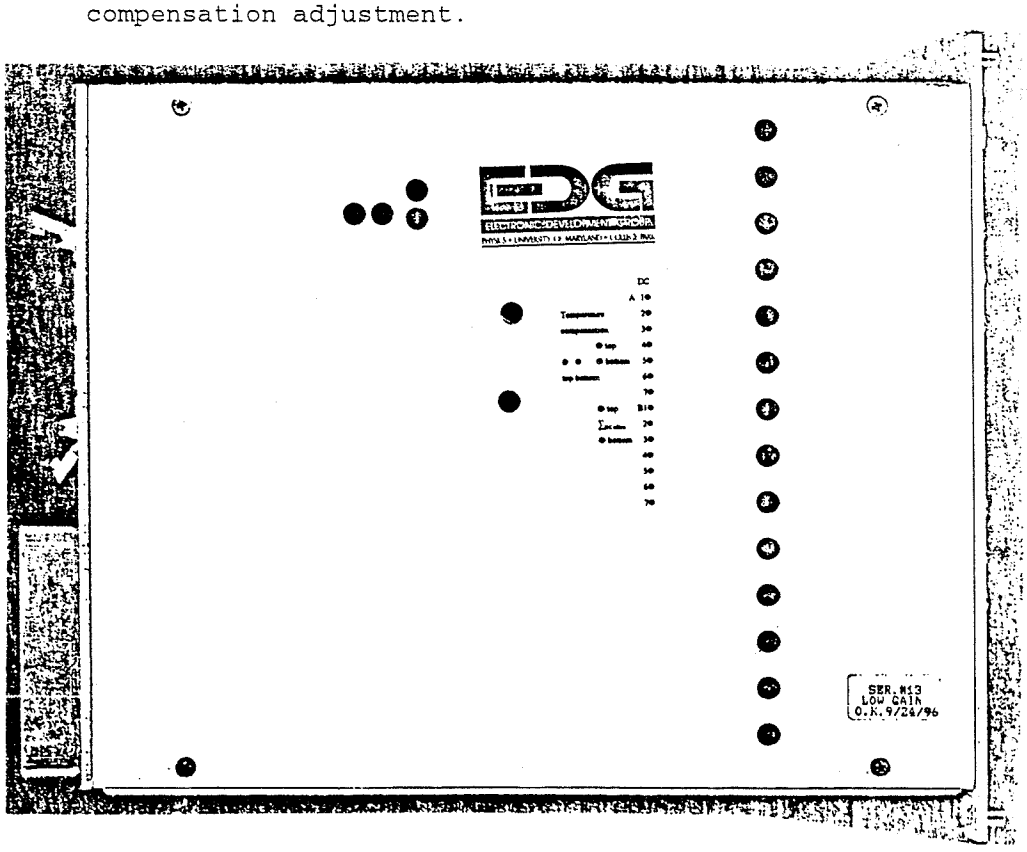
~ 0.2 mV peak-to-peak non-attenuated-input equivalent for individual channels at ~100 MHz;

~< 0.2 mV input-equivalent for summed channels at 30 ns output rise time [from ADC: summed channel: 2 mV at maximum-gain setting of 15].

(1.10) DC offset control (Fig. 3)

Side panel accessible control for each channel;
side panel accessible additional control for each summed output;
side panel accessible adjustable temperature drift compensation for each summed output;
temperature sensor output at front panel;
DC offset will change slightly with front panel gain setting;
DC offset and temperature compensation setting needs to be readjusted after any internal gain change;
for count rates below ~ 100 KHz external AC coupling can be used to eliminate any DC offsets and offset drifts.

FIGURE 3: Side panel with access holes for DC and temperature compensation adjustment.



(2) FUNCTIONAL DESCRIPTION (circuit diagrams Figs. 4 to 6)
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(reference is made to components in channel A1)

(2.1) Input and first amplifier stage (Fig.4)

A fraction F of the full input signal is taken from the 15-turn potentiometer R17 (100 ohm) and provides the input to amplifier U4. The addition of the 100 ohm resistor R19 in parallel to R17 provides 50 ohm input impedance. The diodes D1,D2 and R6 protect the amplifier from brief signals exceeding about +/-6V. The "input bias current" of the amplifier U4 causes the output DC level to depend somewhat on the setting of R17.

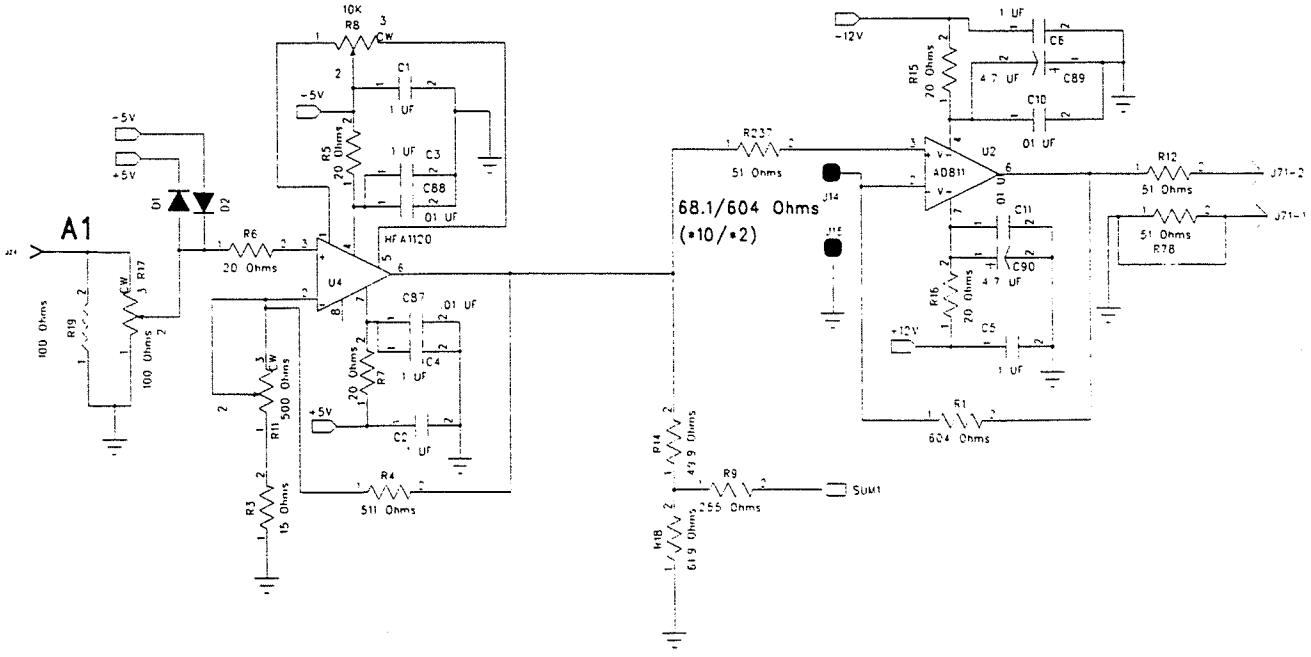
The first amplifier stage U4 is a ~500 MHz HFA1120. Its output, going into 100 ohm, is limited to about +/- 4.5 V and 65 mA. The gain G1 in amplifier U4 can be set via the 3/4 turn potentiometer R11 (500 ohm) in series with R3 = 15 ohm. G1 = 1.0+R4/(R11+R3) and has a range of 2.0 to about 35. Note that the output DC-level and the temperature dependence of DC-drifts will change with R11 gain setting. Potentiometer R8 is provided to adjust the DC level to zero, ideally as observed at the ribbon output J71-2/J71-1.

(2.2) Individual output branches (Fig. 4)

The output of U4 is split to go to the summer (see below) and to the second amplifier stage U2. U2 is a ~100 MHz AD811 amplifier with a +/- 9 volt and 100 mA output capability. The feedback resistor R1=604 ohm is chosen to limit overshoots. The exchangeable gain resistor is located between posts J14 and J15 with a value of 68.1 ohm to yield a gain of G2 = 10, or 604 ohm for a gain of 2.0. Note that, except for channel B7, all of these exchangeable gain resistors are located on the back of the circuit board.

Due to the 50 ohm output resistor R12, a 50 ohm load (e.g. ADC, oscilloscope) sees only half the internal signal amplitude. Thus, the

FIGURE 4: One individual branch, Channel A1.



total gain is G = F * G1 * G2 * 0.5. The "standard" gain is G=10, with F=0.4, G1=5.0, and G2=10.0, providing a gain range of G = 0...25 with F varied from 0 to 1.0. If 100 ohm back-termination is desired, the circuit-board trace parallel to R78 can be cut to provide 100 ohm pseudo-differential termination on the amplifier output.

(2.3) Summing branch (Figs. 4,5)

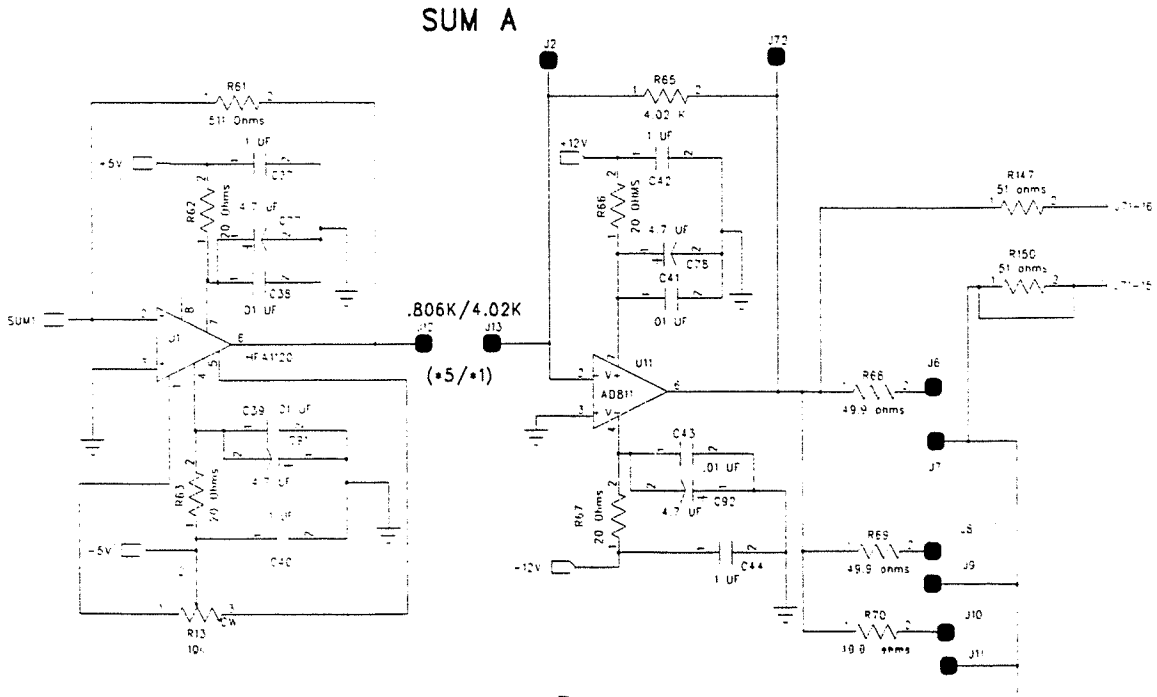
The second output of U4 goes via R14,18 and R9 to ground through a total of 100 ohm (the SUM1 input from R9 is at virtual ground). Half the signal - to minimize cross talk between channels - is summed through R9, along with channels A2 to A7 and the temperature compensation output, into the inverting input of U1. The gain G3 of U1 in the inverting configuration is G3 = -R61/R9. A fixed gain of -2.0 (R9 = 255 ohm) is chosen to compensate for the R18,R14,R9 signal attenuation.

U11 provides the final summed-signal amplification, with the output rise time controlled by the feedback resistors R65 and any resistor placed between J2 and J72 (call it R65'). The gain resistor (Rg), placed between J12 and J13, should be chosen so that Gain = -1.[(1/R65+1/R65') * Rg]. The default values are R65 = 4020 ohm, Rg = 806 ohm for a gain of -5.0 and a rise time of at least 30 ns. Measured rise-time and random-noise total-amplitude values for a gain of -5.0 in U11 with an overall gain of 100 are (R65' = 0 ohm):

		rise time (ns)		
R65(ohm)	Rg(ohm)	10/90%	10/80%	noise (mV)
511	102.5	<10	7.5	44
1100	222	19	14	27
1960	392	28	21	17
5460	1100	74	53	14

The output is deliberately slowed down to make the summed output less sensitive to mismatches in input signal arrival times. It also makes timing of subsequent multiplexer modules easier. In addition, the

FIGURE 5: Summing circuit, channel A.



high frequency random noise contributions are reduced. The rise time can be reduced by adding a resistor R65'; the minimum recommended total value for R65/R65' is 511 ohm to avoid oscillations.

The summed signal outputs are available on channel 8 of the ribbon cable (see individual channel description) and through three front panel Lemo connectors (J6,J8,J10). Each is back-terminated with 50 ohm. The absolute output voltage maximum of +/- 4.5 V may be reduced by the maximum current limit of 100 mA of U11 if front outputs in addition to the ribbon cable output are used (1/2/3 Lemo output used: +/-3.3/2.0/1.4V with 100 ohm ribbon, +/-2.5/1.66/1.25V with 50 ohm ribbon termination).

(2.4) Power supply features

The +/-6 and +/- 12 V supply lines are protected by soldered-in fuses and RF shielded by ferrite beads. Electrolytic capacitors provide further isolation between different modules. The +/-6 V supplies are converted to about +/-5.2 V by dropping 0.8 V on diodes. The inductance of the ferrite beads is either 4 or 30 micro-H. The capacitors are either 220 or 10 micro-F. The different values are the result of attempts to control the shutdown of +/- 12V on the NIMbin power supply, which is remedied now by a change to the NIMbin power supply itself. See also the remarks in chapters (1.6) and (6.3).

(2.5) Temperature dependent DC offset compensation, general features
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U37 and U35 in Fig. 6 provide circuitry for a temperature dependent current source fed into the summing input of U1. Potentiometer R316 controls the gain which is proportional to the voltage measured on test point J31-01.

IMPORTANT NOTE: the temperature compensation for the temperature dependent summed-signal DC-offset has to be adjusted each time the internal gain potentiometers (white pots) are changed. This rather tedious and time-consuming procedure is described below. In contrast, changing (a) the gain at the front panel input potentiometer or (b) changing the internal gain resistors has only a very slight impact on the temperature dependence of DC the offset.

(2.6) Temp. dependent DC offset compensation, functional description
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The DC levels of all amplifier outputs drift somewhat with changes in temperature, easily visible during the first 10 to 30 minutes of warmup after the NIM-power was turned on. Since the effect is most serious in the summed outputs (intended to be used with discriminators) a temperature compensation network has been added for the summed outputs.

The variable DC offset originates primarily from the temperature dependent current and voltage offsets in the seven inputs of the first amplifier stages. The temperature dependence is different for each amplifier chip. It also depends stongly on the gain setting of the first amplifier stage (adjustable with the white potentiometers); thus any modification of these gains must be accompanied by a new (time-consuming) temperature compensation adjustment.

The temperature sensor (U37,LM34) (Fig. 6) delivers 10 mV per degree Fahrenheid (degF) which is amplified by a factor of 2.0 (R313/R312) in the following amplifier (U35A). The voltage is accessible at a front panel output (J32-1); a typical value of 1.80 V corresponds to 90 degF

at the sensor.

A second amplifier (U35B) provides an identical output of opposite polarity. A potentiometer (R316) between the two amplifier outputs allows to select the desired temperature sensitivity; a test point (use high impedance) (J31-1) is provided for monitoring the adjustment. At 0 mV test point value there is no temperature compensation. Potentiometer and test point are accessible through holes in the module's side cover.

The potentiometer output feeds into the summing input of the first summing amplifier (U1) via a 5.1 kohm resistor (R322); together with the 511 feedback resistor (R61) this results in a gain of 0.1. The second summing amplifier (U11) gain resistor (between J12 and J13) is normally set to 806 ohm or 4.02 kohm, resulting in a GAIN of 5.0 or 1.0 (assuming the normal 4.02 kohm feedback resistor R65). Thus the test point value is normally attenuated by a factor of ATTEN = 0.5 or 0.1 when viewed at the front panel summed output (using >1 Mohm instrument).

The temperature compensation adjustment is accompanied by a DC offset which has to be removed with the summed signal DC offset potentiometer (R13), accessible through the side panel.

EXAMPLE (all measurements with a >1 Mohm voltmeter):
An increase of temperature of 30 degF from 90 to 120 degF will result in a front panel voltage change from 1.80V to 2.40V, i.e. by +0.60V (20 mV/degF). If the potentiometer was set to yield a test point value of -225 mV at 90 degF, its value will change by 0.60/1.80*(-225mV)= -75 mV to -300 mV, or by -2.5 mV per degF at the test point.
At the front panel summed output this translates into

```
      -2.5 mV * ATTEN * temperature-change,
i.e., -2.5 mV * 0.5   * 30 = -37.5 mV at GAIN=5.0
or                         = - 7.5 mV at GAIN=1.0.
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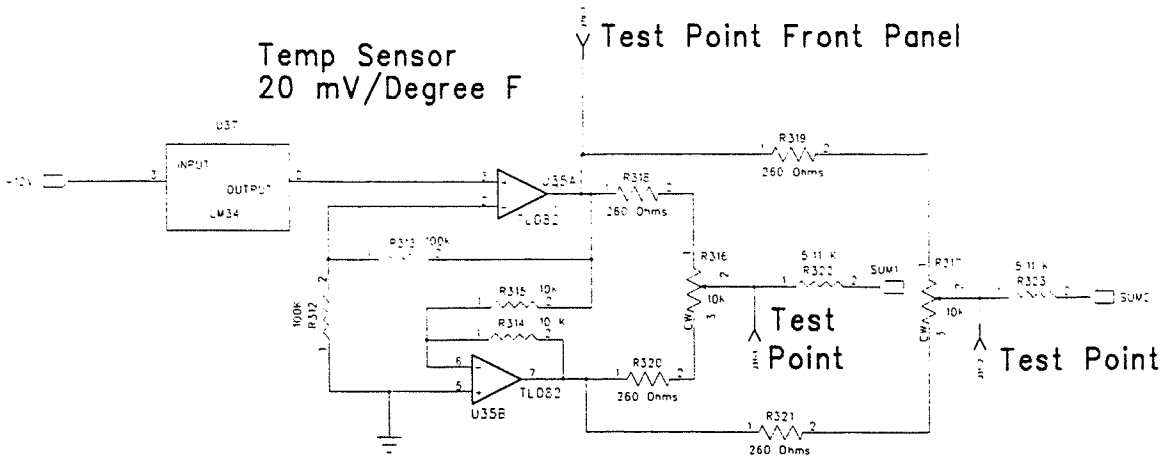
FIGURE 6: Temperature compensation circuit.



(3) PROCEDURE FOR GAIN ADJUSTMENT

Note: internal gain change may require temperature compensation adjustment; see below before proceeding with gain adjustment.

(0) For new modules: let the modules age under power for a week or more.
(1) If needed: select and replace fixed gain resistors (partially on back of circuit board!).
(2) Connect module to NIM power and wait about 15 minutes or more with power on for temperature equilibrium.
(3) Provide input signal which, after amplification does not saturate the output (e.g., attenuated out-bar from a logic module); determine the ampitude into amplifier module (i.e., measure with high impedance voltmeter from a Tee-connector).

-- Set internal gain identical on each channel and set each DC offset.
(4) Turn input attenuator (outside gain control) to 100% of maximum.
(5) Observing the ribbon cable output, adjust DC offset to zero (blue potentiometer) and the gain to desired value by adjusting the white potentiometer. The DC-offset will change during gain adjustments, so several cycles of DC and gain adjustment may be needed. Remember that the output amplitude into 1 Mohm is twice as high as into 50 ohm.
(6) Repeat (4) and (5) for each channel and also for the summed outputs.

--- Set external gain to 40% of range. Do not set too low an external gain, compensated by a huge internal gain, as this maximizes the intrinsic amplifier noise and DC drifts with temperature.
(7) Use the same input signal as before.
(8) Adjust the front panel gain control to 40% of previous value.
(9) Check and set all DC values to 0 including the summed output.
(7-9) Alternately one can observe the front panel summed output and only change the input channels; this can be done if the DC levels shift only insignificantly. Note that the summed output gain may be different from the individual signal gains.
(10) Adjust the temperature compensation network if the white potentiometer gain settings have been changed. (See below).

(4) PROCEDURE TO ADJUST TEMPERATURE COMPENSATION

Note: the temperature compensation network only operates on the summed outputs.
Note: adjust the temperature compensation each time after any of the first-stage gains has been changed with the white potentiometers.
Needed:
- one NIM bin with (!) forced air flow;
- one space heater;
- one high impedance voltmeter, with LEMO adaptor;
- one screwdriver, insulated, able to reach through closed side panel;
- connection between side-panel test-point and voltmeter; suggestion: LEMO cable with connector part on one end screwed off, exposing the pin which can be inserted into the test point;
- several hours to cycle through temperature changes and to do adjustments.

Note: all measurements are assumed to be made with high-ohm voltmeter;
if a 50 ohm instrument is used, the summed output values are
attenuated by a factor of 0.5.

(1) Make sure that the internal amplifier gains have been set to the desired values. First-stage gain changes (white potentiometers) require new temperature compensation settings; front panel gain changes do not.
(2) Determine the summed output gain, defined by the removable gain resistor (4.02 kohm: gain of 1.0; 804 ohm: gain of 5.0).
(3) - Insert insulated leads (modified Lemo cables) into testpoints to allow voltmeter measurement.
- Place unit into a NIMBIN with forced air flow (fans) with space for potentiometer adjustment through the side panel from the left.
- Turn on NIM power and wait at least 15-30 minutes for temperature equilibrium (temperature sensor is much faster than amplifiers!).
- Keep forced air flow (fans) on at all times.
(4) Turn temperature compensation (TC) potentiometers to achieve 0 +/-1 mV reading at test point through side panel opening.
(5) Measuring at front-panel Lemo summed-output, adjust the DC level to 0 mV offset.
(6) Measure and record
- the front panel TEMP value and
- the summed output DC-offset value.
(7) Use a space heater or similar device to increase the air temperature which is drawn through the unit, to simulate an environmental temperature change. (Note: blocking air flow to increase the internal temperature instead of changing the temperature of the forced air flow does not yield adequate results.)
(8) After 30 to 60 minutes equilibrium should be achieved. Measure and record the TEMP and summed-output DC values for this temperature.
(9) Remove heater, let cool down, measure TEMP and DC-offsets again.
(10) Determine the change in testpoint value needed by:
NEEDED = -10.0 * delta-DC / delta-TEMP * TEMP / GAIN , where
- = want to compensate, not enhance;
10.0 = 1/gain of first amplifier stage for temperature stabilization circuit;
delta-DC = change in summed output DC value (into 1 Mohm);
delta-TEMP = change in front panel TEMP test point value;
TEMP = Value of TEMP output at the time of potentiometer adjustment;
GAIN = second summing amplifier gain (see above), 5.0 or 1.0;
(12) Measure side panel test point value, add "NEEDED" to value, and adjust potentiometer to the new value (test-point + NEEDED).
(13) Adjust summed-output DC offset to 0 mV.
(14) If desired, further iterations ((6) to (13)) can be done.

Note: At an internal gain of 12.5 into 50 ohm for the summed output (i.e., "HIGH GAIN" setting), typical drift values are 0.3 mV/degF. Compensation reduces this to about 0.05 mV/degF.
Individual channels drifts at the same "HIGH GAIN" internal setting of 25.0 have been measured for four modules, with an average of 0.11 mV/degF into 50 ohm. The individual results are:

Module 3: A1-7: +0.07, 0.12, 0.01, 0.07, 0.16,-0.07, 0.12 mV/degK
B1-7: +0.32, 0.15, 0.11, 0.17, 0.05, 0.15,-0.07 mV/degK
4: A1-7: +0.08, 0.16, 0.17, 0.16,-0.01, 0.16, 0.16 mV/degK
B1-7: +0.07, 0.19, 0.26, 0.18, 0.17, 0.17,-0.03 mV/degK
5: A1-7: +0.07, 0.06, 0.05, 0.03, 0.21, 0.09, 0.13 mV/degK
B1-7: +0.02, 0.08, 0.19, 0.14,-0.01, 0.02, 0.08 mV/degK
6: A1-7: +0.19, 0.24, 0.07, 0.20, 0.19, 0.06,-0.02 mV/degK
B1-7: +0.16,-9,12,-0.02, 0.01, 0.10, 0.01, 0.18 mV/degK

A 1 mV DC level change at an ADC with 50 ohm input, 0.1 pC/channel, and a 100 ns gate corresponds to 20 channels of pedestal shift.

(5) INITIAL SETUP OF MODULES

The gain settings (as of Jan. 1998) for all modules produced are given in Table 1. The table also shows ownership and temperature compensation settings affecting the summed outputs for the individual module-sections. Serial # 3-10, 16-18 are set up as "HIGH GAIN" modules for the total absorber detectors, # 11-15 are the "LOW GAIN" modules for the preradiator detectors. The different gains for the summed outputs compensate for the differences in photo-tube gain (factor 25) between preradiator and total absorption detectors. This is needed for proper total analog signal summing [chapter (6)].

TABLE 1: Owners and adjustable settings for all Amplifier/Summer modules.
Columns are:
- Serial number;
- Ownership Hall A or C (#0 is prototype);
- first stage gain;
- second stage gain, individual;
- second stage gain, sum;
- front potentiometer setting in % of full scale;
- individual channel gain into 50 ohm (= 1/2 of gain into 1 Mohm);
- summed output gain into 50 ohm (= 1/2 of gain into 1 Mohm);
- temperature compensation setting at typical 1.6 V temperature reading (80 degF), first for top module-section (A), second for bottom module-section (B).

* = should be checked again after burn-in time

Ser. #	Owner Hall	st.1 gain	st.2i gain	st.2s gain	front pot.	gain indiv	gain sum	temp.comp. A / B
0	UMD	2.0	2.0	5.0	50%	1.0	2.5	*
1	C	2.0	2.0	5.0	50%	1.0	2.5	+ 47/+ 61mV *
2	C	2.0	2.0	5.0	50%	1.0	2.5	- 1/- 2mV *
3	A	5.0	10.0	10.0	40%	10.0	10.0	- 50/-106mV
4	A	5.0	10.0	10.0	40%	10.0	10.0	-143/-120mV
5	A	5.0	10.0	10.0	40%	10.0	10.0	- 90/- 71mV
6	A	5.0	10.0	10.0	40%	10.0	10.0	-128/+ 19mV
7	A	5.0	10.0	10.0	40%	10.0	10.0	-106/- 89mV
8	A	5.0	10.0	10.0	40%	10.0	10.0	+ 17/- 92mV
9	A	5.0	10.0	10.0	40%	10.0	10.0	-121/- 31mV
10	A	5.0	10.0	10.0	40%	10.0	10.0	- 44/- 27mV *
11	A	2.0	2.0	1.0	40%	0.8	0.4	+ 81/- 80mV
12	A	2.0	2.0	1.0	40%	0.8	0.4	+ 35/+ 54mV
13	A	2.0	2.0	1.0	40%	0.8	0.4	+100/+ 74mV
14	A	2.0	2.0	1.0	40%	0.8	0.4	+ 11/+ 12mV
15	A	2.0	2.0	1.0	40%	0.8	0.4	+ 22/- 13mV *
16	A	5.0	10.0	10.0	40%	10.0	10.0	- 42/- 49mV *
17	A	5.0	10.0	10.0	40%	10.0	10.0	- 80/- 18mV *
18	A	5.0	10.0	10.0	40%	10.0	10.0	- 77/- 85mV *

(6) USE OF SUMMING FEATURE FOR HALL-A SHOWER COUNTER

(6.1) Shower counter and signal cable details

The CEBAF Hall-A Electron Spectrometer Shower-Counter consists of an array of 2x24 = 48 preshower lead-glass detectors (area of 35x10 cm**2 each) and an array of 6x16 = 96 total absorption detectors (15x15 cm**2 each).

The two arrays are placed behind each other and can be viewed as 8 identical SEGMENTs in which preraditors (2x3 detectors = 70x30 cm**2) and total absorption detectors (6x2 detectors = 90x30 cm**2) exactly overlap, with an extra 10 cm of total absorption counter on each side to contain the expanding shower. Detectors and signal cables are numbered as given in Table 2.

TABLE 2: Relative location and cable numbering scheme for HALL A shower counter detectors. Orientation shown is as seen from the target (along the spectrometer z-direction), with the low momentum region at the top (low detector numbers).

Preradiator	total Absorber	
1L 1R	6 5 4 3 2 1	
2L 2R	12 11 10 9 8 7	= SEGMENT 1
3L 3R		
4L 4R	18 17 16 15 14 13	
5L 5R	24 23 22 21 20 19	= SEGMENT 2
6L 6R		
7L 7R	30 29 28 27 26 25	
8L 8R	36 35 34 33 32 31	= SEGMENT 3
9L 9R		
10L 10R	42 41 40 39 38 37	
11L 11R	48 47 46 45 44 43	= SEGMENT 4
12L 12R		
13L 13R	54 53 52 51 50 49	
14L 14R	60 59 58 57 56 55	= SEGMENT 5
15L 15R		
16L 16R	66 65 64 63 62 61	
17L 17R	72 71 70 69 68 67	= SEGMENT 6
18L 18R		
19L 19R	78 77 76 75 74 73	
20L 20R	84 83 82 81 80 79	= SEGMENT 7
21L 21R		
22L 22R	90 89 88 87 86 85	
23L 23R	96 95 94 93 92 91	= SEGMENT 8
24L 24R		

(6.2) Logic for summing and trigger formation (Fig. 7)

Summed analog detector signals are used to obtain event trigger signals via discriminators. The goal is to sum detector signals in such a way that there always exists an analog signal containing the energy deposited by the full shower from a particle, while at the same time only summing a subset of all detectors to minimize noise contributions from detectors without signals. This goal was realized by summing all signals from each SEGMENT and then summing adjacent SEGMENTs, as shown in the circuit diagram, Fig. 7, and as described next.

The signals in each box in the detector list above (Table 2), bordered by the symbols ":" and "-", are summed in one Amplifier/Summer module-section (i.e., one half of a complete NIM module, "Amp/Sum"). As shown in Fig. 7 for SEGMENT 1, preradiator signals 1R, 2R, 3R, 1L, 2L, 3L are summed in one module-section (Preradiator SEGMENT 1, PS1); total absorbers 1, 2, 3, 7, 8, 9 (TS1a) and 4, 5, 6, 10, 11, 12 (TS1b), respectively, are summed in two additional module-sections. The sequence of inputs and summing originates from the physical separation of cable runs on the left and right of the detector arrays.

NOTE: While the sequence of inputs within each section is of no consequence for the summed signal, the sequence matters for the individual analog signals which are cabled on the back of the Amplifier/Summer modules to individual ADC channels with a one-to-one input to ADC correspondence!

Commercial linear fan-in/out modules are used for the subsequent analog signal sums. PSi, TSia, and TSib are summed to obtain the full signal amplitude Si for SEGMENT i. Before summing, PSi is delayed by 20 ns long cables to compensate for the different transit times of the different types of photo-tubes used for preradiator and total absorber detectors.

The shower of secondary particles from an event can spread to about 10 cm in diameter (in the transverse direction) and therefore can cross one SEGMENT boundary. Thus adjacent SEGMENT signals are summed, resulting in 7 final signals, S12, S23, S34, S45, S56, S67, and S78. These are input into seven CAMAC discriminator channels.

In addition to these adjacent-SEGMENT signals, two more signals are formed:

(PT1-8): the sum of all Si, i=1,8, i.e., the total analog sum of all preradiator and total absorption counters;

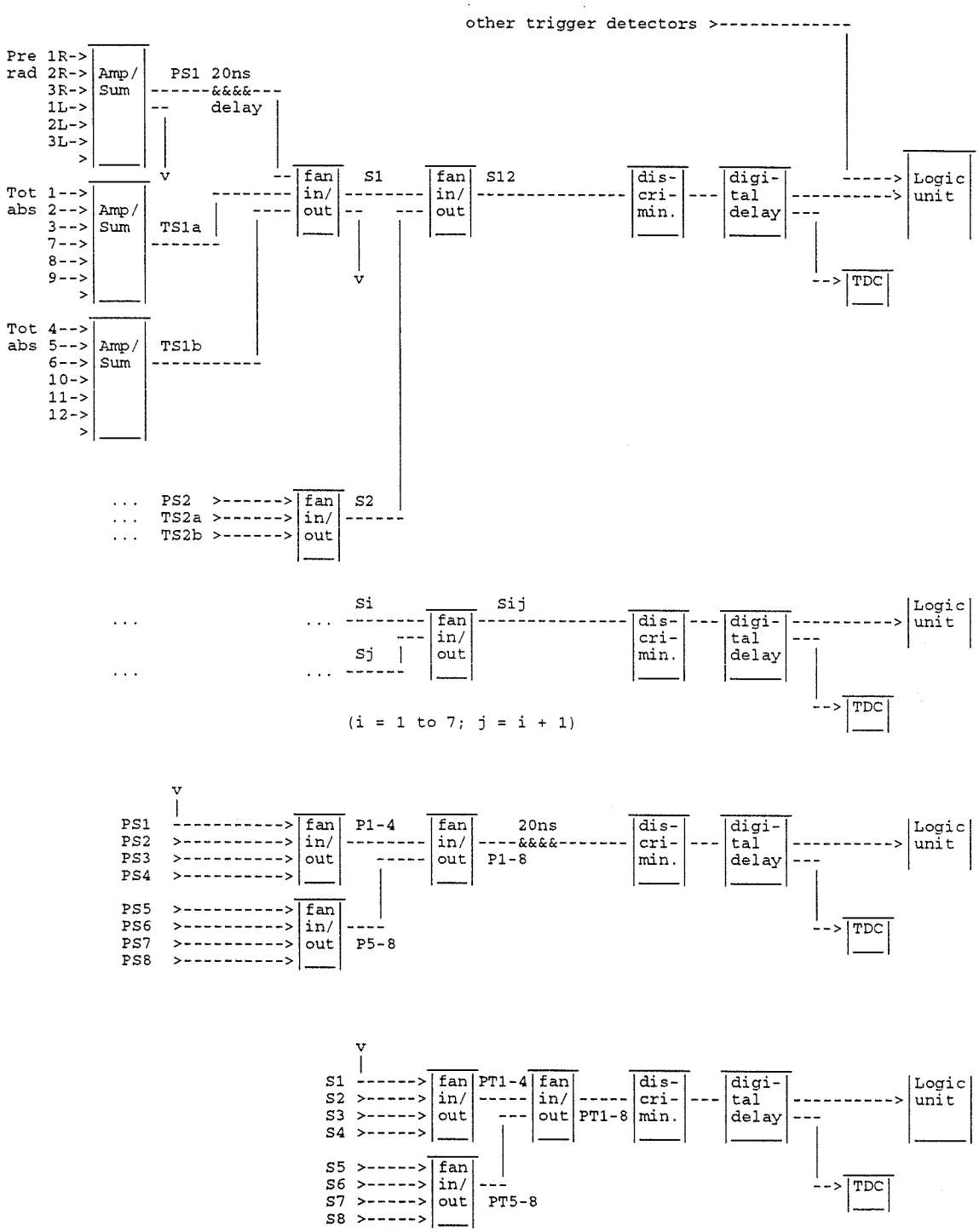
(P1-8): the sum of all PSi, i=1,8, i.e., the total analog sum of all preradiator counters.

These signals are also input into discriminators, where the P1-8 signal is delayed by an additional 20 ns, for the reason stated above.

The 9 analog signals, after processing in discriminators, result in 9 logic signals which are delayed by a common time interval in a digital delay unit and presented to a logic memory lookup unit (Logic unit), which also has inputs from other trigger determining detectors. The logic unit determines the trigger condition. A second output of the delay unit provides signals for time-to-digital converters (TDC).

NOTE 1: It is important that all coincident signals are timed correctly to arrive at the analog summing units at the same time for the

FIG. 7: Circuit diagram showing the summing of shower counter detector analog signals from the preradiator (Pre-rad) and total absorber (Tot-abs) to form logic signals in the discriminators (dis-cri-min.) to be used for time-to-digital converters (TDC) and as input to trigger logic decisions in the Logic unit. For details see text.



discriminators to work as intended. Due to the deliberately large time constant of the summing module outputs, the limit of acceptable time variation between detector signals is about 5 ns.

NOTE 2: One of the detectors (#79) is AC-coupled (via 15 nF capacitor) due to a permanent DC offset. In addition, signal PT1-8 is AC coupled in the same way before going into the discriminator to insure that at least one signal is independent of any DC drifts in the sum of the many analog modules.

NOTE 3: The total sum PT1-8 is delayed by one additional fan in/out module, and thus this Logic Unit input will be approximately 7-8 ns later (6 ns transit for LeCroy 428F plus cable) than the inputs of the other branches.

(6.3) Details of module location and cabling used (Fig. 8)

Since each Amplifier/Summer module contains 2 module-sections, 4 modules are needed for the preradator and 8 modules are needed for the total absorber detectors. In addition 6 fan-in/out modules (each module has 4 module-sections with 4 inputs each) are required (LeCroy model 428F is used).

These 18 modules require two (6,12,24V) NIM bins, with non-standard high-current capability for +-12 V. Ortec model 4001C/4002E was chosen. While the 12 V steady-state current of this model is sufficient with a wide margin, the power-on surge usually shuts down one of the two 12 V supplies when more than about 4-6 amplifier/summer modules are in use [compare chapters (1.6) and (2.4)]. It was found that other supplier's NIM bins have the same problem. Modification of the amplifier/summer module input current filters (capacitors, inductances) do not remedy the NIM-bin shut-down problem. Per our request, Ortec modified three NIM bin power supplies, two of which are in use and one is a spare supply. The remaining units, discriminators, digital delays, TDCs, and the Logic Unit (MLU) are located in CAMAC crates and are mostly connected via ribbon cables.

NOTE: Use only NIM-bins with ORTEC-modified trip-circuits for the +- 12 V power supplies!

The location of the NIM modules and module-sections in the two NIM-bins can be determined from the following diagram (Fig. 8). The notation corresponds to the circuit diagram shown in Fig. 7. The length of the connecting cables are also shown in Fig. 8. Lemo-type cables are used except for the 24 ns delays which are RG58 cables with Lemo connectors. The AC coupling capacitor has a value of 15 nF.

Not shown in any of the diagrams of this manual is the routing of the individual analog signals to the ADCs. These signals exit the Amplifier/Summer units at the back panel (Fig.2) and go via 50 ohm coaxial ribbon adaptor cables to BNC patch panels. Low-loss delay lines (order of 300-400 ns long) lead from this patch panel to one near the ADCs. This patch panel is connected via the same type of adaptor cable through capacitive couplers into the ribbon-type ADC inputs. The capacitive coupler was developed and built in the University of Maryland Physics Department and consists of a circuit board with 15 nF capacitors on all 16 signal cables with connections for 110 ohm ribbon cables.

Some of the empty slots of the NIM-bins are populated with spare module to allow for easy switch-over in case of module failure.

FIGURE 8: NIM-Bin slot population with Amplifier/Summer modules and with fan-in/out modules for the two NIM-Bins in use.
The output signals of the module-sections are given with the notations used in Fig. 7.
The connections are made with cables as indicated.
The discriminators are located in a separate Camac crate.

slot #

1	2	3	4	5	6	7	8	9	10	11	12
Amp/ Sum	Amp/ Sum	spare	Amp/ Sum	Amp/ Sum	Amp/ Sum	Amp/ Sum	spare	fan i/o	fan i/o	fan i/o	spare
PS1	PS3		TS1a	TS1b	TS3a	TS3b		S1	S12	spare	
								S2	S23	P1-4	
PS2	PS4		TS2a	TS2b	TS4a	TS4b		S3	S34	P5-8	
								S4	S45	P1-8	
PS5	PS7		TS5a	TS5b	TS7a	TS7b		S5	S56	PT1-4	
								S6	S67	PT5-8	
PS6	PS8		TS6a	TS6b	TS8a	TS8b		S7	S78	PT1-8	
								S8	spare	spare	

cables lengths used, in nanoseconds:

for i = 1 to 7; j = i + 1:
  PSi -- 24ns -- Si
  TSia -- 4ns -- Si -- 1ns (2ns @ i+1=5) -- Sij -- 9ns --- Discriminator # i
  TSib -- 4ns -- Si

for i = 1 to 4; j = 5 to 8:
  Si -- 4ns -- PT1-4 -- 1ns -- PT1-8
  Sj -- 4ns -- PT5-8 -- 1ns -- PT1-8 -- 1ns -- Capacitor -- 8ns -- Discr. # 8

  PSi -- 4ns -- P1-4 -- 1ns -- P1-8
  PSj -- 4ns -- P5-8 -- 1ns -- P1-8 -- (20ns) ------ 9ns -- Discriminator # 9

Note that some cables are color coded with a permanent marker (sequence: red, green, blue, black) and then tied into bundles.

[above is as cabled on December 17, 1997]